Effects of Channel Width on Electrical Characteristics of Polysilicon TFTs With Multiple Nanowire Channels

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***Abstract*—This brief studies the electrical characteristics of a series of polysilicon thin-film transistors (poly-Si TFTs) with different numbers of multiple channels of various widths, with lightly doped drain (LDD) structures. The nanoscale TFT with ten 67-nm-wide split channels (M10) has superior and more uniform electrical characteristics than other TFTs. Additionally, experimental results reveal that the electrical performance of proposed TFTs enhances with each channel width decreasing, yielding a profile from a single-gate to tri-gate structure.**

***Index Terms*—Lightly doped drain (LDD), nanowire, polysilicon, thin-film transistor (TFT).**

I. Introduction

Polysilicon thin-film transistors (poly-Si TFTs) have attracted much considerable attention because they can be applied in active-matrix liquid-crystal displays (AMLCDs), since they perform very well and can be integrated with peripheral driving circuits on a low-cost glass substrate [1], [2]. Also, poly-Si TFTs have the potential to be used in three-dimensional (3-D) circuits, including vertically integrated SRAMs [3] and DRAMs [4]. Conventional top single-gate poly-Si TFTs, however, exhibit some nonideal effects when applied. First, they suffer from anomalous leakage current in the OFF-state, which correlates with the drain voltage and the gate voltage [5], [6]. This undesirable large OFF-state leakage current limits the application of poly-Si TFTs in switching devices. The dominant mechanism by which the leakage current in poly-Si TFTs is induced involves the field emission of carriers in grain boundary traps, due to the high electric field near the drain junction [7]. An effective method for reducing the electric field in the drain region is to incorporate a lightly doped drain (LDD) region between the heavily doped region and the active channel region [8]. Second, the presence of polysilicon grain boundary defects in the channel region of TFTs drastically affects the electrical characteristics [9], [10], especially when the device dimension is scaled down. Therefore, reducing the number of polysilicon grain boundary defects will improve the performance of poly-Si TFTs. TFTs with several multiple channels have been reported to effectively reduce grain boundary defects [11]–[13]. Additionally, scaling down of TFTs dimension is a continuous trend since its benefits in performance. Smaller device size enables higher device density in SRAMs and DRAMs, and increases the driving current in peripheral driver circuits in AMLCD applications. However, as a TFT's dimensions are reduced, influences from the drain side of the channel become significant, (i.e., gate control becomes lower), which will arise severe short-channel effect, including threshold voltage roll-off, a large subthreshold slope (*SS*), a large drain-induced barrier lowering (DIBL) and the occurrence of kink-effect. These effects are major limitations in realizing a system on panel (SOP). In CMOS technology, many high-performance surrounding gate structures in a silicon-on-insulator (SOI) MOSFET, such that double-gate [14], tri-gate [15], FinFET [16] and gate-all-around [17], have been reported to exhibit superior gate control over the channel than a conventional single-gate MOSFET, to reduce short-channel effects.

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TABLE I
Device Dimensions of M10, M5, M2 and S1 TFT. All Devices Have the Same Active Channel Thickness of 50 nm, and Gate Oxide Thickness of 26 nm

Device name	Gate length (L)	Channel Number	Each channel width (W)
M10	0.5 um	10	67 nm
M5	0.5 um	5	0.18 um
M2	0.5 um	2	0.5 um
S1	0.5 um	1	1 um

In this brief, we first apply the tri-gate structure on short-channel (gate length $= 0.5\ \mu$m) poly-Si TFTs design, also employed multi-channel with different widths and LDD structures. Experimental results show that the electrical characteristics are highly depended on the channel's width. The ten-nanowire-channels (M10) TFT shows the best gate control, and its short-channel effects are more reduced than other TFTs, which is responsible its for excellent performance.

II. Device Structure and Fabrication

In this brief, a series of TFTs, with a gate length of 0.5 um, consisting of ten strips of multiple 67 nm wire channels (M10) TFT, five strips of multiple 0.18-μm channels (M5) TFT, two strips of 0.5 μm channels (M2) TFT and a single-channel structure (S1) with $W = 1\ \mu$m TFT, were fabricated, as listed in Table I. Fig. 1(a) presents the structure of the M10 TFT. Fig. 1(b) presents the cross section of the M10 TFT perpendicular to the AA$'$ direction. This M10 TFT has a conventional top-gate LDD MOSFET structure. Fig. 1(c) presents cross section of the M10 TFT perpendicular to the BB$'$ direction, in which the channels were surrounded by the gate electrode as tri-gate structure. Fig. 2 presents device electrical characteristics simulation results using the DESSIS software from ISE. The double-gate TFT simulation results serve to tri-gate TFT due to the similar dimension. Fig. 2(a) shows the encroachment of electrical field from drain side of S1 TFT. However, in Fig. 2(b), M10 TFT can confine the electrical field due to its superior tri-gate control. Therefore, it is expected that the M10 TFT tri-gate structure can suppress effectively short-channel effects.

The devices were fabricated on 6-in silicon wafers with a 400-nm-thick layer of thermal oxide layer substrate. A thin 50-nm-thick undoped amorphous-Si (a-Si) layer was deposited by low-pressure chemical vapor deposition (LPCVD) at 550 °C. The deposited a-Si layer was then recrystallized at 600 °C for 24 h in nitrogen ambient. After electron beam (ebeam) direct writing and reactive ion etching (RIE), the device active islands were formed. Then, a 26-nm-thick layer of tetra-ethyl-ortho-silicate (TEOS) oxide and a 150-nm-thick layer of undoped polysilicon were deposited by LPCVD, and transferred to a gate electrode by ebeam direct writing and RIE. Phosphorous ions were implanted in the lightly doped source and the drain region at a dose of 5×10^{13} cm^{-2}. A 200-nm-thick layer of TEOS oxide was then deposited by LPCVD, and anisotropically etched by RIE

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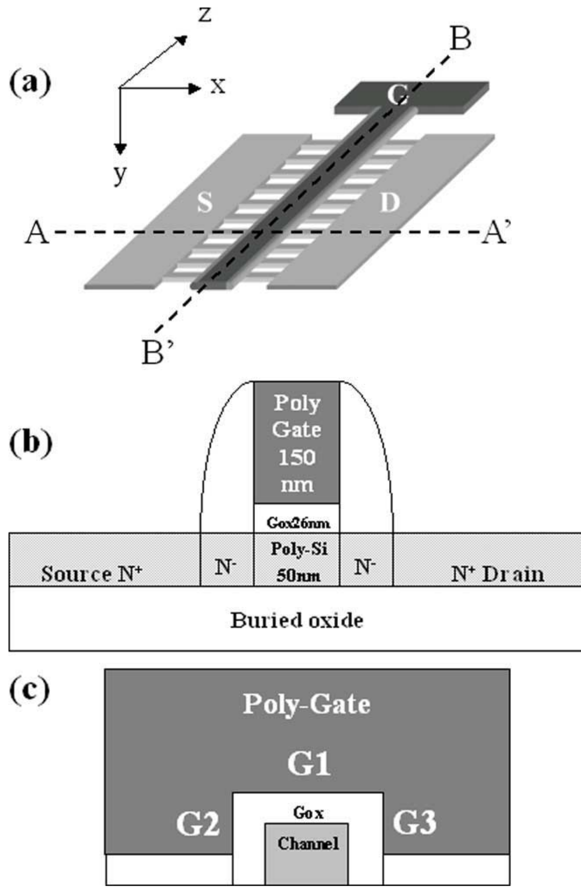

Fig. 1. (a) Schematic diagram of M10 poly-Si TFT. (b) Cross-sectional view of (a), AA′ direction, as a conventional top-gate LDD MOSFET structure. Active layer, gate oxide, and poly-gate thickness are 50, 26, and 150 nm, respectively. (c) One of the channel cross-sectional view of (a), BB′ direction, as a tri-gate structure.

to form a sidewall spacer that abutted the polysilicon gate. Then, the self-aligned source and drain regions were formed by the implantation of phosphorous ions at a dose of 5×10^{15} cm^{-2}. The dopant was activated by rapid thermal annealing at 1000 °C. After source and drain (S/D) implantation, a 300-nm-thick TEOS oxide layer was deposited as the passivation layer by LPCVD. Next, the contact hole was defined and Al metallization was performed. The devices were then sintered at 400 °C in nitrogen ambient for 30 min. Finally, each device was passivated by NH_3 plasma treatment for 1 h at 300 °C.

III. Results and Discussion

Fig. 3 presents a active region scanning electron microscope (SEM) photograph of the poly-Si M10 TFT, including the gate, source, drain, and ten multiple nanowire channels. The inset SEM photograph presents a magnified area of the ten nanowire channels in the M10 TFT, each of which is 67 nm wide. Fig. 4(a)–(d) plots transfer curves of all poly-Si TFTs. In Fig. 4(a), the single-channel TFT (S1 TFT) shows significant short-channel effect, including DIBL, a large subthreshold slope (SS) of 334 mV/dec, and a large leakage current of 4×10^{-12} A. By comparing all studied TFTs in this brief, however, the transfer characteristics reveal that the M10 TFT performs best, as shown in Fig. 4(d), with the lowest OFF-state leakage current of 3×10^{-13} A, the highest drain current ON/OFF ratio of 7.36×10^{9}, the smallest SS of 137 mV/dec and an absence of DIBL. In addition,

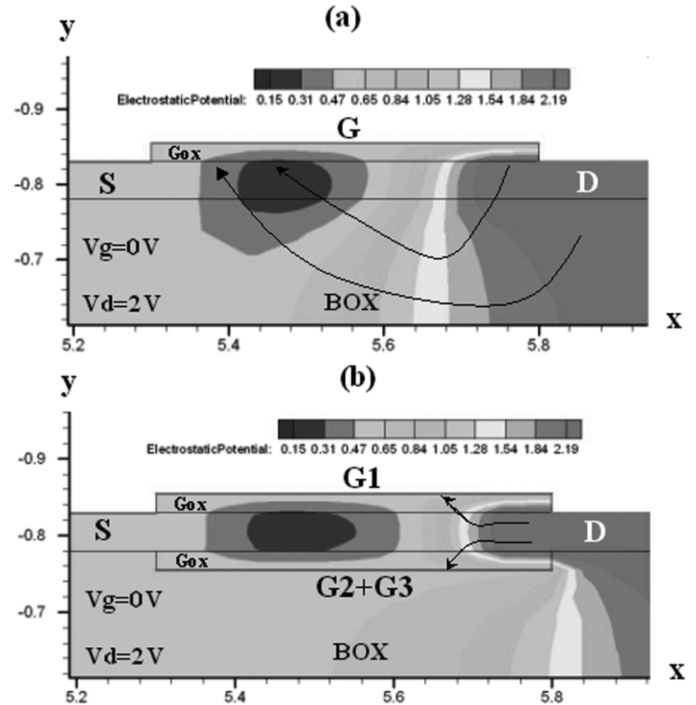

Fig. 2. Simulation results of potential contour plots and electrical field lines of (a) single-top-gate TFT and (b) tri-gate TFT with $L = 0.5$ μm, gate oxide= 26 nm, channel thickness = 50 nm at $V_g = 0$ V, $V_d = 2$ V.

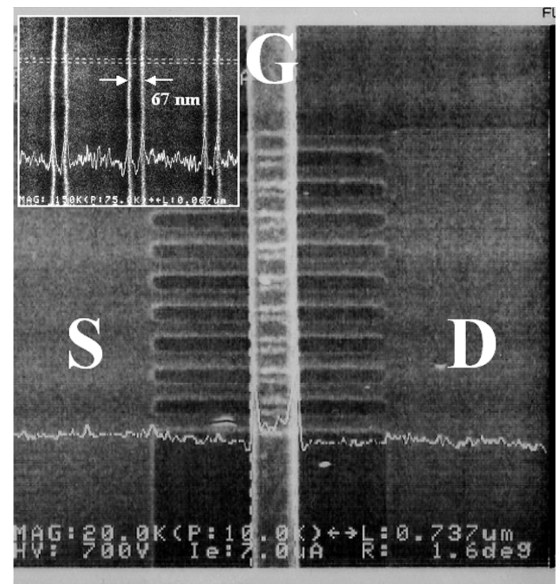

Fig. 3. (a) SEM photograph of active pattern with the gate (with TEOS-SiO_2 spacer), source, drain, and ten nanowire channels of M10 TFT. The inset SEM photograph shows the magnified area of ten nanowire channels. Each nanowire width is 67 nm.

the device performance enhances with the channel width decreasing, from S1, M2, and M5 to M10 TFTs

Device performance uniformity is another important issue for realization of large-glass poly-Si AMLCD. The uniformity of device performance can be revealed by measuring the statistical variation of device parameters. For the investigation of device performance uniformity, in the following discussion, each dimension including five TFTs in different areas on the 6-in wafer were characterized.

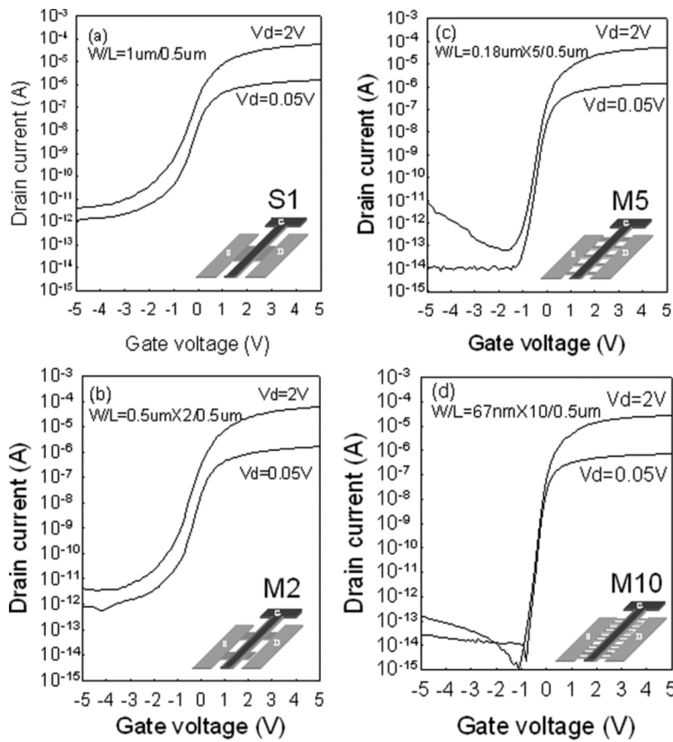

Fig. 4. Device transfer $I_d - V_g$ curves of (a) S1 $(W/L = 1\ \mu\text{m}/0.5\ \mu\text{m})$, (b) M2$(W/L = 0.5\ \mu\text{m} \times 2/0.5\ \mu\text{m})$, (c) M5 $(W/L = 0.18\ \mu\text{m} \times 5/0.5\ \mu\text{m})$, and (d) M10 $(W/L = 67\ \text{nm} \times 10/0.5\ \mu\text{m})$ poly-Si TFT.

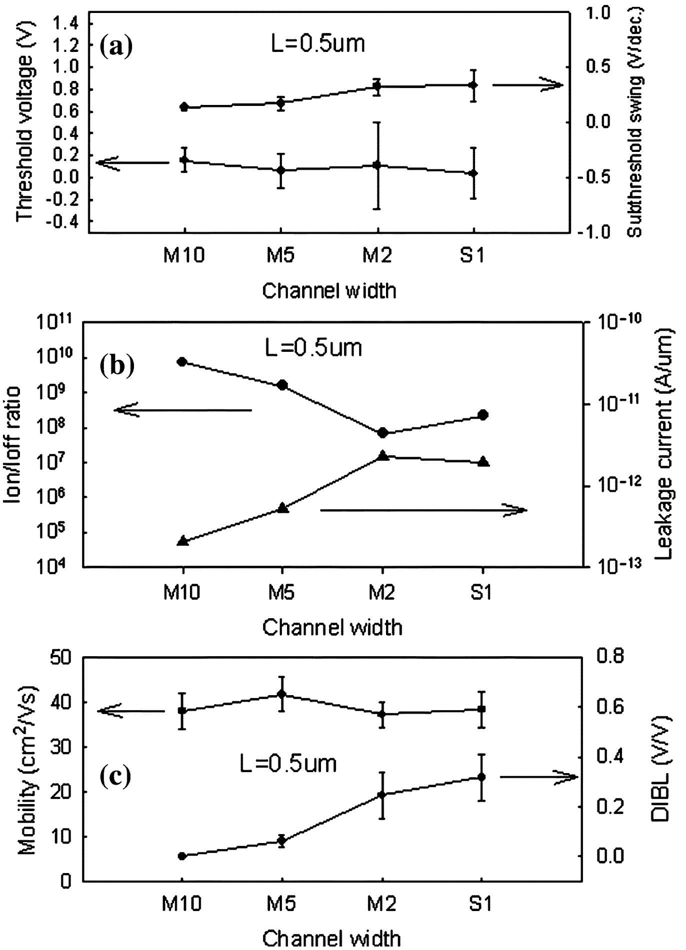

Fig. 5. (a) Threshold voltage (V_{th}) and SS, (b) drain ON/OFF current ratio (R) and drain leakage current, and (c) field-effect mobility (μ_{FE}) and DIBL versus multichannel with different widths poly-Si TFTs. In all plots, the dots value present average and error bars present standard deviation.

Fig. 5(a) plots the TFTs' V_{th} (left) and SS (right) versus the multichannel with different widths. The V_{th} is defined as the gate voltage required to yield normalized drain current of $I_d/(W/L) = 10^{-7}$ A at $V_d = 2$ V. The average V_{th} value for each TFT device is similar and between 0 and 0.2 V, indicating that the channel width does not affect the mobility for the constant current extraction method of V_{th}. Notably, the value of V_{th} for the M10 TFT has the smallest standard deviation, indicating that the M10 TFT is a relatively stable structure in the fabrication and thus involves smaller variations, which in fact is crucial key in the uniform larger-glass AMLCD applications. The average and standard deviation of SS both decrease with the each channel width decreasing. The M10 TFT has a smaller average (137 mV/dec) and standard deviation (23 mV/dec) of SS than those of the other TFTs. The steep SS of the M10 TFT is also explained by the fact that M10 has the robust tri-gate control and exhibits the best NH_3 plasma passivation due to its ten split nanowire, which both are responsible for the steep SS.

Fig. 5(b) plots the TFT's ON/OFF ratio (left) and the leakage current I_{OFF} (right) versus the multichannel with different widths. I_{OFF} is defined as the minimum drain turn-off current at $V_d = 2$ V. Thus, the ON/OFF ratio is defined as maximum $I_{\text{ON}}/I_{\text{OFF}}$. The leakage current is reduced significantly in the OFF-state from 10^{-12} (A/ μm) to 10^{-13} (A/ μ m) in order from the S1 TFT to the M10 TFT. The enhanced performance in electrical characteristics of M10 TFT can be explained that it has a split nanowire structure (Fig. 3), most of which is exposed to NH_3 plasma passivation, further reducing the number of grain boundary defect density (N_t), which is responding for achieving low leakage current. Thus, the M10 TFT has a higher ON/OFF ratio $(> 10^9)$ than those of other TFTs in this brief.

Fig. 5(c) plots the TFT's μ_{FE} (left) and DIBL (right) versus the multichannel with different widths. The μ_{FE} is extracted from the linear region $(V_d = 0.05\ \text{V})$ of transcendence (g_m). DIBL is defined as $\Delta V_g/\Delta V_d$ at $I_d = 10^{-10}$ A. The result reveals that the S1, M2, M5, and M10 poly-Si TFTs yield almost the same carrier mobility, indicating that the carrier mobility and the turn-on current are not degraded in TFTs with various numbers of channels. The DIBL effect leads to a substantial increase in electron injection from the source to the drain associated with penetration electrical field from drain. In Fig. 5(c), the M10 TFT has an average and standard deviation of DIBL of zero. The ten nanowire of M10 TFT are strongly controlled by their tri-gate electrodes [Fig. 1(c)]. The simulation results of Fig. 2(b) further reveal that the tri-gate TFT has superior gate control, which can confine the electrical field penetrated from drain side. Fig. 5 reveals that the M10 TFT performs best in switching applications, with the most stable V_{th} and the smallest SS, and without the DIBL effect. These results are summarized by stating that the active channels around the tri-gate of the M10 TFT exhibit the best gate control to highly reduced short-channel effect, as determined by its nanowire structure. Additionally, experimental results also indicate that the gate control enhances with the each channel width decreasing from S1, M2, and M5 to M10, as similar as the structure changes from a single-gate to tri-gate sequentially. Additionally, NH_3 plasma passivation more efficiently affects M10 TFT than it does other TFTs. Because M10 TFT has a split nanowire structure, most of which is exposed to NH_3 plasma passivation, further reducing the number of grain boundary defects.

IV. Conclusion

This brief studied the relationship between electrical characteristics and channel width dimension in multichannel poly-TFT with nanowire devices. Experimental results indicate that the device performance enhances with the each channel width decreasing, from S1, M2, M5, to M10 TFTs, because their structures vary from single-gate to tri-gate controlled devices gradually. Therefore, M10 TFT exhibits superior and uniform characteristics, including a low leakage current, a high ON/OFF drain current ratio, a steep SS, an absence of DIBL. The fabrication of multichannel TFTs with nanowire is compatible with CMOS technology and involves no additional processes. Such TFTs are thus very promising candidates for use in future high-performance poly-Si TFT applications.

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Nitride-Based Light-Emitting Diodes With p-AlInGaN Surface Layers

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***Abstract*—We have prepared bulk p-AlInGaN layers and light-emitting diodes (LEDs) with p-AlInGaN surface layers by metal–organic chemical vapor deposition. By properly control the TMAl and TMIn flow rates, we could match the lattice constant of p-AlInGaN to that of GaN. It was found that surface of the LED with p-AlInGaN layer was rough with a high density of hexagonal pits. Although the forward voltage of the LED with p-AlInGaN layer was slightly larger, it was found that we can enhance the output power by 54% by using p-AlInGaN surface layer.**

***Index Terms*—InGaN/GaN, light-emitting diode (LED), p-AlInGaN, V-shap pits.**

I. Introduction

Recently, tremendous progress has been achieved in GaN-based blue, green, and ultraviolet (UV) light-emitting diodes (LEDs) [1]–[6]. For example, GaN-based blue and green LEDs have already been extensively used in full-color displays and high efficient light source for traffic light lamps. UV emitters are of interest for fluorescence based chemical sensing, flame detection, and possibly optical storage applications. These nitride-based LEDs are also potentially useful for solid-state lighting. To realize solid state lighting, however, one needs to further improve output efficiency of the nitride-based LEDs.

It is known that external quantum efficiency of LEDs depends on the refractive index and morphology of the top surface layer. Light extraction efficiency of GaN-based LED is limited mainly by the large difference in refractive index between GaN film and the surrounding air. The critical angle for photons to escape from GaN film is determined by Snell's law. This angle is crucially important for the light extraction efficiency of LEDs. Since the refractive indexes of GaN and the air are 2.5 and 1, respectively, external quantum efficiency was limited to only a few percents for conventional GaN-based LEDs. Although it is not possible to change the GaN refractive index, it has been shown that one can enhance light output by roughening the GaN sample surface. With a rough surface, photons generated in the active layer will have multiple opportunities to find the escape cone [7]–[10]. Angular randomization of photons can thus be achieved by surface scattering from the roughened top surface of the LED. In other words, we might be able to enhance the LED output intensity by changing surface morphology of LEDs. Previously, it has been shown that surface morphology of

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