Optimal Design of CMOS Pseudoactive Pixel Sensor (PAPS) Structure for Low-Dark-Current and Large-Array-Size Imager Applications

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***Abstract*—In this paper, a pixel structure called the *optimal pseudoactive pixel sensor* (OPAPS) is proposed and analyzed for the applications of *CMOS imagers*. The shared zero-biased-buffer in the pixel is used to suppress both *dark current* of *photodiode* and leakage current of pixel switches by keeping both biases of photodiode and parasitic *pn junctions* in the pixel bus at zero voltage or near zero voltage. The factor of photocurrent-to-dark-current ratio per pixel area (PDRPA) is defined to characterize the performance of the OPAPS structure. It is found that a zero-biased-buffer shared by four pixels can achieve the highest PDRPA. In addition, the column sampling circuits and output correlated double sampling circuits are also used to suppress fixed-pattern noise, clock feedthrough noise, and channel charge injection. An experimental chip of the proposed OPAPS CMOS imager with the format of 352 $\times$ 288 (CIF) has been designed and fabricated by using 0.25-μm single-poly-five-level-metal (1P5M) N-well CMOS process. In the fabricated CMOS imager, one shared zero-biased-buffer is used for four pixels where the PDRPA is equal to 47.29 μm^{-2}. The fabricated OPAPS CMOS imager has a pixel size of 8.2 $\times$ 8.2 μm, fill factor of 42%, and chip size of 3630 $\times$ 3390 μm. Moreover, the measured maximum frame rate is 30 frames/s and the dark current is 82 pA/cm^2. Additionally, the measured optical dynamic range is 65 dB. It is found that the proposed OPAPS structure has lower dark current and higher optical dynamic range as compared with the active pixel sensor (APS) and the conventional passive pixel sensor (PPS). Thus, the proposed OPAPS structure has high potential for the applications of high-quality and large-array-size CMOS imagers.**

***Index Terms*—CMOS imagers, dark current, optimal pseudoactive pixel sensor (OPAPS), photodiode, pn junctions.**

I. Introduction

CMOS imagers which consist of optical collections of photons (e.g., microlens), wavelength discrimination of photons (e.g., color filter), detectors for conversion of photons to electrons (e.g., a photodiode), timing control, color processing, analog readout circuits [1]–[5], analog-to-digital conversion, and other interface electronics [6], [7] have been used in various applications. Several important factors contribute to the emergence of CMOS imagers at this time rather than 10 to 20 years ago. The primary reason is recent demand for portable, low voltage [8], [9], low power consumption [10], and miniaturized digital image systems. Moreover, the second important reason is that CMOS technology offers a submicron feature size with low defeat and permits cost-effective pixel size [1]. Generally, small pixel size and low dark current are required in the design of high-resolution and high-quality CMOS imagers [1].

Temporal noise is the fundamental limitation on image sensor performance [11]. The dominant source of temporal noise in high illumination is the shot noise that is proportional to the sum of photocurrent and dark current in a photodiode [11]. Large dark current in the photodiode array of a CMOS imager could lead to high noise, nonuniformity, low scalability, and reduced dynamic range. Therefore, reducing dark current in the photodiode also eliminates noise in the CMOS imager.

Dark current is dominantly generated from reverse-biased photodiode and parasitic pn junctions in the pixel. Generally, higher (lower) reverse-biased voltage leads to larger (smaller) dark current. In the conventional active pixel sensor (APS) [1], the dark current is dominantly generated from the photodiode, which is different in every pixel due to both process variations and different reverse-biased voltages of photodiodes caused by different intensity of the incident light on every pixel. Thus, the bias effect of the dark current cannot be reduced even by using the dummy photodiode in the pixel. In the passive pixel sensor (PPS) [1], the dark current is generated from both photodiode and parasitic pn junctions in the column bus. Due to the same reasons, the dark current is also different in every pixel and cannot be reduced.

To design a low-dark-current and high-signal-to-noise-ratio CMOS imager, several techniques have been proposed. Among them, the phototransistor pixel sensor with dark current cancellation [12] is proposed to reduce dark current by using one dummy shielded photodiode in each pixel. However, the total dark current still cannot be effectively cancelled because the reverse-biased voltage between the photodiode and the dummy shielded photodiode is different. In addition, the increased pixel size in this structure may degrade the image resolution and increase cost in the design of imagers with large array size. The structure of differential passive pixel imager with fixed-pattern noise (FPN) reduction [13] is also proposed to cancel dark current. However, it still cannot effectively reduce dark current due to the mismatch between the photodiode in the photodiode array and that in the dummy shielded pixel outside the array.

Another factor in the design of high-resolution and large-array-size CMOS imagers is the requirement of small pixel size.

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The pixel size is small under the same fill factor if the number of devices in the pixel is as small as possible. Recently, the structure of pseudoactive pixel sensor (PAPS) [4] has been proposed to reduce pixel area and lower dark current. However, the dark current generated in the parasitic pn junctions of a column bus is large due to the large number of pixels in the column bus. For example, 288 pixels are connected to the column bus in the CIF design. The large dark current decreases the signal-to-noise ratio (SNR) in the design of high-resolution CMOS imagers.

It is the aim of this paper, to optimize the design of the structure of PAPS for the large-array-size CMOS imagers with low dark current. In the proposed optimal PAPS (OPAPS) structure, a buffer circuit called the zero-biased-buffer direct injection (ZBBDI) is shared by limited number of pixels to keep the photodiodes at zero or near zero bias and readout the selected pixel current [5]. Then the integration of readout current is performed by using an APS-like circuit. A new factor called the photocurrent-to-dark-current ratio per pixel area (PDRPA) is defined and optimized for the OPAPS structure. In the OPAPS design, both column sampling circuit and output correlated double sampling (CDS) circuit are used to reduce FPN, clock feedthrough noise, and the noise from the effect of channel charge injection. The experimental results successfully verified the function of the proposed OPAPS structure and its performance.

In Section II, the new structure of the proposed optimal PAPS (OPAPS) is described and the principles to decrease dark current and optimize the factor of PDRPA are presented. In Section III, chip architecture and simulation results are described. In Section IV, chip layout and experimental results are presented and analyzed. Finally, the conclusion is given.

II. OPAPS

The general structure of the proposed OPAPS with $P+/N$-well photodiode is shown in Fig. 1 where one zero-biased buffer is shared by N pixels and each pixel has a pixel select switch device Mri where $i = 1, 2, \ldots, N$. The gate of Mri is connected to the pixel select signal Ri. Moreover, the cathode of photodiode is connected to the pixel bias voltage of 1.8 V, whereas the anode is connected to the shared zero-biased-buffer through the pixel select switch Mri. The inverting input of a gain stage G1 with the gain A is connected to the pixel bus of node D in Fig. 1 and its noninverting input is connected to the bias voltage Vcom. The output of the gain stage is connected to the gate of Min as a common-gate input stage. In the OPAPS circuit, the gain stage is implemented by a single CMOS differential pair to reduce the chip area.

The use of shared zero-biased-buffer in the OPAPS structure is the same as the buffer-direct-injection (BDI) [14], [15] readout structure. Through the shared zero-biased-buffer, the bias of pixel bus is controlled by the input voltage Vcom of the gain stage G1. The value of Vcom is set to 1.8 V by a low-noise constant voltage source to maintain the voltage of pixel bus at 1.8 V or near 1.8 V. Thus, the effective voltage drop across the photodiode is zero or near zero when the pixel select switch of Mri is on.

The MOSFET of Mrstt and the parasitic capacitor Cp are used to integrate the photocurrent at the node C of Fig. 1. Moreover, the gate control signal of Reset is used to reset the voltage

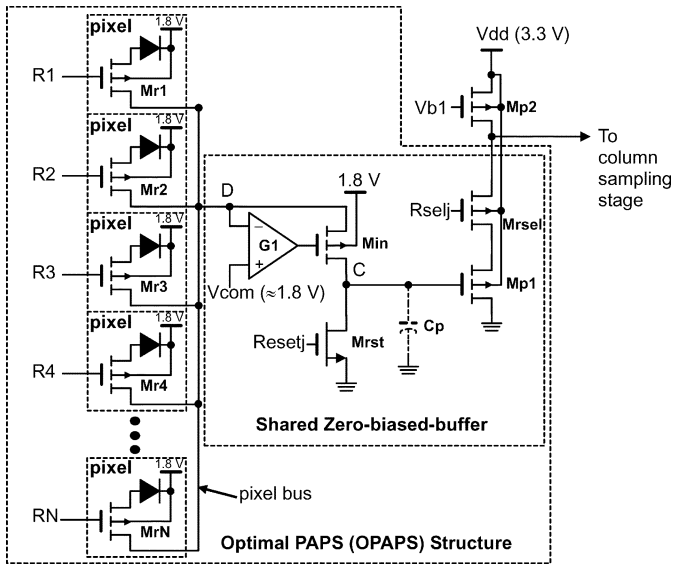

Fig. 1. OPAPS circuit with $P+/N$-well photodiode.

of node C at zero voltage. The source follower, composed of Mp1, Mrsel, and Mp2 is used as a buffer to transfer the voltage at the node C to the column sampling stage without interference. The gate control signal Rselj where $j = 1, 2, \ldots, K$ is used as the row selection. The gate of Mp2 is connected to the biased signal $\mathrm{Vb1}$.

The interconnections of pixels, shared zero-biased-buffers, and column sampling stages in the OPAPS CMOS imager are shown in Fig. 2. The shared zero-biased-buffers are contained in the entire sensor array as shown in Fig. 2. The N pixels connected to the same shared-zero-biased-buffer and controlled by the pixel select switch Ri where $i = 1, 2, \ldots, N$ in one set of OPAPS circuit are put in the same column. K sets of OPAPS circuit controlled by the set select switch Rselj where $j = 1, 2, \ldots, K$ are also put in the same column. Thus, the total number of pixels in the same column of the OPAPS CMOS imager are equal to NK. When both pixel select switch Ri and set select switch of Rselj are on, the image information of pixels in the ith row at the jth set of the OPAPS circuit in all columns are readout to the column sampling stage simultaneously. With both the pixel select switch Ri on and set select switches of Rsel1 to RselK on sequentially, $1/N$ frames of image information are transferred to the column sampling stage. Then the pixel select switch Ri is set to off and the next pixel select switch $\mathrm{Ri}+1$ is on to transfer another $1/N$ frames of image information to the column sampling stage. The readout of the total image is completed after the N transformations of $1/N$ frames.

In additional to maintain the stable bias at the node D of Fig. 1, the input impedance seen from the node D is decreased by a factor of A due to the negative-feedback structure. The injection current from the pixel is mainly drained toward the node D due to the low input impedance. The current injection efficiency of the OPAPS readout structure is expressed as [16]

$$\eta(s) = \frac{(1+A)\, g_{\mathrm{m}}\mathrm{Ro}}{1+(1+A)\, g_{\mathrm{m}}\mathrm{Ro}} \left(\frac{1}{1+\frac{s}{2\pi f_{\mathrm{BW}}}} \right) \tag{1}$$

$$f_{\mathrm{BW}} = \frac{1+(1+A) g_{\mathrm{m}}\mathrm{Ro}}{2\pi \mathrm{Ro} \mathrm{C}_{\mathrm{T}}} \tag{2}$$

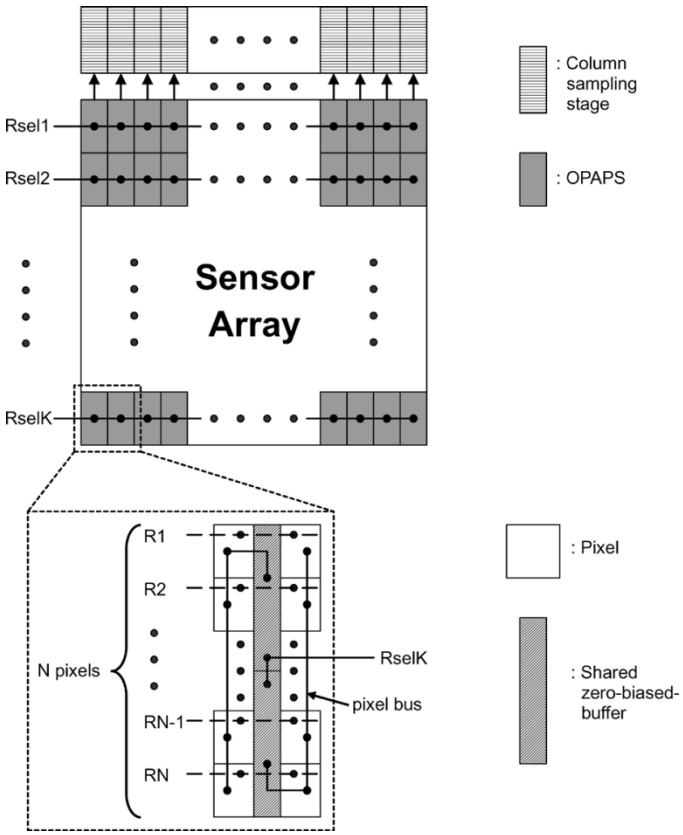

Fig. 2. Interconnections of pixels, shared zero-biased-buffers, and column sampling stages in the OPAPS CMOS imager.

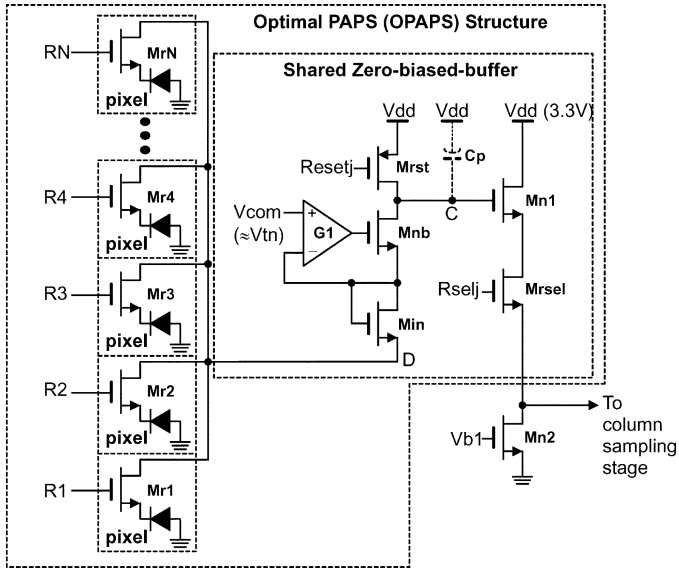

Fig. 3. Modified OPAPS circuit with $N+/P$-substrate photodiode.

where A is the gain of the buffer, g_{m} is the transconductance of Min, C_{T} is the capacitance at the node D, and Ro is the output resistance of Mri. From (1), the current injection efficiency is increased by the gain of the buffer. In this design, the gain of A is about 100, which makes the injection efficiency close to 1.

In order to decrease the pixel area and reduce power dissipation, the use of MOSFETs in the pixel must be minimized. In addition, the power consumption of the shared zero-biased-buffer often becomes intolerable in the large-array-size CMOS imager. To solve the above problems, the same technique in the shared-buffer direct injection (SBDI) [17] is used. Thus, the gain stage in the OPAPS circuit is composed of only one half of the differential pair [17]. The additional power consumption of the gain stage can be reduced by proper design of the gain stage with low bias current. The effective total device number in the OPAPS circuit of Fig. 1 is $(N+7)$ and one pixel is composed of only $(1+7/N)$ MOSFETs.

The OPAPS circuit can be modified for the applications to the $N+/P$-substrate photodiode which has lower dark current and higher quantum efficiency. The modified OPAPS circuit for the $N+/P$-substrate photodiode is shown in Fig. 3 where an extra NMOS device Min is added. In Fig. 3, the modified OPAPS circuit is composed of the buffer-direct-injection (BDI) [14], [15] readout structure, the PMOS transistor Mrst as the reset switch, the APS-like structure with the NMOS source follower $\mathrm{Mn1}$, Mrel, and $\mathrm{Mn2}$, and a parasitic capacitor Cp. The value of Vcom is set to be slightly larger than the threshold voltage Vtn of Min. Thus, the bias at the node D is equal to near zero voltage. The photodiode is biased at zero or near zero voltage when the pixel select switch of Mri is on. The impedance seen from the node D to Vdd is increased by $1/g_{\mathrm{min}}$ where g_{min} is the transconductance of Min. To avoid the degraded injection efficiency, the channel geometric ratio W/L of Min should be large enough to increase g_{min}.

In the N-well CMOS technology, the $P+/N$-well pn junction is used as the photodiode. From the measurement results, it is found that the ratio of the photocurrent i_P to the dark current i_{d} under the reverse bias of 0 V is much larger than that under the reverse bias of 3 V. Thus, biasing the photodiode at zero or near zero voltage can achieve lower dark current, lower shot noise [11], and higher ratio of the photocurrent to the dark current.

From the above results, it is shown that both photodiode and all the parasitic pn junctions in the pixel select switch must be operated under the reverse bias of 0 V to effectively reduce the dark current. Thus, the voltage difference between the cathode of the photodiode and the node D of Fig. 1 is operated at 0 V in the proposed OPAPS structure in order to maintain the zero bias of both photodiode and parasitic pn junctions as shown in Fig. 1. When the pixel select switch of Mri is on, the voltage at the source of Mri is the same as that of node D which is 1.8 V. The photodiode, the parasitic pn junction between the source and substrate of Mri, and the parasitic pn junction between the drain and substrate of Mri are all operated under the reverse-biased voltage of 0 V. The photocurrent is then delivered to the node C for charge integration while both the dark current of the photodiode and the leakage current of the parasitic pn junctions are decreased to near 0 A.

When the pixel select switch of Mri is turned off by setting the signal of Ri at Vdd, the diagram of pixel circuit in OPAPS is shown in Fig. 4. In Fig. 4, the source of Mri, N-well, and the drain of Mri form the parasitic lateral pnp BJT device Q1 with base and collector connected to 1.8 V and pixel bus, respectively, and emitter connected to node A. Moreover, the source of Mri, N-well, and P-substrate form the parasitic vertical pnp BJT device Q2 with the P-substrate collector connected to ground. Under incident light, the photodiode is forward-biased with the voltage drop equal to V_{F} and is operated

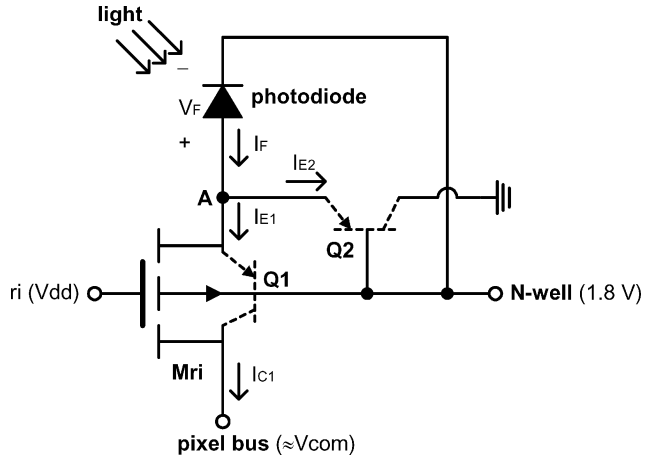

Fig. 4. Diagram of pixel circuit in OPAPS when the pixel select switch of Mri is off.

as a solar cell. With $V_{\rm F}$ as the forward substrate bias between source and body of Mri, the threshold voltage Vtp of Mri is decreased due to the body effect. But the row select switch device Mri is still kept off because the voltage at the node A which is $1.8 + V_{\rm F}$, is smaller than Vdd + Vtp. However, the collector current $i_{\rm C1}$ of Q1 flows into the pixel bus as the dark current. As shown in Fig. 4, the current of $i_{\rm F}$ in the photodiode is equal to the sum of the emitter current $i_{\rm E1}$ of Q1 and $i_{\rm E2}$ of Q2. Thus, we have

$$\begin{aligned} i_{\rm F} &= i_{P1} - i_{\rm SP}(e^{V_{\rm F}/V_{\rm T}} - 1) \\ &= i_{\rm E1} + i_{\rm E2} = i_{\rm S1}(e^{V_{\rm F}/V_{\rm T}} - 1) + i_{\rm S2}(e^{V_{\rm F}/V_{\rm T}} - 1) \end{aligned} \quad (3)$$

where $i_{\rm SP}$, $i_{\rm S1}$, and $i_{\rm S2}$ are the reverse saturation current of photodiode, parasitic lateral BJT device Q1, and parasitic vertical BJT device Q2, i_{P1} represents the photocurrent when the photodiode is biased at 0 V, and $V_{\rm T}$ is the voltage equivalent of temperature. From (3), the total equivalent dark current $i_{\rm TED}$ from the parasitic BJT device Q1 flowing into the pixel bus can be expressed as

$$\begin{aligned} i_{\rm TED} &= (N-1)i_{\rm C1} = (N-1)\alpha i_{\rm E1} \\ &= (N-1)\alpha i_{P1}\frac{i_{\rm S1}}{i_{\rm SP} + i_{\rm S1} + i_{\rm S2}} \\ &= 2.107 \times 10^{-5} \times (N-1) i_{P1} \end{aligned} \quad (4)$$

where N is the number of pixels connected to the same pixel bus and α is the common-base current gain of Q1.

The values of $i_{\rm SP}$, $i_{\rm S1}$, $i_{\rm S2}$, and α in the proposed OPAPS CMOS imager with 0.25-μm CMOS technology and channel width(length) of Mri are given in Table I. From (4), the ratio of $i_{P1}/i_{\rm TED}$ is larger than that of the APS CMOS imager if N is smaller than 2000. Thus, the dark current contributed by the current $i_{\rm TED}$ in the proposed OPAPS CMOS imager is smaller than the dark current of the APS CMOS imager if N is smaller than 2000. Consequently, the proposed OPAPS CMOS imager can be applied to the large-array-size imager with the dark current contributed by $i_{\rm TED}$ in (4) smaller than the dark current of the APS CMOS imager.

The photocurrent generated from the selected pixel is integrated on the node C of Fig. 1 after the reset operation with Mrst off. After the integration, the row select switch signal Rsel is on and the integrated photo-signal voltage is transferred to the photo-signal sampling circuit in the column sampling stage through the source follower. At the end of integration, the reset switch Mrst is turned on and the reset-signal voltage at the node C is also transferred to the reset-signal sampling circuit in the column sampling stage to perform the operation of double delta sampling (DDS) [4].

TABLE I
DATA OF $i_{\rm SP}$, $i_{\rm S1}$, $i_{\rm S2}$, α, AND WIDTH/LENGTH OF Mri

I_{SP}	1.97×10^{-17} A
I_{S1}	4.20×10^{-22} A
I_{S2}	3.02×10^{-20} A
α	0.99
width/length of Mri	0.5 μm / 0.35 μm

TABLE II
DESIGN PARAMETERS OF $i_{\rm d1}$, i_{P1}, $A_{\rm buf}$, $A_{\rm psw}$, $A_{\rm psw,D}$, $A_{\rm psw,S}$, $A_{\rm pd}$, $A_{\rm sp}$, AND $C_{\rm R}$ FOR 0.25-μm 1P5M N-WELL CMOS PROCESS

I_{d1}	0.13fA
I_{p1}	570fA
A_{buf}	65.22 μm^2
A_{psw}	3.6 μm^2
$A_{psw,D}$	0.5 μm^2
$A_{psw,S}$	0.25 μm^2
A_{pd}	28.04 μm^2
A_{sp}	19.30 μm^2
C_R	3.8

In the OPAPS structure, as the number of pixels connected with the same shared-zero-biased-buffer is increased, the total pixel area (TPA) is decreased if the photodiode area is kept constant. However, the PDR is decreased because the dark currents from the deselected pixels are increased. Thus, the optimal number of pixels connected with the shared zero-biased-buffer can be determined from the factor of PDRPA. The TPA in the OPAPS structure is expressed as

$$\text{TPA} = A_{\rm psw} + A_{\rm pd} + A_{\rm sp} + \frac{A_{\rm buf}}{N} \quad (5)$$

where $A_{\rm psw}$ is the area of pixel select switch, $A_{\rm pd}$ is the area of photodiode, $A_{\rm sp}$ is the average area of devices spacing and signal routing channel in a pixel, and $A_{\rm buf}$ is the area of the shared zero-biased-buffer.

The PDR at the node D of Fig. 1 is expressed as

$$\text{PDR} = \frac{i_{P1}A_{\rm pd}}{i_{\rm d1}(A_{\rm pd} + C_{\rm R}A_{\rm psw,S} + C_{\rm R}NA_{\rm psw,D}) + i_{\rm TED}A_{\rm pd}} \quad (6)$$

where i_{P1} and $i_{\rm d1}$ are the photocurrent and dark current per unit area in photodiode, respectively, when it is biased at zero voltage, $i_{\rm TED}$ is the total equivalent dark current from the parasitic BJT device Q1 in Fig. 4 flowing into node D of Fig. 1, $C_{\rm R}$ is the dark-current ratio of the parasitic pn junctions between the source/drain and substrate of Mri in Fig. 1 and photodiode under the same area, $A_{\rm psw,S}$ is the source area of Mri, and $A_{\rm psw,D}$ is the drain area of Mri.

All the values of these parameters in 0.25 μm CMOS technology are listed in Table II where the photodiode area is 28.04 μm^2 which is nearly equal to that in a conventional APS

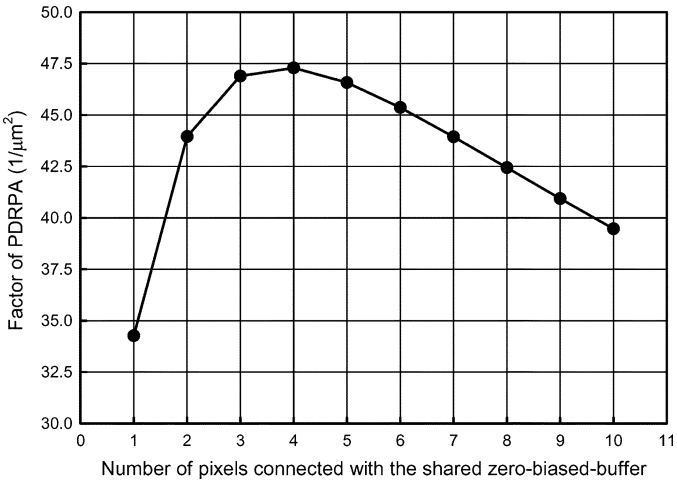

Fig. 5. Factor of PDRPA in the OPAPS circuit.

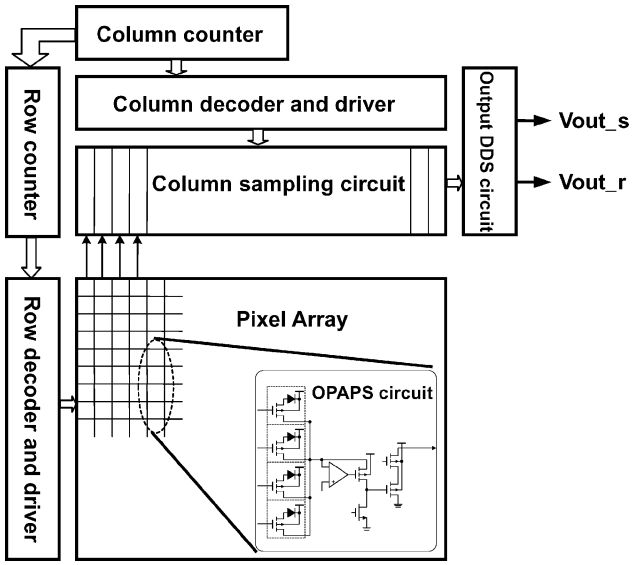

Fig. 6. Block diagram of the OPAPS CMOS imager.

pixels of 8.5 × 8.5 μm. Using the parameter values, the factor of PDRPA can be rewritten as

$$\mathrm{PDRPA} = \frac{\mathrm{PDR}}{\mathrm{TPA}} = \frac{280\,400}{(50.94 + \frac{65.22}{N})(64.54 + 5.91N)}. \quad (7)$$

The calculated values of the factor PDRPA in (7) versus N is shown in Fig. 5. As shown in Fig. 5, the factor of PDRPA has the maximum value when the value of N is equal to 4. Thus, the optimized number of pixels connected with the shared zero-biased-buffer in the OPAPS structure is equal to 4 and the optimized factor of PDRPA is equal to 47.29 $\mu\mathrm{m}^{-2}$. Under this circumstance, the factor of PDR in the OPAPS structure is equal to 3179.86 which is much larger than that of APS.

For different CMOS technologies, the optimal N value may not be equal to 4. It can be calculated by using (5) and (6) to generate the maximum value of PDRPA.

III. Chip Architecture and Simulation Results

The block diagram of the proposed optimal OPAPS CMOS imager is shown in Fig. 6 where $N = 4$, i.e., four pixels share the same zero-biased-buffer. The 352 × 288 (CIF) format of CMOS

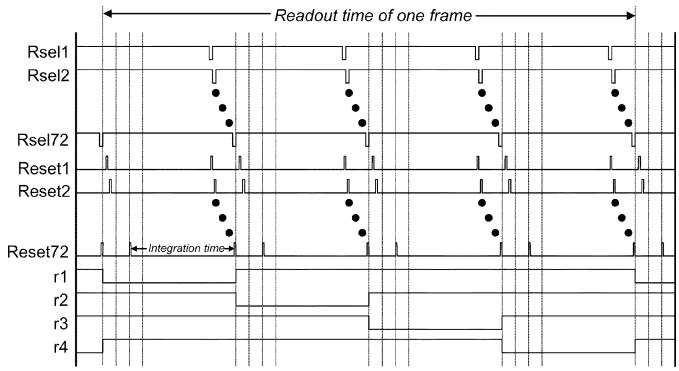

Fig. 7. Major timing diagram of the OPAPS circuit.

imager is taken as an example to realize the proposed OPAPS structure. As shown in Fig. 6, the proposed OPAPS circuit is composed of four pixels and one shared zero-biased-buffer. The row decoder and row counter on the left side of pixel array are used to generate the control signals to the row switches. In addition, the column decoder and column counter on the top side of pixel array are used to generate the control signals for the reset operation and those to the column switches, the output correlated double sampling (DDS) circuit, and the row counter. Each column of the pixel array has a column sampling circuit to reduce FPN. The column readout circuit generates two analog output voltages. One is the signal proportional to the gray scale intensity of the image whereas the other is the signal proportional to the reset voltage at the integration capacitor. The output DDS circuit is used to drive the external loads and perform the DDS operation.

The photo-signal and reset-signal are used for the operation of DDS. The two signals generated in the output DDS circuit are delivered to the programmable gain amplifier (PGA), A/D converter, and display system outside the chip to generate the raw image.

The major operational timing diagram of the proposed OPAPS circuit is shown in Fig. 7. At first, the pixel select switch of r1 is low and the photocurrent of this pixel is integrated on the node C of Fig. 1 after the reset operation at the node C. After the photocurrent integration, the row select switches of Rsel1 to Rsel72 are on sequentially to transfer 1/4 frames of image information to the column sampling stage. Then the pixel select switch of r1 is switched off and the next pixel select switch of r2 is switched on to transfer another 1/4 frames of image information to column sampling stage. The readout of the total image is completed after the four transformations of 1/4 frames.

The HSPICE simulation results of the voltage at node C of the OPAPS circuit in Fig. 1 and the voltage difference between Vout_r and Vout_s of the output DDS circuit in Fig. 6 for the input photocurrent from 200 to 800 fA under the frame rate of 30 frames/s are shown in Fig. 8(a) and (b), respectively. As may be seen from Fig. 8, the linearity of the readout circuit is 92% and the maximum output swing is 0.9 V. The 0.25-μm 1P5M CMOS technology used in the design of the imager chip has the mask of deep N-well beneath the P-well. In other words, the potential of the P-well at the top of deep N-well can be set to any value. Thus, the substrates of NMOSFETs can be connected to their

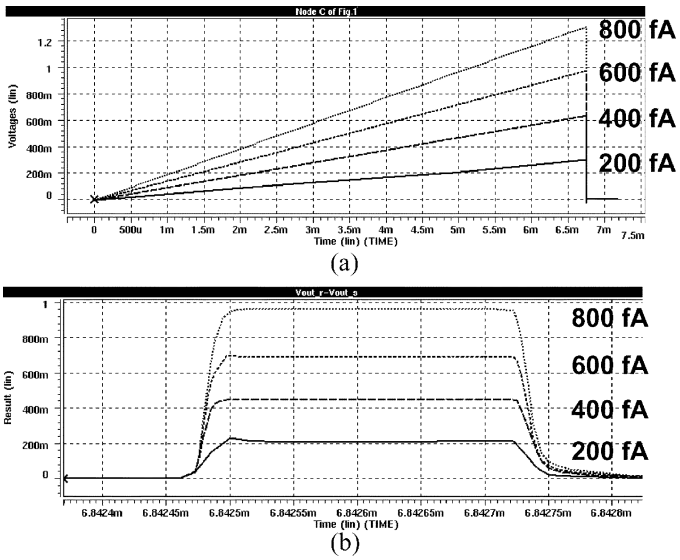

Fig. 8. HSPICE simulation results of (a) the voltage at node C of Fig. 1 and (b) the voltage difference between Vout_r and Vout_s of Fig. 6 for the input photocurrent from 200 fA to 800 fA.

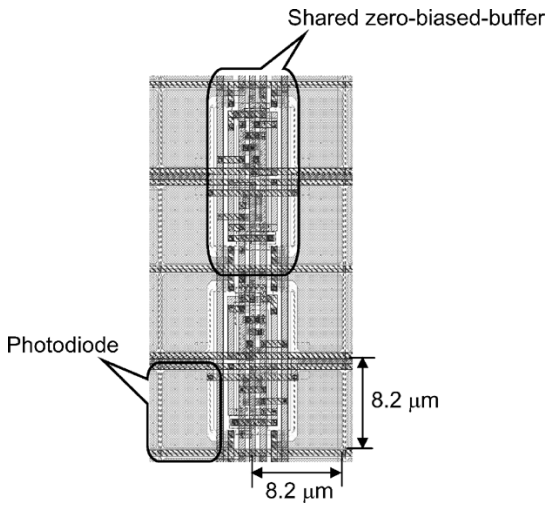

Fig. 9. Layout of eight pixels in the OPAPS CMOS imager chip.

source and the gain in the NMOS source follower is not attenuated by the body effect. Thus, the linearity of the readout chip will be improved by using the NMOS source follower without the body effect.

IV. Experimental Results

In the experimental chip, a 352×288 (CIF) CMOS imager based on the proposed OPAPS structure is designed and fabricated by using 0.25 μm 1P5M N-well CMOS process. The pixel size is 8.2×8.2 μm. The layout diagram of eight pixels in two OPAPS circuits is shown in Fig. 9 where the source of pixel select transistor is connected directly to the P+ diffusion of the photodiode without contacts to increase sensor area and fill factor. The corner of the photodiode is clipped 135° to reduce the effect of leakage current at the right angle. The fill factor in the OPAPS pixel is 42%. The fill factor can be designed larger by moving the N-well contact outside the pixel.

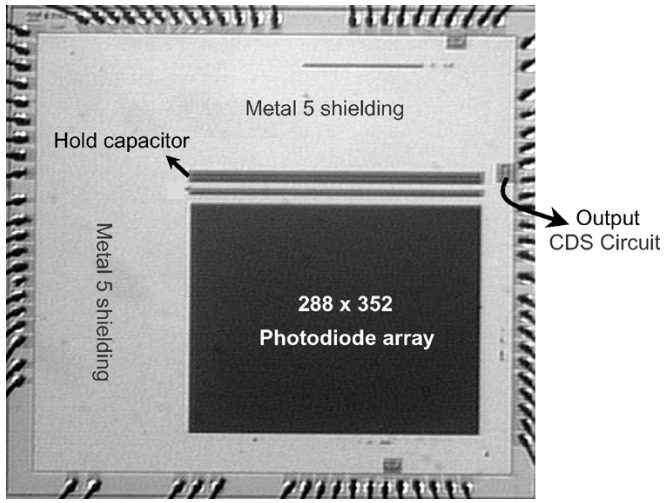

Fig. 10. Die photograph of the test chip.

Fig. 11. (a) Original image and (b) grayscale image captured by the test chip under Vcom of 1.79 V.

To obtain the uniform characteristics of the sensor array, two layers of dummy photodiodes are added around the active sensor array. The P+ regions of the dummy photodiodes are connected to N-well to maintain zero bias such as the photodiodes in the active sensor array. The dummy photodiodes are completely shielded by metal5. In addition, double guard rings are inserted around the sensor cell array to reduce substrate coupling of the digital switching noise.

The analog-to-digital converter is not implemented to simplify the design in the test chip. The photograph of the fabricated imager chip is shown in Fig. 10 where the area except the regions of sensor and capacitor are covered by metal5 for light shielding. The total chip size is 3630×3300 μm.

To test the fabricated CIF OPAPS CMOS imager chip, a data acquisition card with the function of A/D converter is utilized to capture the image. The original image and the measured grayscale image captured by the fabricated CIF OPAPS CMOS imager chip under Vcom of 1.79 V is shown in Fig. 11. Moreover, the measured raw images captured by the fabricated CIF OPAPS CMOS imager chip under different values of Vcom are shown in Fig. 12(a)–(d). When the value of Vcom is 1.79 V, the image quality in Fig. 12(a) is good and no observable fixed-pattern noise (FPN) is presented. With the decrease of Vcom from 1.79 to 1.35 V, as shown in Fig. 12(b)–(d), the image quality is degraded by the effect of leakage current in the parasitic pn junctions of the deselected row switches.

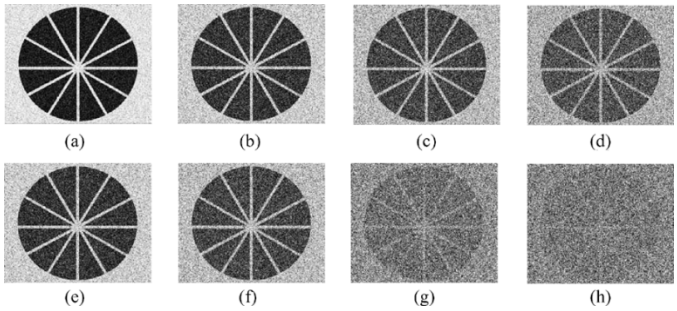

Fig. 12. Images captured by the test chip of OPAPS structure under the integration time of 6.5 msec and Vcom of (a) 1.79 V, (b) 1.65 V, (c) 1.50 V, and (d) 1.35 V and those captured by the test chip of PAPS structure under Vcom of (e) 1.79 V, (f) 1.65 V, (g) 1.50 V, and (h) 1.35 V.

TABLE III
MEASUREMENT RESULTS OF THE PROPOSED OPAPS CMOS IMAGER WITH THE VALUE OF Vcom EQUAL TO 1.79 V AND ITS COMPARISONS WITH THAT OF PAPS [4] AND APS CMOS IMAGER [18]

Pixel Structure	OPAPS	PAPS [4]	APS [18]
Technology	0.25 μm 1P5M N-well CMOS	0.25 μm 1P5M N-well CMOS	0.35 μm 1P3M N-well CMOS
Power Supply	3.3 V	3.3 V	3.3 V
Output Swing	0.9 V	1.2 V	0.8 V (estimate)
Readout Speed	30 frames/sec	30 frames/sec	30 frames/sec
Linearity	92%	92%	80% (estimate)
Dark Current	82 pA/cm^2 (room temperature)	93 pA/cm^2 (room temperature)	370 pA/cm^2 (room temperature)
Optical Dynamic Range	65dB	72dB	53dB
Sensitivity	0.25 V/lux·s (monochrome)	0.16 V/lux·s	0.52 V/lux·s
Fixed Pattern Noise (FPN)	6.2 mV (peak-to-peak)	5.3 mV (peak-to-peak)	8 ~ 24 mV (estimate)
Chip Size	3630 μm x 3390 μm	3660 μm x 3500 μm	5840 μm x 5010 μm
Pixel Size	8.2 μm x 8.2 μm	5.8 μm x 5.8 μm	7.4 μm x 7.4 μm
Array Size	352 x 288 (CIF)	352 x 288 (CIF)	640 x 480
Fill Factor	42%	58%	25% ~ 40% (estimate)
Operating Temperature	25°C	25°C	25°C
Power Dissipation	30 mW	24 mW	31 mW

The images captured by the fabricated CIF PAPS CMOS imager chip [14] under different values of Vcom are also shown in Fig. 12(e)–(h). Comparing the images of Fig. 12(a)–(d) to the corresponding images of Fig. 12(e)–(h), respectively, it can be realized that the OPAPS structure has smaller dark current than that of PAPS structure because the leakage current from the parasitic pn junctions of deselected pixels in the OPAPS structure is smaller than that in the PAPS structure. Thus, the function of the proposed OPAPS CMOS imager is successfully verified. It can be used in the high-resolution applications by keeping the value of Vcom equal to 1.8 V or slightly smaller than 1.8 V.

The measurement results of the proposed CIF OPAPS CMOS imager with the value of Vcom equal to 1.79 V are summarized in Table III, where the corresponding measurement results of the PAPS [4] and APS [18] CMOS imager are also given for comparisons. The dark current in the OPAPS CMOS imager is equal to 82 pA/cm^2 which is smaller than that of the PAPS [4], APS [18], [19], and PPS CMOS imager. In addition, the optical dynamic range of 65 dB in the OPAPS CMOS imager is larger than that of the APS [18], [19] and PPS CMOS imagers because the dark current in the OPAPS structure is the smallest.

The sensitivity of 0.25 $V/\text{lux}\cdot\text{s}$ under the monochrome light source in the OPAPS CMOS imager is smaller than that of the APS and PPS CMOS imagers due to the low quantum efficiency of $P+/N$-well photodiode. To achieve the same sensitivity and quantum efficiency as that of the APS and PPS CMOS imagers, the OPAPS circuit can be modified for the applications to the $N+/P$-substrate photodiode as shown in Fig. 3. FPN caused by device mismatch and process variation was evaluated using a dark image created by averaging 100 frames [19]. There are two sources of FPN, namely, pixel FPN, which is caused by mismatch in the pixel circuit, and column FPN, caused by mismatch in the column readout circuit [20]. The FPN in the OPAPS CMOS imager is 6.2 mV (peak-to-peak) which is smaller than that of the APS CMOS imager with DDS circuits [20]. But the FPN in the OPAPS CMOS imager is slightly larger than that of the PAPS CMOS imager due to the larger pixel FPN in OPAPS CMOS imager. This is because the shared zero-biased-buffers in the OPAPS CMOS imager are put in the sensor array and the mismatches among them increase the pixel FPN. In the PAPS CMOS imager, only one shared zero-biased-buffer is used per column and is put outside the sensor array. However, the FPN of both OPAPS and PAPS CMOS imagers is smaller than that of the APS CMOS imagers with DDS circuits [20]. The total power dissipation of the fabricated CMOS imager chip is equal to 30 mW under the power supply of 3.3 V.

V. CONCLUSION

A pixel structure called the optimal OPAPS structure, has been proposed and analyzed for the applications of CMOS imagers. In the OPAPS structure, the zero-biased buffer is shared by several pixels to increase fill factor, suppress dark current of photodiodes, and decrease the leakage current of parasitic pn junctions. The factor of PDRPA is defined and optimized in the OPAPS structure. It is found that one zero-biased-buffer shared by four pixels in 0.25-μm 1P5M N-well CMOS technology can achieve the maximum PDRPA factor and, thus, represents the best choice. The available integration time is divided by four for a fixed frame rate. In imagers with the OPAPS structure, the DDS circuits are also used to suppress FPN, clock feedthrough noise, and channel charge injection. An experimental chip of CIF OPAPS CMOS imager is designed, fabricated, and measured. The measurement results have verified the performance of the proposed OPAPS structure. Thus, the proposed OPAPS CMOS imager can be used in low-dark-current and high-resolution imager applications by keeping the value of Vcom equal to 1.8 V or slightly smaller than 1.8 V.

It has been found from the experimental results that dark current of 82 pA/cm^2 and optical dynamic range of 65 dB in the fabricated CIF OPAPS CMOS imager are superior than those of the APS and PPS CMOS imagers. In addition, the number of transistors in the pixel of the OPAPS CMOS imager is smaller than that of the APS CMOS imager. With the advantageous characteristics of low dark current, high dynamic range, and high fill factor, it is expected that the proposed OPAPS CMOS imager structure can be applied to the design of high-quality and large-array-size CMOS imagers.

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