Single-Loop Current Sensorless Control for Single-Phase Boost-Type SMR

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***Abstract*—In this paper, the first single-loop current sensorless control (SLCSC) in continuous current mode (CCM) for single-phase boost-type switching-mode rectifiers (SMRs) is developed and digitally implemented in a DSP-based system. Compared to the conventional multiloop control with one inner current loop and one outer voltage loop, there is only one voltage loop in the proposed SLCSC, where the voltage loop's output is used to shift the nominal duty ratio pattern generated from the sensed input and output voltages. Because of no current loop, the efforts of sampling and tracking inductor current can be saved. It implies that the proposed SLCSC is simple and very adaptable to the implementation with mixed-signal ICs. First, the effects of shifting nominal duty ratio pattern on the input current waveform are analyzed and modeled by considering the inductor resistance and conduction voltages. The result of analysis shows that the pure sinusoidal current can be inherently generated by the nominal duty ratio pattern where the current amplitude is roughly proportional to the controllable phase of nominal duty ratio pattern. Then, a voltage controller is included to regulate the dc output voltage by tuning this controllable phase. Finally, some simulated and experimental results have been given to demonstrate the performance of the proposed SLCSC.**

***Index Terms*—Power factor correction, sensorless control, switching-mode rectifier (SMR).**

I. Introduction

In DC/DC conversion, we often pay close attention on the performance of output voltage regulation. Alternatively, in the qualified ac/dc conversion, we are interested in the performances of input current shaping and output voltage regulation. The use of a switching-mode rectifier (SMR) [1]–[3] with power factor correction (PFC) function is an effective mean to perform the qualified ac/dc conversion. Boost-type SMRs, as shown in Fig. 1, are the most popular circuit topology among all the others to shape the current waveform for their continuous input current in the boost inductors. However, since there is only one controllable power switch in the boost-type SMR, both desired functions, including input current shaping and output voltage regulation, must be met by adequately turning on and turning off the single switch.

In the conventional multiloop control shown in Fig. 2, the inner loop focuses on input current shaping and the outer loop contributes to voltage regulation. Then, the two cascaded loops work together to yield adequate switching signal to control the single power switch in order to achieve both desired functions. In the implementation of conventional multiloop control, we need to sense three signals including input voltage, output voltage, and input current, and the rate of sampling current set according to the switching frequency is considerably greater than that of sensing input and output voltages.

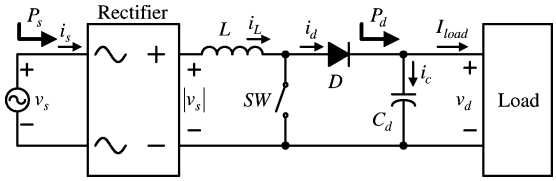

Fig. 1. Power circuit of the boost-type SMR.

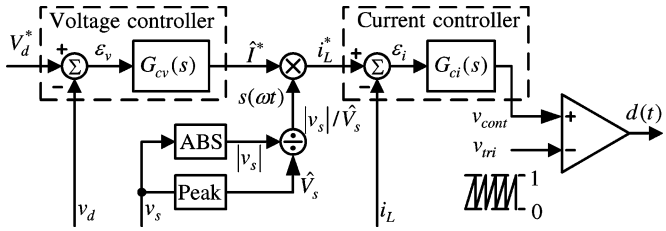

Fig. 2. Conventional multiloop control for boost-type SMRs in CCM.

For single-phase boost-type SMRs, many voltage sensorless controls [4], [5], [7]–[9] and current sensorless controls [6], [7] have been proposed in literatures in order to reduce the total number of input signals. From the view of control structure, these sensorless control methods [4]–[9] can be divided into two categories: one is multiloop sensorless control [4]–[6] and the other is single-loop sensorless control [7]–[9]. Since there is only one voltage loop in the latter category, they can be seen as voltage-mode control, and therefore, the former category can be regarded as current-mode sensorless control for their inner current loop. All the sensorless control methods are summarized in Table I.

In a boost-type SMR, the rising rate of current is proportional to the input voltage, and the falling rate is proportional to voltage difference between the output voltage and the input voltage. The earlier relations are used in the multiloop sensorless control methods [4]–[6], where the input voltage in [4] is reconstructed from the rising rate of inductor current, and the output voltage in [4] and [5] are estimated from the falling rate of the available inductor current. Alternately, the current is predicted from the sensed input and output voltages in [6].

It is noted that at least two current samplings within the durations of rising current or falling current must be obtained in order to calculate the time rate of change of current in [4] and [5].

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TABLE I
SUMMARIZED RESULT FOR VARIOUS SENSORLESS CONTROL [4]–[9]

		[4]	[5]	[6]	[7]	[8]	[9]	Proposed SLCSC
Sensorless Control	Multi-Loop (Current-Mode)	√	√	√				
	Single-Loop (Voltage-Mode)				√	√	√	√
Current Waveform	CCM	√	√	√		√	√	√
	DCM				√			
Input Voltage Sensorless		√			√	√	√	
Output Voltage Sensorless		√	√					
Current Sensorless				√	√			√

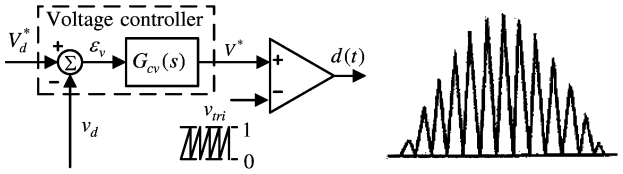

Fig. 3. Conventional voltage-mode control for boost-type SMRs in DCM.

In the multiloop current sensorless control in [6], the rate of sampling input and output voltages must be increased to the level of switching frequency in order to predict the current accurately [6]. It implies that the actual sensing effort does not decrease but increases as the developed sensorless method in [4]–[6]. Therefore, the implementation of multiloop sensorless control is more complex than that of the conventional multiloop control. In addition, the value accuracy of inductance has a great effect upon the performances of multiloop sensorless control in [4]–[6] for that they are based on the inductive relation between the inductor current and inductor voltage.

The control techniques in [7]–[9] are the group of single-loop sensorless controls. The commonly used voltage-follower control illustrated in Fig. 3 can be seen as the first single-loop sensorless control, where the single switch is directly controlled by comparing the output of voltage loop with the carrier signal [7]. Though the discontinuous current is rich in harmonics and far from the pure sinusoidal waveform, the simple voltage-follower control in Fig. 3 is able to meet some standards, and is usually used in many low-power applications.

Both the nonlinear carrier control in [8] and the average current-mode control in [9] are the other single-loop sensorless controls without sensing input voltage. The amplitudes of the nonlinear carrier signal [8] and the triangle carrier signal [9] are adjusted by the output of the single voltage loop. Then, their switching signals are generated from the result of comparison between the sensing current and the adjustable carrier signal. However, although there is no current loop in [8] and [9], the currents are still feedback, and the SMRs are operating under continuous current mode (CCM). However, for single-loop control structure, there is no current sensorless control till now. In this paper, the author develops the first single-loop current sensorless control (SLCSC) in CCM.

The paper is organized as follows. Initially, the effect of phase of the control signal on input current is analyzed and modeled. The results show that the sinusoidal current waveform can be automatically generated by the nominal duty ratio pattern, and the input current amplitude is roughly proportional to its adjustable phase. Subsequently, based on the effect of phase on the input current amplitude, the voltage loop is included in SLCSC to regulate the dc output voltage by means of tuning the phase. Finally, some simulated and experimental results have been given to illustrate the performances of the proposed SLCSC.

II. BOOST-TYPE SMR

As shown in Fig. 1, the power circuit of the boost-type SMR mainly consists of a diode bridge rectifier and a boost-type dc/dc converter. From the circuit topology shown in Fig. 1, we can find that when input voltage v_s is positive, inductor current i_L is equal to input current i_s, and that the inductor current i_L is equal to the negative input current $-i_s$ when the input voltage v_s turns to negative. Then, the inductor current can be represented in terms of input current [10]

$$i_L(t) = \text{sign}(v_s(t))i_s(t) \tag{1}$$

where sign(•) is the sign operator and

$$\text{sign}(X) = \begin{cases} +1, & \text{when } X \geq 0 \\ -z, & \text{when } X < 0. \end{cases} \tag{2}$$

In order to model the behaviors of the boost-type SMR, the following assumptions are made initially.

1) Power switch SW is assumed to operate at a switching much higher than the input frequency. Thus, the input voltage over one switching period can be considered as constant.
2) A bulk capacitor C_d is included in the power circuit, and thus, the output voltage v_d can be assumed to be its average value V_d. Therefore, in steady state, the output voltage v_d can be assumed to be the voltage command V_d^*.
3) Without loss of generality, the input voltage is assumed to be $v_s(t) = \hat{V}_s \sin(\omega t)$, where $\hat{V}_s$ is the magnitude of input voltage.
4) When the boost-type SMR is operating in CCM with unity power factor, the input current must be sinusoidal waveform, and thus, the input current can be assumed to be $i_s(t) = \hat{I}_s \sin(\omega t)$, where $\hat{I}_s$ is the magnitude of the input current.

Therefore, the drawn input power $P_s(t)$ can be expressed as the product of input current $i_s(t) = \hat{I}_s \sin(\omega t)$ and input voltage $v_s(t) = \hat{V}_s \sin(\omega t)$

$$P_s(t) = 0.5\hat{V}_s\hat{I}_s - 0.5\hat{V}_s\hat{I}_s \cos(2\omega t) = \bar{P} - \bar{P}\cos(2\omega t) \tag{3}$$

where $\bar{P} = 0.5\hat{V}_s\hat{I}_s$ is the average power into the SMR.

For the balance between input and output powers, we are able to adjust the output power to regulate output voltage by controlling the magnitude of sinusoidal current $\hat{I}_s$. In the conventional multiloop control shown in Fig. 2, the sinusoidal current is yielded through the cooperation of the outer voltage loop and the inner current loop. First, the input current amplitude $\hat{I}_s$

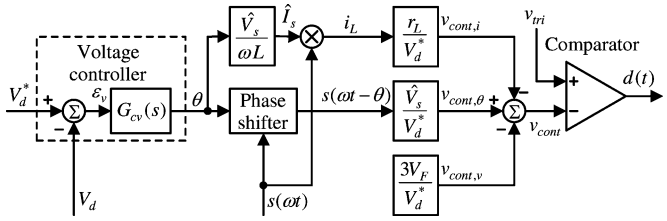

Fig. 4. Proposed SLCSC for boost-type SMRs.

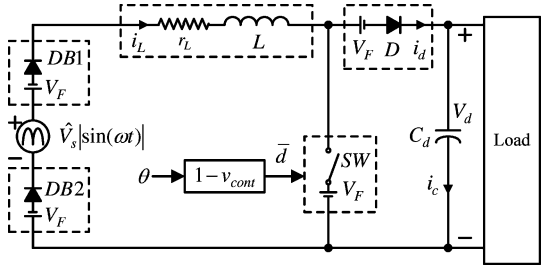

Fig. 5. Boost-type SMR with adjustable phase signal θ.

can be obtained through the outer voltage controller in order to regulate the output voltage. By multiplying $\hat{I}_s$ with the unity rectified signal $s(\omega t) = |\sin \omega t|$, the inductor current command i_L^* can be obtained. Then, the switching signal $d(t)$ in Fig. 2 is generated by comparing the current controller output signal $v_{\rm cont}$ and triangular signal $v_{\rm tri}$ at the comparator's (+) terminal and (−) terminal, respectively.

Alternately, we can find that in the following proposed SLCSC, the input sinusoidal current can be yielded automatically by the single voltage loop without inner current loop and sensing any current.

III. Single-Loop Current Sensorless Control

A. Configuration

The configuration of the proposed SLCSC with only one voltage loop is plotted in Fig. 4. Like the conventional controls plotted in Figs. 2 and 3, the duty signal $d(t)$ of SLCSC is also generated from the comparison between the fixed triangle signal $v_{\rm tri}$ and the control signal $v_{\rm cont}$. However, note that the control signal $v_{\rm cont}$ of SLCSC is at (−) terminal, and the fixed triangle signal $v_{\rm tri}$ is at (+) terminal. Besides, compared with the current magnitude $\hat{I}_s$ at the output of voltage controller in Fig. 2, the output of voltage controller in the proposed SLCSC is the controllable phase θ. And the unity rectified signal $s(\omega t)$ is

$$s(\omega t) = \frac{|v_s(t)|}{\hat{V}_s} = |\sin(\omega t)| = \text{sign}(\sin(\omega t))\sin(\omega t). \quad (4)$$

The control signal $v_{\rm cont}$ in SLCSC is composed of three signals, and can be expressed as

$$v_{\rm cont} = v_{{\rm cont},\theta} - v_{{\rm cont},i} - v_{{\rm cont},v} \quad (5)$$

where

$$v_{{\rm cont},\theta} = \frac{\hat{V}_s}{V_d^*} s(\omega t - \theta) \quad (6)$$

$$v_{{\rm cont},i} = \theta \frac{\hat{V}_s}{\omega L} \frac{r_L}{V_d^*} s(\omega t) \quad (7)$$

$$v_{{\rm cont},v} = \frac{3V_F}{V_d^*} \quad (8)$$

where r_L and V_F are the inductor resistance and diode/switch conduction voltage, respectively.

B. Analysis

In order to simplify the following analysis, all the conduction voltages of the three diodes and the single switch SW are assumed equal to each other and denoted by V_F. By combining the main circuit topology in Fig. 1 and the proposed SLCSC in Fig. 4, we can obtain the equivalent circuit model shown in Fig. 5 for simplified analysis where the diode rectifier is replaced by two series-connected diodes DB1 and DB2, and the input voltage is the ideal rectified sinusoidal voltage $\hat{V}_s|\sin(\omega t)|$.

Since the control signal $v_{\rm cont}$ is at (−) terminal and the triangle signal $v_{\rm tri}$ is at (+) terminal, as shown in Fig. 4, the average duty ratio signal $\bar{d}$ over one switching period T_s can be expressed as

$$\bar{d} = 1 - v_{\rm cont}. \quad (9)$$

By combining (5)–(9), the average duty ratio signal $\bar{d}$ can be further expressed in terms of phase signal θ of the output of voltage controller

$$\bar{d} = 1 - \frac{\hat{V}_s}{V_d^*}|\sin(\omega t - \theta)| + \theta \frac{\hat{V}_s}{\omega L}\frac{r_L}{V_d^*}|\sin(\omega t)| + \frac{3V_F}{V_d^*}. \quad (10)$$

From Fig. 5, when SW is turned on, the current flows through DB1, switch SW, and DB2. Thus, the sum of total conduction voltage drops is equal to $3V_F$. From KVL, the inductor voltage v_L can be expressed as

$$v_L = L\frac{di_L(t)}{dt} = \hat{V}_s|\sin(\omega t)| - 3V_F - i_L(t)r_L, \quad \text{when SW is turning on.} \quad (11)$$

Similarly, when SW is turned off, the current flows through DB1, freewheeling diode *D*, and DB2, and the total conduction voltages is also equal to $3V_F$. The inductor voltage v_L can be found

$$v_L = L\frac{di_L(t)}{dt} = \hat{V}_s|\sin(\omega t)| - V_d^* - 3V_F - i_L(t)r_L, \quad \text{when SW is turned off.} \quad (12)$$

By using the time-averaging approach, the earlier two equations can be combined to obtain the average inductor voltage through multiplying (11) by turning-on time $\bar{d}T_s$ and (12) by turning-off time $(1-\bar{d})T_s$, respectively

$$\bar{v}_L(t) = L\frac{d\bar{i}_L(t)}{dt} = \hat{V}_s|\sin(\omega t)| - (1-\bar{d})V_d^* - 3V_F - \bar{i}_L(t)r_L. \quad (13)$$

Therefore, by substituting the averaged duty ratio signal $\bar{d}$ in (10) into (13) and arranging the terms, we can obtain the following time differential equations for inductor current

$$\bar{v}_L(t) = L\frac{d\bar{i}_L(t)}{dt} = \hat{V}_s|\sin(\omega t)| - \hat{V}_s|\sin(\omega t-\theta)| + \left[\frac{\hat{V}_s\theta}{\omega L}|\sin(\omega t)| - \bar{i}_L(t)\right] r_L \tag{14}$$

where the terms of V_F are canceled out.

Then, the term $\sin(\omega t-\theta)$ can be extracted by applying the following trigonometric identity $\sin(A-B) = \sin A\cos B - \sin B\cos A$, and the approximations $\sin\theta \approx \theta$ and $\cos\theta \approx 1$ if the phase signal θ in radians is small and near to zero ($\theta \approx 0$). Then, (14) can be rewritten as

$$\frac{d\bar{i}_L(t)}{dt} \approx \frac{\hat{V}_s|\sin(\omega t)|}{L} - \frac{\hat{V}_s|\sin(\omega t)-\theta\cos(\omega t)|}{L} + \left[\frac{\hat{V}_s\theta}{\omega L}|\sin(\omega t)| - \bar{i}_L(t)\right]\frac{r_L}{L}. \tag{15}$$

Since the inductor current is repetitive with double line frequency $2f_{\rm in}$, the current differential equation (15) can be simplified by removing the absolute operators [10], and then, the common terms $\hat{V}_s\sin(\omega t)$ can be canceled out

$$\frac{d\bar{i}_L(t)}{dt} \approx \frac{\hat{V}_s\theta}{L}\text{sign}(\sin(\omega t))\cos(\omega t) + \left[\frac{\hat{V}_s\theta}{\omega L}\text{sign}(\sin(\omega t))\sin(\omega t) - \bar{i}_L(t)\right]\frac{r_L}{L}. \tag{16}$$

Then, by solving (16), we can obtain the average inductor current $\bar{i}_L(t)$

$$\bar{i}_L(t) \approx \frac{\hat{V}_s\theta}{\omega L}\text{sign}(\sin(\omega t))\sin(\omega t) = \frac{\hat{V}_s\theta}{\omega L}s(\omega t). \tag{17}$$

From (1), the assumption of the infinite switching frequency, the input current $i_s(t)$ can be expressed as

$$i_s(t) \approx \frac{\hat{V}_s\theta}{\omega L}\sin(\omega t) = \hat{I}_s\sin(\omega t). \tag{18}$$

From (18), obviously, the sinusoidal input current i_s is inherently generated, and its current amplitude $\hat{I}_s = (\hat{V}_s\theta)/(\omega L)$ is proportional to the controllable phase θ without sensing current and current loop. Additionally, the sinusoidal input current i_s is in phase with the input voltage v_s.

By substituting $\hat{I}_s = (\hat{V}_s\theta)/(\omega L)$ into (7), the component $v_{\text{cont},i}$ of the control signal v_{cont} can be expressed as

$$v_{\text{cont},i}(t) = \theta\frac{\hat{V}_s}{\omega L}\frac{r_L}{V_d^*}s(\omega t) = \frac{r_L}{V_d^*}i_L(t) \tag{19}$$

where the rectified signal $v_{\text{cont},i}$ is proportional to the inductor current i_L. From (8) and (19), obviously, the components $v_{\text{cont},i}$ and $v_{\text{cont},v}$ of the control signal v_{cont} can be seen as two feedforward signals used to compensate the effects of voltage drops across the inductor resistance r_L and the conduction voltage V_F, i.e., the component $v_{\text{cont},\theta}$ with fixed wave pattern and controllable phase mainly contributes to the generation of sinusoidal current.

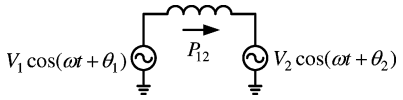

Fig. 6. Basic circuit of power flow in power system

C. Power Flow

Then, by substituting (18) into (3), the average input power becomes

$$\bar{P} = \frac{\hat{V}_s^2\theta}{2\omega L} \propto \theta \tag{20}$$

where the average input power is proportional to the controllable signal θ. It follows that we can include a voltage controller $G_{cv}(s)$ in SLCSC to automatically adjust the phase signal θ to control input power to meet the desired function of output voltage regulation. Consequently, both PFC functions including current shaping and output voltage regulation can be met by using the proposed SLCSC.

Similarly, by substituting $\hat{I}_s = (\hat{V}_s\theta)/(\omega L)$ into (14), the inductor voltage v_L can be expressed as

$$v_L(t) = L\frac{di_L(t)}{dt} = \hat{V}_s|\sin(\omega t)| - \hat{V}_s|\sin(\omega t-\theta)|. \tag{21}$$

Thus, the inductor can be seen as being connected two rectified sinusoidal voltages with identified magnitude but with little phase difference between them, that is analogous to the basic circuit of power flow in the power system. In the basic circuit of power flow, as shown in Fig. 6, two ac voltage sources are interconnected by an inductor. Then, the real power P_{12} and reactive power from the terminal 1 to terminal 2 is

$$P_{12} = \frac{V_1V_2}{2\omega L}\sin(\theta_1-\theta_2) \tag{22}$$

$$Q_{12} = \frac{V_1}{2\omega L}[V_1 - V_2\cos(\theta_1-\theta_2)]. \tag{23}$$

From (21), the idea of the proposed SLCSC can be seen as the special case of the earlier basic circuit, where both amplitudes of two terminal voltages are equal to each other $V_1 = V_2 = \hat{V}_s$ and very little phase difference $\theta_{12} = \theta_1 - \theta_2 \approx 0$ exists between them. Then, the power flow contains near zero reactive power $Q_{12} \approx 0$ and only real power $P_{12} \approx \hat{V}_s^2\theta_{12}/(2\omega L)$ proportional to the little phase difference θ_{12}. Thus, we also obtain the same result in (20).

In summary, by adjusting the little phase difference θ through the voltage controller, we can regulate the flow of real power and maintain near-zero flow of reactive power. Thus, from the point of power flow, the idea of the proposed SLCSC is tuning the phase difference θ between the terminal voltages to yield sinusoidal current in phase with the input voltage and regulate the output voltage.

TABLE II
SIMULATED CIRCUIT PARAMETERS

Input line voltage (peak)	$\hat{V}_s = 155V$ ($110V_{rms}$)
Voltage command	$V_d^* = 300V$
Rated output power	$\overline{P} = 500W$
Input line frequency	$f = 50Hz$
Smoothing capacitance	$C_d = 560\mu F$
Boost inductance	$L = 4.65mH$
ESR of boost inductance	$r_L = 0.9\Omega$
Conduction voltage	$V_F = 0.7V$
Carrier frequency	$f_{tri} = 25kHz$

In (18), we can find that $\hat{I}_s = (\hat{V}_s\theta)/(\omega L)$. Additionally, $\hat{I}_{\rm short}$ is defined as the peak short-circuit current that will flow if the input voltage v_s with amplitude $\hat{V}_s$ was short-circuited through boosting inductance L. It follows that $\hat{I}_s = \theta\hat{I}_{\rm short}$. For given current amplitude $\hat{I}_s$, the interval length φ in which cusp distortion occurs can be determined as follows [3]:

$$\varphi = 2\tan^{-1}\left(\frac{\hat{I}_s}{\hat{I}_{\rm short}}\right) = 2\tan^{-1}(\theta). \tag{24}$$

In normal condition, the circuit parameter should be carefully designed to alleviate the cusp distortion as far as possible. It follows that interval length φ should be kept as small as possible. It implies that the assumptions of small θ and the simplification $\sin\theta \approx \theta$ are reasonable.

IV. SIMULATED RESULTS

In this section, we begin with a series of computer simulations to demonstrate the proposed SLCSC. Some nominal values and circuit elements are listed in Table II. The simple plus-integral (PI) controller is used as the voltage controller in the developed SLCSC to automatically adjust the controllable phase.

A. Steady-State Response

For the circuit parameters in Table II, the simulated waveforms are plotted in Fig. 7, where the enlarged signals $10\times v_{{\rm cont},i}$ and $10\times v_{{\rm cont},v}$ are plotted for the sake of comparison. We can find that the output voltage v_d is well regulated to the voltage command $V_d^* = 300$ V, and the sinusoidal current i_s is in phase with the input voltage v_s. From Fig. 7, the control signal $v_{\rm cont}$ is obviously dominated by the component $v_{{\rm cont},\theta}$ because the voltage v_L across the inductor is much higher than the conduction voltage V_F and the voltage across the inductor resistance r_L. The simulated total current harmonic distortion THD_i in Fig. 7 is about 6.64%.

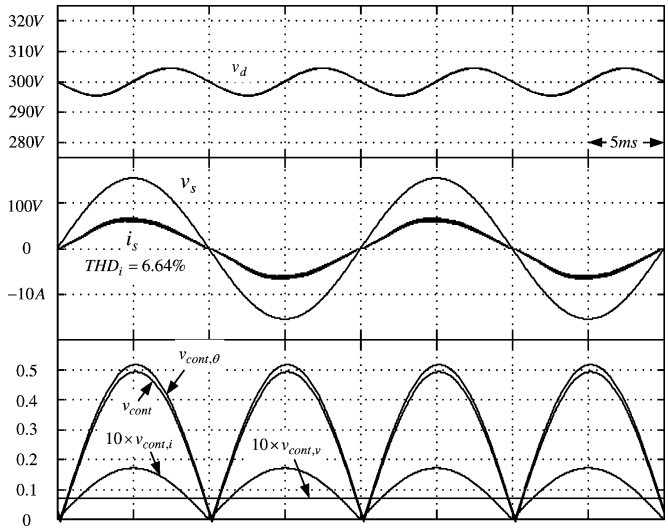

Fig. 7. Simulated steady-state waveforms for the proposed SLCSC

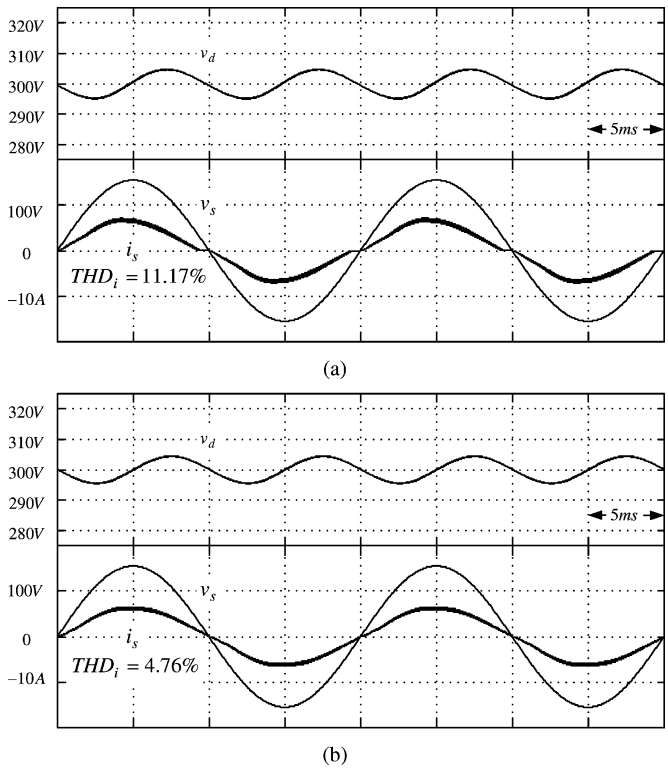

Fig. 8. Simulated steady-state waveforms for the case of inductor (a) with 20% smaller than the nominal value and (b) with 10% larger than the nominal value.

B. Sensitivity—Inductance Parameter

In practice, the inductor value may become 20% smaller due to saturation or 10% larger because of production tolerance. In order to understand the controller performance of parameter variations, the simulated steady-state waveforms for the case of inductor with 20% smaller and 10% larger than the nominal value are plotted in Fig. 8(a) and (b), respectively. Obviously, for the voltage regulation function of PFC, the output voltages v_d in both cases are well regulated to the desired voltage command $V_d^* = 300$ V.

For the case of inductance 20% smaller than the nominal value in Fig. 8(a), the input current i_s is stagnated due to the reduction of the feedforward effect from $v_{{\rm cont},i}$, and thus, the simulated THD_i is increased to near 11.17%. In the other case shown in Fig. 8(b), the amplified feedforward effect of $v_{{\rm cont},i}$

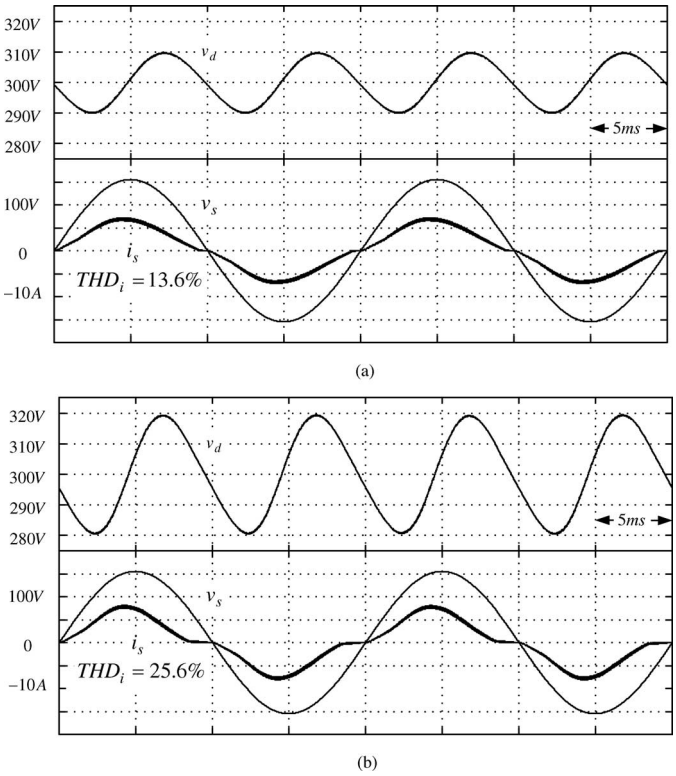

Fig. 9. Simulated waveforms with output capacitance (a) $C_d = 280$ μF and (b) $C_d = 160$ μF.

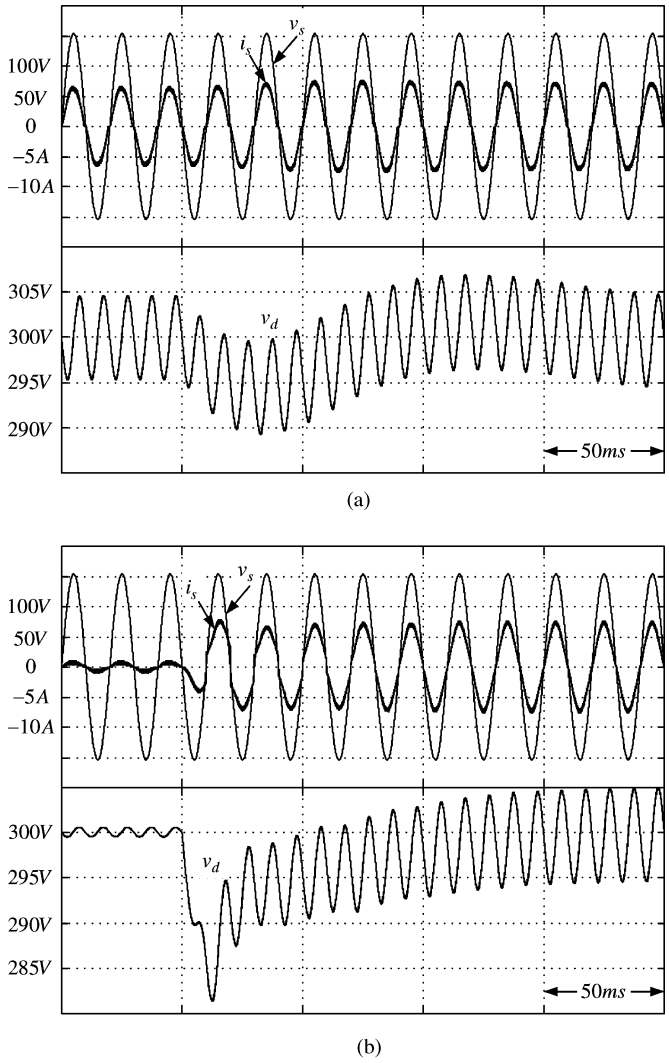

Fig. 10. Simulated waveforms for the proposed SLCSC during load change. (a) From 90% to 100%. (b) From 10% to 100%.

can not only compensate the voltage drop on inductor resistance r_L, but also alleviate the cusp distortion [11]. Consequently, the simulated THD_i decreases to near 4.76% smaller than 6.64% of the nominal case in Fig. 7.

Note that it is not a good idea to continuously increase the inductance to amplify the feedforward effect of $v_{\text{cont},i}$ in order to reduce the current distortion and cusp distortion. The simulated results show that on the contrary, the simulated THD_i would be larger than 6.64% when the inductance is 30% larger than the nominal value.

However, though the inductance variation aggravates the current distortion, the performance of current shaping function is acceptable. Therefore, the PFC performance of the proposed SLCSC is not sensitive to the parameter variations.

C. Sensitivity—Amplitude of Output Voltage Ripple

In the assumption of bulk capacitor C_d, the output voltage v_d is equal to the voltage command V_d^*. However, a bulk capacitor is not permitted in practice due to the considerations of cost and volume. The simulated waveforms for the small output capacitance 280 and 160 μF are plotted in Fig. 9(a) and (b), respectively.

We can find that the amplitude of output voltage ripple increases from ± 5 V, as shown in Fig. 7, to ± 20 V due to the reduction of output capacitances. The earlier the input current returns to zero before the zero-crossing points of input voltage [i.e., the more expansion of discontinuous current mode (DCM) close to the zero-crossing points of input voltage], the more harmonics the input current possesses. Thus, the simulated THD_i increases from 6.64% in Fig. 7 to 13.6% and 25.6% in Fig. 9. However, from the voltage-regulation performance, the output voltages v_d in both cases are well regulated to the desired voltage command $V_d^* = 300$ V. It follows that the sensibility of amplitude of output voltage ripples is acceptable.

D. Transient Response

The simulated load-regulation waveforms for the proposed SLCSC are plotted in Fig. 10(a), when the load resistance R_{load} is suddenly changed from 200 (90% load) to 200 $\Omega \| 1600$ $\Omega = 177.78$ Ω (near 100% load). In order to support sufficient power to regulate the output voltage, the input current magnitude is increased from 6.7 to near 7.3 A by SLCSC. The simulated load-regulation waveforms for the sudden power change from 10% rated load to 100% rated load is plotted in Fig. 10(b), and it shows that the regulation performance is also acceptable. From both cases, we can find that the input current i_s is always in phase with the input voltage v_s even though SMR is under transient

response. Consequently, the proposed SLCSC can keep good performance under the condition of load change.

V. Experimental Results

The proposed SLCSC has been digitally implemented in a DSP-based system using TMS320F240. Only input voltage and output voltage are sensed, where the former provides the phase information of input voltage and the latter helps to regulate the output voltage. The generation of the rectified signal $s(\omega t)$ and the phase shifter in the proposed SLCSC are implemented together by looking up a rectified sine table.

The rectified signal stored in memory is simply synchronized with the input voltage by alignment of individual zero-crossing points. In a system with fixed line frequency, the alignment of zero-crossing points is an effective method to synchronize with input voltage. In order to focus on the function of the proposed CSC, the phase shifter in this paper is implemented by the simplest way, i.e., looking up table with varying address offest. From the experience of implementation, the resolution of lookup table plays an important role in the performances of phase shifter and the proposed control. Too small resolution would result in instable operation.

In the experiment, the digital resolution of phase signal θ is set to 0.00008π rad. For sinusoidal current waveform in SLCSC, the respective digital resolution of input current magnitude $\hat{I}_s$ and average input power are about 0.0267 A and 2.075 W, respectively, corresponding to the digital resolution of phase signal θ. All the circuit parameters in the experimental system have been listed in Table II.

The simple PI-type controller is used in the voltage loop. Its proportional gain is 0.0021 rad/V, and the integral gain is 0.067 rad/V·sec^{-1}.

A. Steady-State Response

Fig. 11 shows the experimental waveforms for the proposed SLCSC at the condition $V^* = 300$ V and $R_{\rm load} = 177.78\ \Omega$. The phase signal θ shown in the middle plot keeps around 0.021π rad·s in order to stably yield enough input power to regulate the output voltage. It is noted that the phase signal $\theta \approx 0.021\pi$ is so small that it is reasonable to use the approximations $\sin\theta \approx \theta$ and $\cos\theta \approx 1$ in the derivation of (15).

The signals $v_{{\rm cont},\theta}$, $v_{{\rm cont},i}$, and the average duty signal $\bar{d}$ are also plotted together to help understanding the operation of the proposed SLCSC. Since signal $v_{{\rm cont},\theta}$ is higher than the signal $v_{{\rm cont},i}$, we can find that average duty signal $\bar{d}$ is dominated by signal $v_{{\rm cont},\theta}$. It follows that the maximum duty ratio is 100%, and minimum duty ratio is about 48% equal to the ratio of input voltage magnitude $\hat{V}_s = 155$ V to the output voltage command $V_d^* = 300$ V. Due to the experimental resolution, the measured total current harmonic distortion THD$_i$ is about 12.56%. However, from the top plot of output voltage v_d and the bottom plots of input current i_s and input voltage v_s, we can find that the proposed SLCSC meets the PFC functions, including input current shaping and output voltage regulation.

The experimental waveforms under partial load $R_{\rm Load} = 500\ \Omega$(≈180 W) and $R_{\rm Load} = 300\ \Omega$(≈315 W) are plotted in Fig. 12(a) and (b), respectively. Due to the digital resolution of phase signal θ, the input current returns to zero and keep zero current until the next cycle under light load. Thus, the stagnated current would result in rich harmonic currents and the large

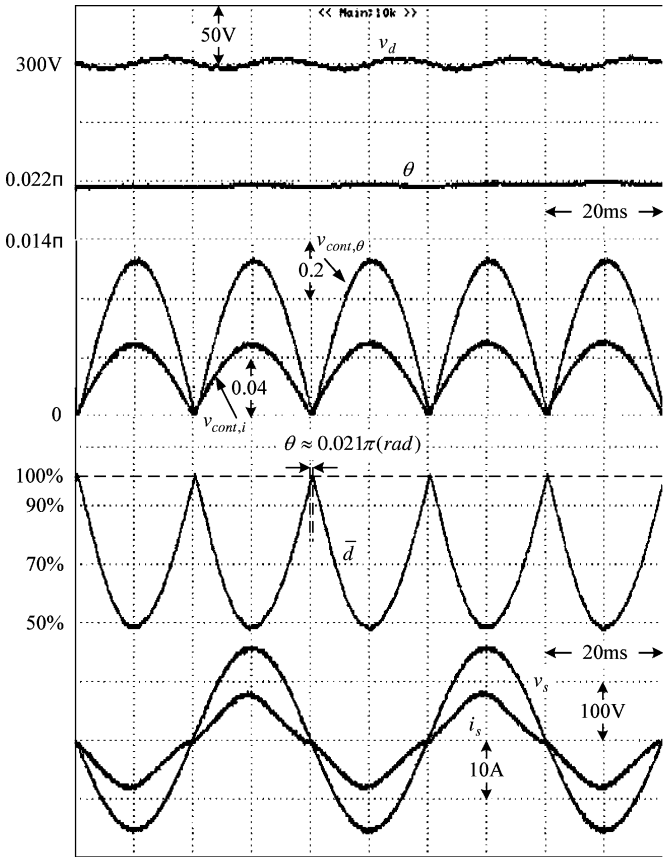

Fig. 11. Experimental steady-state waveforms for SLCSC.

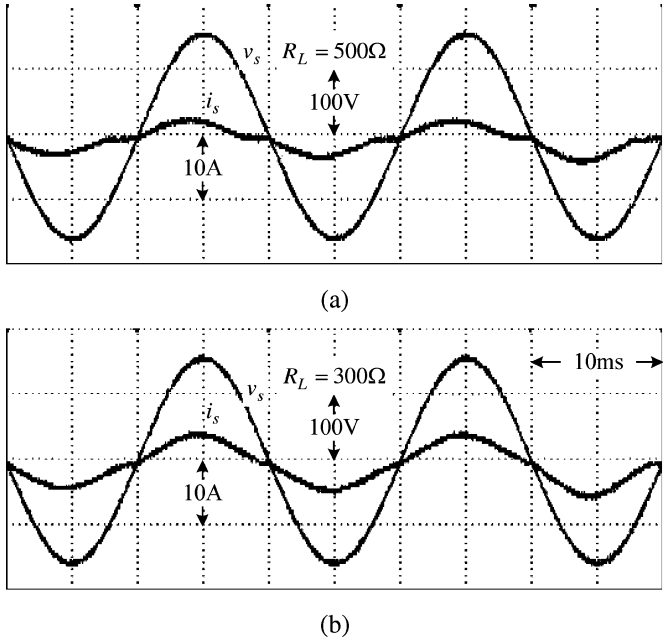

Fig. 12. Experimental input current and voltage waveforms under partial load. (a) $R_{\rm Load} = 500\ \Omega$. (b) $R_{\rm Load} = 300\ \Omega$.

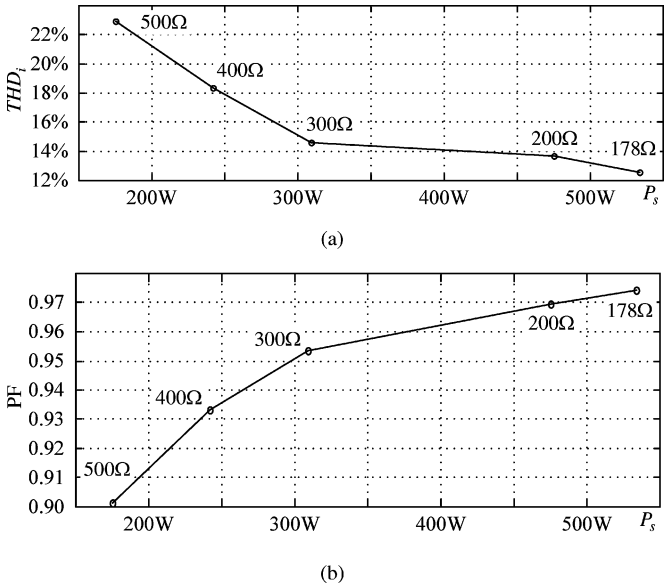

Fig. 13. Experimental variation of (a) THD_i and (b) PF with delivered power.

measured total current harmonic distortion THD_i. To understand the performance of various load power, the experimental variation of the measured total current harmonic distortion THD_i and power factor (PF) with various delivered power are plotted in Fig. 13(a) and (b), respectively. It follows that the higher the delivered power, the smaller the THD_i the input current possesses and the higher PF the input quality. In addition, because in the earlier experiment, the input voltage is the pure sinusoidal voltage, only the fundamental component in input current is able to contribute to generate real power.

In practice, the inductance varies with the inductor current, but the inductance parameter used in control loop is fixed, which implies that parameter mismatch occurs. In simulation, the inductance is fixed, which means that no parameter mismatch occurs. For less current distortion found in the simulated waveforms of Fig. 7, we can find that the inductance mismatch mainly contributes to the current distortion and the expansion of DCM close to the zero-crossing point. In addition, the mismatch of real circuit parameter and the used circuit parameter would lead to two effects. One is the easy entrance into DCM close to the zero-cross points, and the other is the current distortion.

Since the inductance parameter used in control loop is fixed regardless of high and low powers, the parameter mismatch becomes more serious at low power. It contributes to the increase of duration of DCM close to the zero-cross points at low power. Thus, the tendency shown in Fig. 12 is related to the DCM limitations.

B. Transient Response

To verify the dynamic performance of the proposed SLCSC, some experimental results are shown in Fig. 14, where the load resistance is suddenly changed from 200 Ω(≈475 W) to 177.78 Ω(≈530 W). In order to regulate the output voltage, the phase signal θ increases due to the PI-type voltage controller in order to yield sufficient input current and input power. During

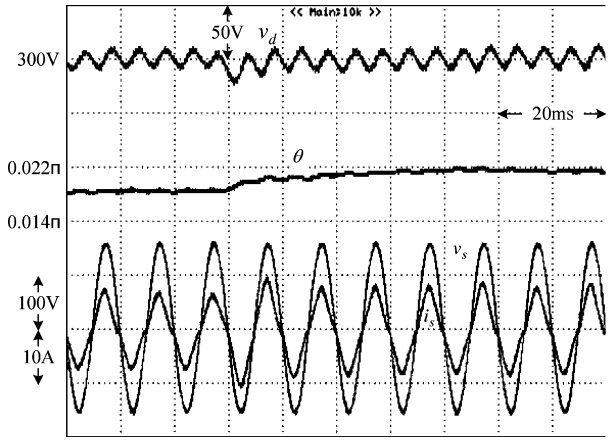

Fig. 14. Experimental waveforms with SLCSC during load regulation.

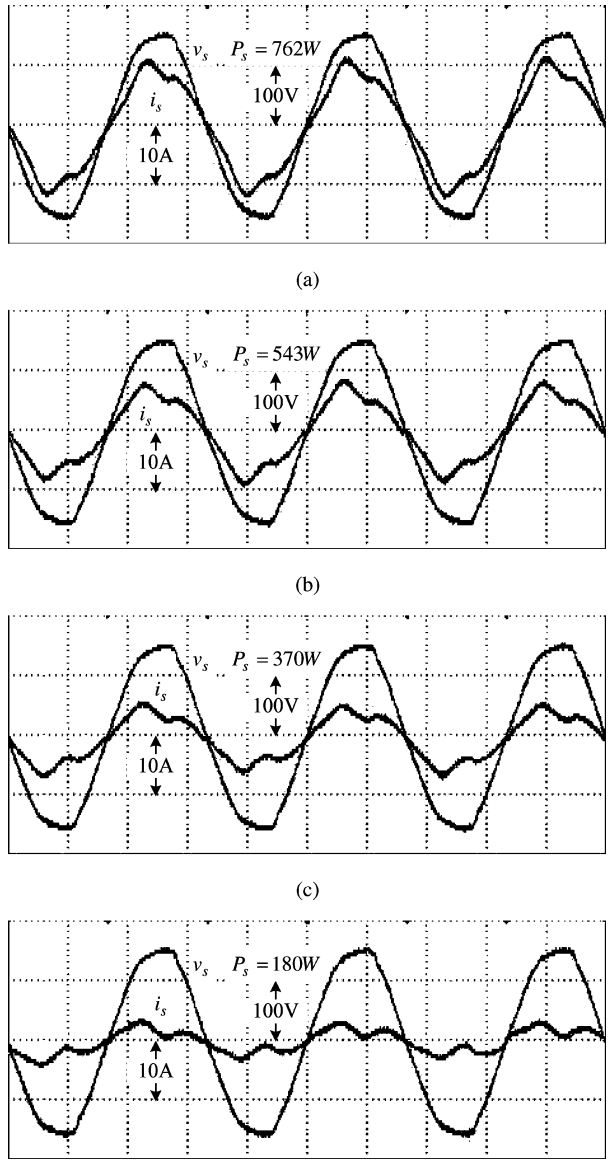

Fig. 15. Experimental input current and voltage waveforms under various load. (a) $P_s = 762$ W. (b) $P_s = 543$ W. (c) $P_s = 370$ W. (d) $P_s = 180$ W.

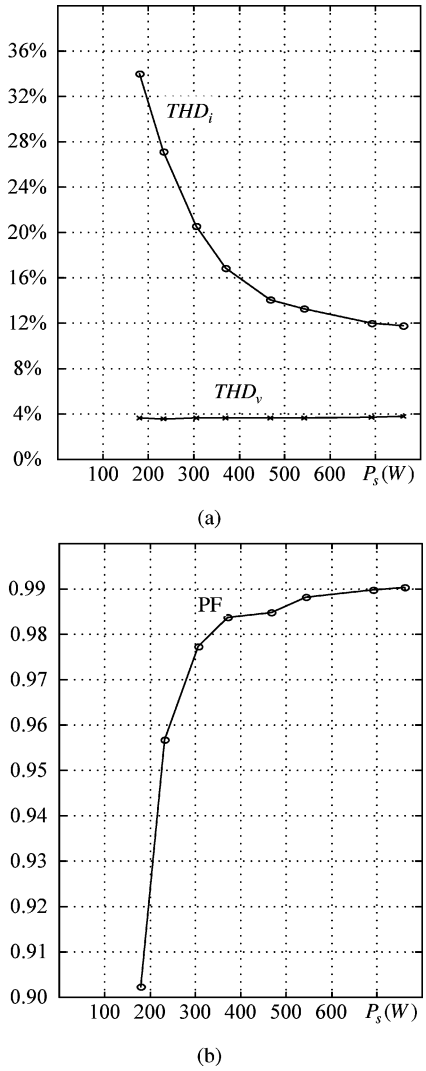

Fig. 16. Experimental variation of (a) THD_i and (b) PF under distorted input voltage.

the regulation, the input current keeps in phase with the input voltage. It clearly shows that the proposed single-loop CSC also possesses good regulation ability.

C. Distorted Input Voltage

To further verify the performance of the proposed SLCSC, a distorted input voltage with $\text{THD}_v \approx 4\%$ is used in the following experiment. Some experimental waveforms with various yielded powers are shown in Fig. 15. From the input waveforms, the proposed SLCSC is stable and still can yield the PFC functions of current shaping and voltage regulation. The variations of THD_i and PF with delivered power are plotted in Fig. 16(a) and (b), respectively. Obviously, due to the voltage distortion, THD_i in Fig. 16(a) is higher than that in Fig. 13(a).

It is noted that with pure sinusoidal input voltage in Figs. 11–14, no average power can be yielded from the harmonic currents. But with the distorted voltage, the harmonic current may result in some average power due to the existence of the voltage component of the same harmonic orders. Therefore, the variation of PF with distorted voltage shown in Fig. 16(b) is slightly higher than that with pure sinusoidal voltage shown in Fig. 13(b).

VI. Conclusion

In this paper, the proposed SLCSC for boost-type SMRs have been analyzed. A prototype of boost-type SMR controlled by a DSP evaluation board was built to verify the proposed SLCSC. From the simulation and experimental results, the proposed SLCSC possesses good performance under not only steady-state condition, but also transient condition, and can meet the desired PFC functions with parameter variation and distorted input voltage. In addition, compared with the conventional multi-loop control, the proposed SLCSC is simple and a cost-effective solution for PFC application.

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