

Very High-Density ($23 \text{ fF}/\mu\text{m}^2$) RF MIM Capacitors Using high- κ TaTiO as the Dielectric

K. C. Chiang, C. H. Lai, Albert Chin, *Senior Member, IEEE*, T. J. Wang, H. F. Chiu, Jiann-Ruey Chen, S. P. McAlister, *Senior Member, IEEE*, and C. C. Chi

Abstract—A very high density of $23 \text{ fF}/\mu\text{m}^2$ has been measured in RF metal-insulator-metal (MIM) capacitors which use high- κ TaTiO as the dielectric. In addition, the devices show a small reduction of 1.8% in the capacitance, from 100 kHz to 10 GHz. Together with these characteristics the MIM capacitors show low leakage currents and a small voltage-dependence of capacitance at 1 GHz. These TaTiO MIM capacitors should be useful for precision RF circuits.

Index Terms—Capacitor, RF metal-insulator-metal (MIM), TaTiO.

I. INTRODUCTION

ACCORDING to International Technology Roadmap for Semiconductors (ITRS), continuous down-scaling of the size of metal-insulator-metal (MIM) capacitors is required to reduce chip size and the cost of analog and RF ICs [1]. The use of a high- κ dielectric [2]–[15] is the only way to achieve this goal, since decreasing the dielectric thickness (t_d) to achieve high capacitance density ($\epsilon_0\kappa/t_d$) degrades the leakage current, loss tangent and voltage-dependence of the capacitance ($\Delta C/C$). Hence, the high- κ dielectric in MIM capacitors has evolved from using SiON ($\kappa \sim 4 - 7$) [3]–[5] and Al₂O₃ ($\kappa = 10$) [13] to HfO₂ ($\kappa \sim 22$) [7]–[11] or Ta₂O₅ ($\kappa \sim 25$) [12], [14]. To increase the κ value beyond 25, the dielectric TiO₂ is a potential candidate, since it can display very high- κ (~ 80). However, the large leakage current from crystallization of the TiO₂ is a major limitation for device applications. Here, we report the use of TiTaO as the dielectric, and show capacitors with low leakage current and without crystallization, even after backend processing. We report devices with a high density of $23 \text{ fF}/\mu\text{m}^2$, a high- κ value of 39–45 (beyond the previous $\kappa \sim 25$

Manuscript received May 25, 2005; revised July 19, 2005. This work was supported in part by the National Science Council of Taiwan, R.O.C. under Grant 92-2215-E-009-031. The review of this letter was arranged by Editor C.-P. Chang.

K. C. Chiang, C. H. Lai, and T. J. Wang are with the Department of Electronics Engineering, Nano-Science Technology Center, National Chiao-Tung University, Hsinchu 300, Taiwan, R.O.C.

A. Chin is with SNLD, Department of Electrical and Computer Engineering, National University of Singapore, Singapore, on leave from the Department of Electronics Engineering, Nano Science Technology Center, National Chiao-Tung University, Hsinchu 300, Taiwan, R.O.C., (e-mail: albert_achin@hotmail.com).

H. F. Chiu and J.-R. Chen are with the Department of Materials Science and Engineering, National Tsing-Hua University, Hsinchu 300, Taiwan, R.O.C.

S. P. McAlister is with the National Research Council of Canada, Ottawa, ON, Canada.

C. C. Chi is with the Department of Physics, National Tsing-Hua University, Hsinchu 300, Taiwan, R.O.C.

Digital Object Identifier 10.1109/LED.2005.856708

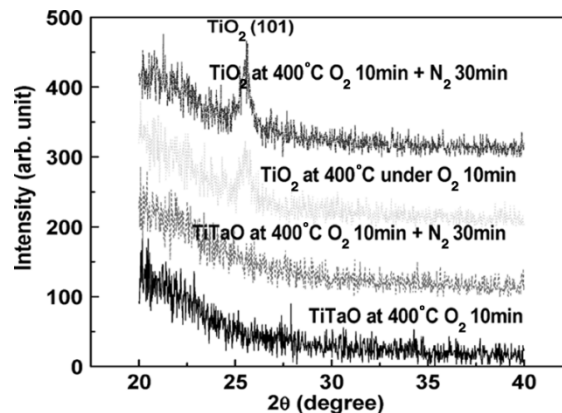


Fig. 1. XRD patterns of TiO₂ and TiTaO dielectric layers, $\sim 28 \text{ nm}$ thick, after 400°C O₂ oxidation and N₂ annealing.

barrier), and low leakage current of $1.2 \times 10^{-6} \text{ A/cm}^2$. This performance of the TiTaO MIM capacitors is accompanied by a small $\Delta C/C$ of 550 ppm at 1 GHz. Compared with current technology these high performance capacitors can drastically reduce the RF capacitor area [1], yet can be fabricated with full compatibility with current VLSI process lines.

II. EXPERIMENTAL PROCEDURE

High- κ TiTaO MIM capacitors were fabricated on 4-in Si wafers. First, a $2\text{-}\mu\text{m}$ -thick isolation SiO₂ was deposited on the Si substrates. The bottom capacitor electrodes were formed by depositing $0.05\text{-}\mu\text{m}$ TaN on a $1\text{-}\mu\text{m}$ Ta layer, followed by patterning. Then, a 17-nm -thick Ti_{*x*}Ta_{*1-x*}O ($x \sim 0.6$) was deposited on the TaN/Ta electrode, followed by 400°C oxidation and annealing. Finally, Al was deposited and patterned to form the top capacitor electrode and RF transmission lines. For comparison purposes devices with TiO₂ as the dielectric was also fabricated using the same process. The fabricated RF MIM capacitors were characterized using an HP4284A precision LCR meter from 10 KHz to 1 MHz, and an HP8510C network analyzer for the S-parameter measurements from 200 MHz to 20 GHz [13]–[15]. The series inductance and RF pads were deembedded from a “through” and “open” transmission lines [16], [17], respectively. The RF frequency capacitance was extracted from the measured S-parameters using an equivalent circuit model [15].

III. RESULTS AND DISCUSSION

Fig. 1 shows the X-Ray diffraction (XRD) patterns of 28-nm -thick TiO₂ and TiTaO layers, which were used to examine the

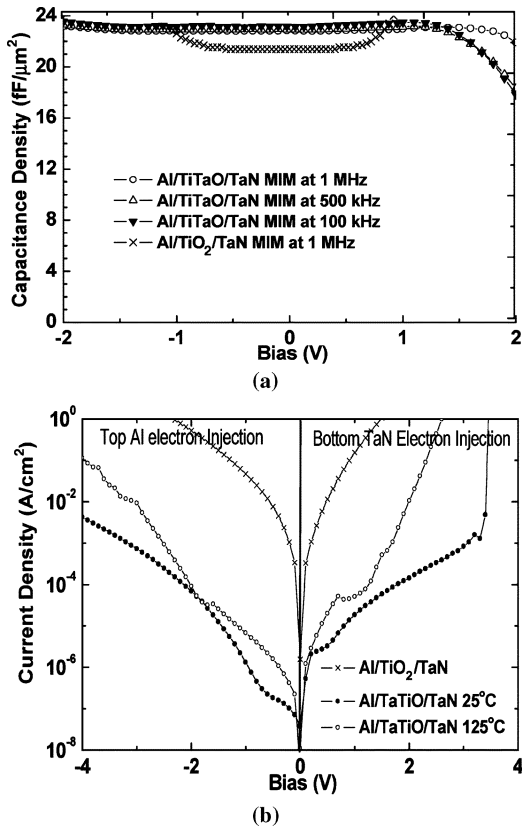


Fig. 2. (a) C - V and (b) J - V characteristics of TiO_2 and TaTiO capacitors. The leakage current is lower in the TiTaO capacitors. The leakage currents at both 25°C and 125°C from top and bottom electrodes are shown for comparison. The capacitor size is $20 \times 20 \mu\text{m}^2$.

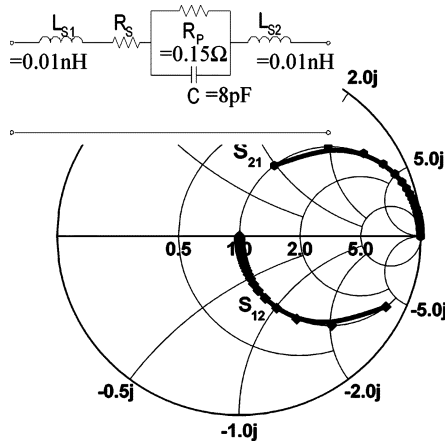


Fig. 3. Scattering parameters of a TiTaO MIM capacitor, from 200 MHz to 20 GHz, after deembedding the through transmission line. Insert: the equivalent circuit model used for capacitance extraction. The capacitor size is $20 \times 20 \mu\text{m}^2$.

thermal stability on their amorphous structure. Significant crystallization of the TiO_2 was measured after a 400°C O_2 treatment for 10 min which became worse after subsequent 30 min N_2 annealing. In contrast the TiTaO was amorphous after the same thermal cycle. This good stability after backend thermal treatment is important in reducing the leakage current in RF MIM capacitors. Further trading off the Ti composition <0.6 in $\text{Ti}_x\text{Ta}_{1-x}\text{O}$ with thermal stability is necessary if higher thermal cycle is used such as 450°C and above.

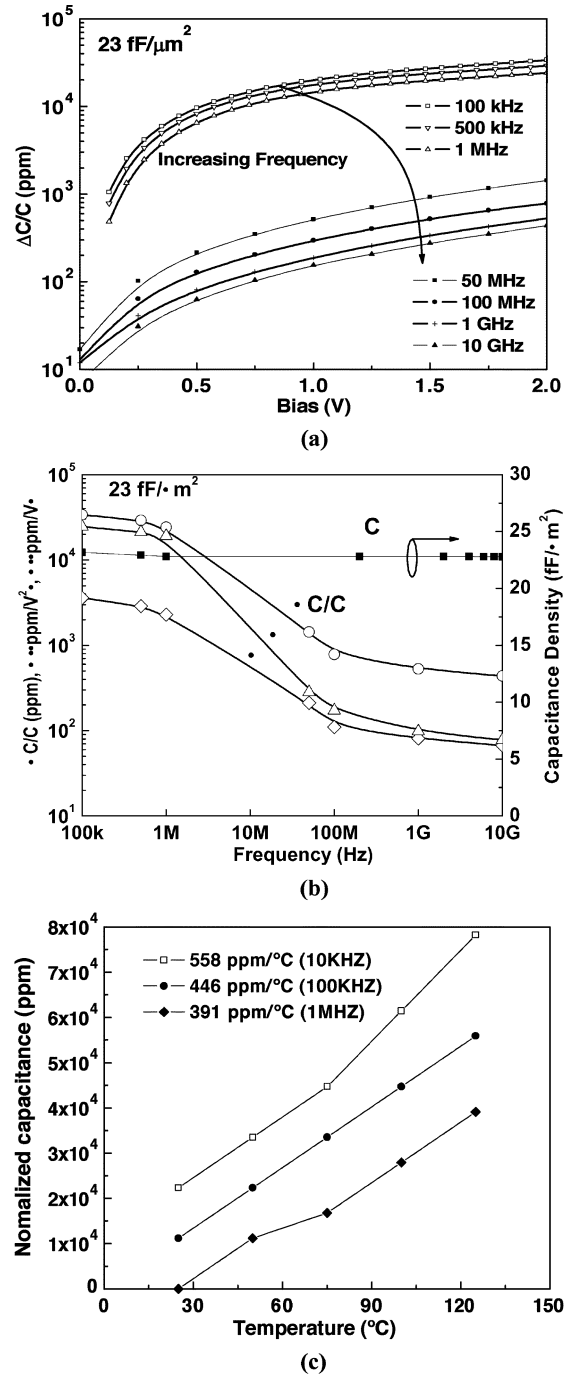


Fig. 4. (a) $\Delta C/C$ - V characteristics of a TiTaO MIM capacitor. The data for frequencies $>1 \text{ MHz}$ were obtained from the S -parameters. (b) Frequency dependent capacitance density, $\Delta C/C$, α and β for a TiTaO MIM capacitor biased at 2 V . (c) Temperature-dependence of capacitance (TCC). The capacitor size is $20 \times 20 \mu\text{m}^2$.

Fig. 2(a) and (b) shows the C - V and J - V characteristics of TaTiO and TiO_2 MIM capacitors. For the TiTaO device a very high capacitance density of $23 \text{ fF}/\mu\text{m}^2$ was measured, giving a high- κ value of ~ 39 , although more detailed study in a different experiment with Transmission Electron Microscopy for thickness calibration gives a κ value of ~ 45 [18]. This κ value is greater than the $\kappa \sim 22$ – 25 value for HfO_2 and Ta_2O_5 which are used in DRAM. However the TiO_2 MIM capacitor showed an unusual capacitance variation at voltages above $\pm 0.75 \text{ V}$. The

poor C - V for the TiO_2 MIM capacitor is thought to be related to its large leakage current, Fig. 2(b), which may be due to the current conduction through grain boundaries of the poly-crystalline TiO_2 . In contrast, constant capacitance values, with little voltage and frequency dependence, were found for the TiTaO MIM capacitor. The TiTaO MIM capacitors have ~ 5 – 7 orders of magnitude lower leakage current than that for the TiO_2 devices. Note that although the ITRS only specifies the capacitance density and Q -factor [1], the leakage current was as low as 5 pA (1.2×10^{-6} A/cm²) at 1 V for a large 9.2 pF capacitor ($20 \times 20 \mu\text{m}^2$ in size) and lower than the leakage current of sub-100 nm transistors [16]. The leakage current, injecting electrons from the Al contact, is lower than that from using the lower TaN electrode. This is due to the better interface for the Al, which also gives better voltage and frequency dispersion in the C - V curves. The leakage current is even worse at 125 °C and the using high work-function metal electrode to reduce the leakage current will be needed [19]–[21].

Fig. 3 shows the measured S -parameters for a TiTaO MIM capacitor, where the capacitance at RF frequencies can be extracted from S -parameters using the equivalent circuit model shown in the insert. Fig. 4(a) displays the $\Delta C/C - V$ characteristics, where the data > 1 MHz were calculated from the measured S -parameters using a circuit-theory derived equation [10]. The frequency dependent capacitance value is shown in Fig. 4(b). The capacitance reduction of 1.8% from 100 kHz to 10 GHz indicates good device performance over the IF to RF range. However, the rapid $\Delta C/C$ reduction with increasing frequency above megahertz regime may be due to the trapped carriers being unable to follow the high frequency signal [10], [15], [17]. Here, the typical carrier lifetime of trap-related Shockley–Read–Hall recombination is in the range ms to μs . The first order voltage linearity (β) and quadratic voltage linearity (α) [7] are also shown in Fig. 4(b). The small $\Delta C/C$ of 550 ppm, low α of 81 ppm/V² and β of 98 ppm/V at 1 GHz are important for high-speed analog/RF IC applications [7]–[11]. Fig. 4(c) shows the temperature-dependence of capacitance (TCC). Again, similar reduction of both capacitance and TCC are found with increasing frequency.

IV. CONCLUSION

Very high 23 fF/ μm^2 capacitance density, with a capacitance reduction of 1.8% from 100 kHz to 10 GHz, and a small 550 ppm $\Delta C/C$ at 1 GHz were simultaneously achieved in novel high- κ TiTaO MIM capacitors processed at 400 °C. These MIM capacitors should be suitable for precision RF circuits.

REFERENCES

[1] International Technology Roadmap for Semiconductors (ITRS), RF & A/MS Technologies for Wireless Chapter, pp. 8–10, 2004.
 [2] C.-M. Hung, Y.-C. Ho, I.-C. Wu, and K. O., "High-Q capacitors implemented in a CMOS process for low-power wireless applications," in *IEEE MTT-S Int. Microw. Symp. Dig.*, 1998, pp. 505–511.

[3] J. A. Babcock, S. G. Balster, A. Pinto, C. Dirnecker, P. Steinmann, R. Jumpertz, and B. El-Kareh, "Analog characteristics of metal-insulator-metal capacitors using PECVD nitride dielectrics," *IEEE Electron Device Lett.*, vol. 22, no. 5, pp. 230–232, May 2001.
 [4] C. H. Ng, K. W. Chew, and S. F. Chu, "Characterization and comparison of PECVD silicon nitride and silicon oxynitride dielectric for MIM capacitors," *IEEE Electron Device Lett.*, vol. 24, no. 8, pp. 506–508, Aug. 2003.
 [5] L. Y. Tu, H. L. Lin, L. L. Chao, D. Wu, C. S. Tsai, C. Wang, C. F. Huang, C. H. Lin, and J. Sun, "Characterization and comparison of high- κ metal-insulator-metal (MIM) capacitors in 0.13 μm Cu BEOL for mixed-mode and RF applications," in *Symp. VLSI Tech. Dig.*, 2003, pp. 79–80.
 [6] Z. Chen, L. Guo, M. Yu, and Y. Zhang, "A study of MIMIM on-chip capacitor using Cu/SiO₂ interconnect technology," *IEEE Microw. Wireless Components Lett.*, vol. 12, pp. 246–248, Jul. 2002.
 [7] C. Zhu, H. Hu, X. Yu, A. Chin, M. F. Li, and D. L. Kwong, "Dependences of VCC (voltage coefficient of capacitance) of high- κ HfO₂ MIM capacitors: an unified understanding and prediction," in *IEDM Tech. Dig.*, Dec. 2003, pp. 379–382.
 [8] S. J. Kim, B. J. Cho, M.-F. Li, C. Zhu, A. Chin, and D. L. Kwong, "HfO₂ and lanthanidedoped HfO₂ MIM capacitors for RF/mixed IC applications," in *Symp. VLSI Tech. Dig.*, 2003, pp. 77–78.
 [9] S. J. Kim, B. J. Cho, S. J. Ding, M.-F. Li, M. B. Yu, C. Zhu, A. Chin, and D.-L. Kwong, "Engineering of voltage nonlinearity in high- κ MIM capacitor for analog/mixed-signal ICs," in *Symp. VLSI Tech. Dig.*, 2004, pp. 218–219.
 [10] H. Hu, S. J. Ding, H. F. Lim, C. Zhu, M. F. Li, S. J. Kim, X. F. Yu, J. H. Chen, Y. F. Yong, B. J. Cho, D. S. H. Chan, S. C. Rustagi, M. B. Yu, C. H. Tung, A. Du, D. My, P. D. Fu, A. Chin, and D. L. Kwong, "High performance HfO₂ - Al₂O₃ laminate MIM capacitors by ALD for RF and mixed signal IC applications," in *IEDM Tech. Dig.*, 2003, pp. 879–882.
 [11] S. J. Kim, B. J. Cho, M.-F. Li, C. Zhu, A. Chin, and D. L. Kwong, "HfO₂ and lanthanidedoped HfO₂ MIM capacitors for RF/Mixed IC applications," in *Symp. VLSI Tech. Dig.*, 2003, pp. 77–78.
 [12] T. Ishikawa, D. Kodama, Y. Matsui, M. Hiratani, T. Furusawa, and D. Hisamoto, "High-capacitance Cu/Ta₂O₅/Cu MIM structure for SoC applications featuring a single-mask add-on process," in *IEDM Tech. Dig.*, 2002, pp. 940–942.
 [13] S. B. Chen, J. H. Lai, K. T. Chan, A. Chin, J. C. Hsieh, and J. Liu, "Frequency-dependent capacitance reduction in high- κ AlTiO_x and Al₂O₃ gate dielectrics from IF to RF frequency range," *IEEE Electron Device Lett.*, vol. 23, no. 4, pp. 203–205, Apr. 2002.
 [14] M. Y. Yang, C. H. Huang, A. Chin, C. Zhu, B. J. Cho, M. F. Li, and D. L. Kwong, "Very high density RF MIM capacitors (17 fF/ μm^2) using high- κ Al₂O₃ doped Ta₂O₅ dielectrics," *IEEE Microw. Wireless Comp. Lett.*, vol. 13, no. 10, pp. 431–433, Oct. 2003.
 [15] C. H. Huang, M. Y. Yang, A. Chin, C. X. Zhu, M. F. Li, and D. L. Kwong, "High density RF MIM capacitors using high- κ AlTaO_x dielectrics," in *IEEE MTT-S Int. Microw. Symp. Dig.*, vol. 1, Jun. 2003, pp. 507–510.
 [16] M. C. King, Z. M. Lai, C. H. Huang, C. F. Lee, D. S. Yu, C. M. Huang, Y. Chang, and A. Chin, "Modeling finger number dependence on RF Noise to 10 GHz in 0.13 μm Node MOSFETs with 80 nm gate length," in *Proc. IEEE RF-IC Symp. Dig.*, Jun. 2004, pp. 171–174.
 [17] K. T. Chan, A. Chin, C. M. Kwei, D. T. Shien, and W. J. Lin, "Transmission line noise from standard and proton-implanted Si," in *IEEE MTT-S Int. Microw. Symp. Dig.*, vol. 2, Jun. 2001, pp. 763–766.
 [18] K. C. Chiang, A. Chin, C. H. Lai, W. J. Chen, C. F. Cheng, B. F. Hung, and C. C. Liao, "Very high κ and high density TiTaO MIM capacitors for analog and RF applications," in *Symp. VLSI Tech. Dig.*, Jun. 2005, pp. 62–63.
 [19] D. S. Yu, A. Chin, C. C. Laio, C. F. Lee, C. F. Cheng, W. J. Chen, C. Zhu, M.-F. Li, S. P. McAlister, and D. L. Kwong, "3D GOI CMOSFETs with novel IrO₂(Hf) dual gates and high- κ dielectric on 1P6M-0.18 μm -CMOS," in *IEDM Tech. Dig.*, 2004, pp. 181–184.
 [20] A. Chin and S. P. McAlister, "The power of functional scaling: beyond the power consumption challenge and the scaling roadmap," *IEEE Circuit Devices Mag.*, vol. 21, no. 1, pp. 27–35, Jan./Feb. 2005.
 [21] C. H. Lai, A. Chin, K. C. Chiang, W. J. Yoo, C. F. Cheng, S. P. McAlister, C. C. Chi, and P. Wu, "Novel SiO₂/AlN/HfAlO/IrO₂ memory with fast erase, large ΔV_{th} and good retention," in *Symp. VLSI Tech. Dig.*, 2005.