Novel Single-Poly EEPROM With Damascene Control-Gate Structure

Hung-Cheng Sung, Tan Fu Lei, Te-Hsun Hsu, S. W. Wang, Ya-Chen Kao, Yung-Tao Lin, and Chung S. Wang

***Abstract*—A novel single-poly EEPROM using damascene control gate (CG) structure is presented in this letter. The CG is tungsten (W) line made by a damascene process, and intergate dielectric is Al_2O_3 grown by atomic layer deposition (ALD). The program and erase mechanism is the same as the one for traditional stacked-gate cell, which uses the channel hot electron injection for programming and Fowler–Nordheim tunneling for channel erasing. With the high dielectric constant (*K*) property of Al_2O_3, we can perform the program and erase function with a voltage less than 6.5 V, which can be handled by 3.3 V devices instead of traditional high voltage devices. In the process compatibility aspect, this new cell needs only two extra masking steps over the standard CMOS process, and the high-κ material is deposited in the back-end metallization steps without the contamination concerns on the front-end process. Therefore, this new technology is suitable for embedded application. In this letter, the good cell performance is demonstrated; such as, fast programming/erasing, good endurance and data retention.**

***Index Terms*—Atomic layer deposition (ALD), damascene, EEPROM, single poly.**

I. Introduction

THE double-poly stacked-gate nonvolatile memory has dominated Flash technology for more than decades because of its small cell size, robust programming/erasing, and good reliability performance [1]. However, up to ten extra masking steps for the cell and high-voltage (HV) devices formation make the embedded application unfavorable due to the high process cost. To overcome the problem, some single poly approaches using well coupling were proposed [2], [3]. However, this kind of approach has a very large cell size, as a result, the application is limited to low-density EEPROM only. In this letter, a novel single-poly EEPROM with small cell size and fewer extra masking steps is presented. The uniqueness of this cell is that the control gate (CG) structure is a tungsten line formed by damascene process and the inter-gate dielectric is the high-κ material grown by atomic layer deposition (ALD) [4]. Because a stronger coupling between CG and floating-gate (FG) is induced by the high-κ material like Al_2O_3, the program and erase voltage can be lowered from ~10 to 6.5 V. Therefore, the program/erase circuitry can be handled by 3.3 V devices instead of conventional HV devices [5], [6]. Furthermore, the cell size can be very compact because the control gate is on top of the FG but not from the huge well diffusion. For CMOS process compatibility, this new approach need only two extra masking steps, which are deep n-well (DNW) and CG, in addition, there is no the high-κ material contamination concerns to the front-end process because the material is deposited during back-end metallization steps. Therefore, the new cell presented in this letter is very suitable for middensity embedded multi-time-program (MTP) applications.

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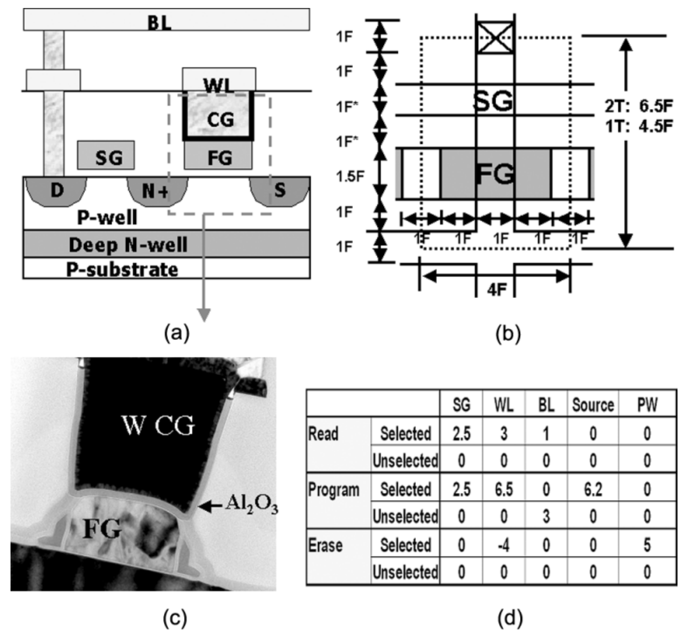

		SG	WL	BL	Source	PW
Read	Selected	2.5	3	1	0	0
	Unselected	0	0	0	0	0
Program	Selected	2.5	6.5	0	6.2	0
	Unselected	0	0	3	0	0
Erase	Selected	0	-4	0	0	5
	Unselected	0	0	0	0	0

Fig. 1. (a) Cross-sectional view of a single cell and (b) top view cell layout. The ideal 2T and 1T cell size is 26 and 18 F^2, respectively, (c) TEM picture of final cell, and (d) typical cell operation condition.

II. Device Fabrication

The cross-sectional and top view of a single cell is shown in Fig. 1(a) and (b). The ideal 2T and 1T cell size is 26 and 18 F^2, respectively [7]. For a feasibility study, a relaxed 2T cell, 1.5 μm^2, is chosen in this experiment because the 2T structure is immune from the over-erase concern [8]. The channel width is 0.32 μm, and the channel length for FG and select gate is 0.4 and 0.18 μm, respectively. The FG overlap with STI is 0.32 μm per side. The starting material is the P-type wafer with 8–12 $\Omega \cdot$cm resistance. The device fabrication begins with a DNW photo and implantation, then uses the standard 0.18-μm CMOS process from shallow-trench isolation (STI) to contact plug formation. The gate oxide (~7 nm) and gate poly (150~200 nm) for periphery devices are acted as the tunneling oxide and floating

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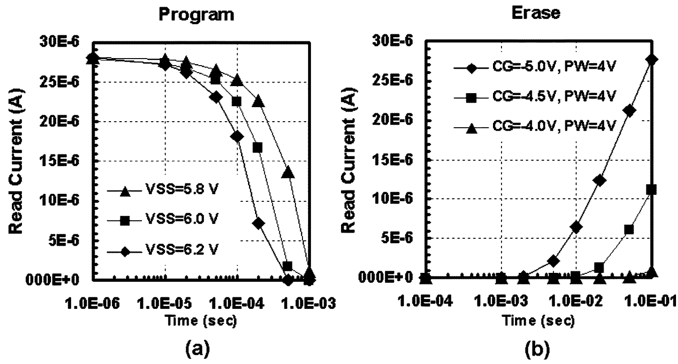

Fig. 2. (a) Program characteristics under different source (V_{ss}) voltage, (b) erasing characteristics with different CG voltage.

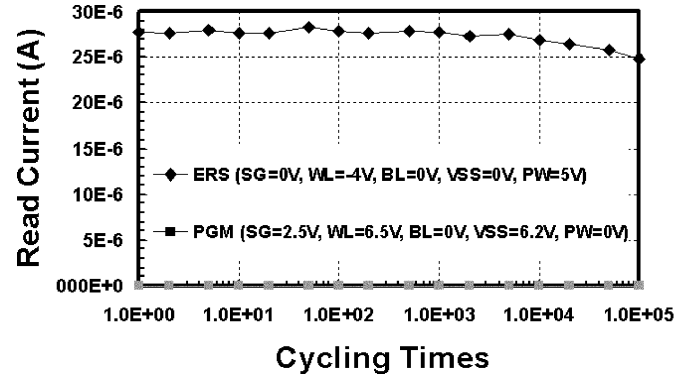

Fig. 3. Endurance cycling characteristics with CHE programming and FN erasing. Only 10% current drop is observed after 100-K cycling.

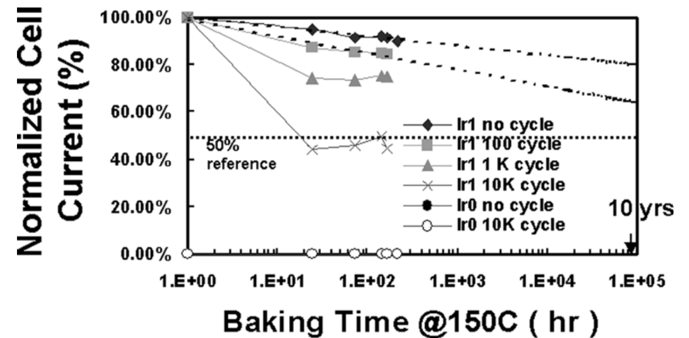

Fig. 4. Data retention characteristics under various precycling stress at 150 °C baking.

poly for this EEPROM device. After contact plug formation, the control gate is formed by a tungsten (W) damascene process, which includes Control gate photo and etching, Al_2O_3 deposition, barrier metal (TiN) deposition, W fill, and CMP. A proper oxidation treatment ($\sim$1 nm) before ALD and a post ALD anneal were done to ensure a good inter-gate dielectric quality. The physical thickness and the equivalent oxide thickness (EOT) of Al_2O_3 is about 20 and 9 nm, respectively. After the CG damascene process, the typical back-end metal process is followed. The transmission electron microscope (TEM) picture of final cell is shown in Fig. 1(c). Note that the high-κ film, Al_2O_3, is deposited in the back-end metallization steps but not in the front-end process shown in the previous works [5], [9], so there is no contamination concern. To prevent data retention problems induced by salicidation, the cell area is blocked with protective oxide during the salicidation process [10].

III. Result and Discussion

The program and erase mechanism is the same as the one for traditional stacked-gate cell, which uses channel hot electron injection for programming and Fowler–Nordheim (FN) tunneling for channel erasing. The typical cell operation is shown in Fig. 1(d). As shown in Fig. 2(a) and (b), the programming and erasing can be accomplished in 500 and 100 ms, respectively. The maximum voltage is 6.5 and 5 V for programming and erasing, respectively. The voltage is less than the typical stacked-gate flash memory because of the stronger FG-CG coupling contributed by the high-κ film, Al_2O_3, whose dielectric constant is nine, which is 2.3 times and 28% higher than oxide and nitride, respectively. The coupling ratio is around 70%, which is calculated from the cell layout and the EOT. No disturb behavior is found on the nonselected cells in bit-line and word-line directions during programming. Figs. 3 and 4 show the single cell reliability on cycling and retention. As shown in Fig. 3, the cell current only degrades 10% after 100-K cycling. In Fig. 4, data retention is projected to last more than ten years at 150 °C for the cells with cycling up to 100 to 1 K. However, the current of the cell with 10-K cycling drops seriously within 24 h but reaches a saturation level on the further extended bake. We think that there are two possible mechanisms causing this current drop. The first one is the trapping characteristics of the Al_2O_3 film, which is known to be a good trapping material [9]. Because there is no sufficient top and bottom barrier for the Al_2O_3 in this study, the charges driven by high program/erase electric field could be easily trapped in Al_2O_3. More cycling times will result in more trapped charges and worsen the data retention performance [11]. The second possible reason is that the tunneling oxide was damaged by the W CMP stress during damascene CG process. To clarify the root cause and to further improve the retention performance, the experiments on the interpoly dielectric film and CG forming process are on going.

IV. Conclusion

The EEPROM cell with W damascene CG was presented for the first time. The device fabrication was very compatible to standard CMOS process because the extra masking step is only two over the CMOS process and the high-κ film is deposited in the back-end metallization steps. The ideal cell size for 2T and 1T cell is about 26 and 18 F^2, which is much smaller than other single poly EEPROM with nwell coupling. In addition, the good single cell performance with 6.5 V program/erase is demonstrated in this letter. Owing to the significant advantages like logic compatible process, compact cell size and low voltage program/erase operation, this new cell is suitable for middensity embedded MTP application.

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REFERENCES

[1] R. Bez, E. Camerlenghi, A. Modelli, and A. Visconti, "Introduction to flash memory," *Proc. IEEE*, vol. 91, no. 4, pp. 489–502, Apr. 2003.

[2] A. Pesavento, T. Gilliland, C. Lindhorst, S. Srinivas, F. Bernard, S. Salazar, C. Diorio, S. King, C. Bockorick, B. Wang, Y. Ma, C. H. Wang, T. Humes, and J. Caywood, "Embedded nonvolatile memory in logic CMOS," in *Proc. IEEE NVSMW*, 2004, pp. 49–50.

[3] K. Ohsaki, N. Asamoto, and A. Takagaki, "A single poly EEPROM cell structure for use in standard CMOS processes," *IEEE J. Solid-State Circuits*, vol. 29, no. 3, pp. 311–316, Mar. 1994.

[4] Y. L. Tu, H. L. Lin, L. L. Chao, D. Wu, C. S. Tsai, C. Wang, C. F. Huang, C. H. Lin, and J. Sun, "Characterization and comparison of high-κ metal–insulator–metal (MiM) capacitors in 0.13 μm Cu BEOL for mixed-mode and RF applications," in *Symp. VLSI Technol. Dig.*, 2003, pp. 79–80.

[5] B. Govoreanu, P. Blomme, M. Rosemeulen, J. Van Houdt, and K. De-Meyer, "VARIOT: a novel multilayer tunnel barrier concept for low-voltage nonvolatile memory devices," *IEEE Electron Device Lett.*, vol. 24, no. 2, pp. 99–101, Feb. 2003.

[6] J. C. Mitros, C. Y. Tsai, H. Shichijo, K. Kunz, A. Morton, D. Goodpaster, D. Mosher, and T. R. Efland, "High-voltage drain extended MOS transistors for 0.18-um logic CMOS process," *IEEE Trans. Electron Devices*, vol. 48, no. 8, pp. 1751–1755, Aug. 2001.

[7] Y. H. Song, J. I. Han, J. W. Kim, J. H. Park, S. Y. Kim, D. W. Kwon, Y. M. Park, J. S. Lee, W. K. Lee, D. Y. Lee, J. W. Kim, M. S. Kang, J. Kim, and K. D. Sub, "A high density and low-cost self-aligned shallow trench isolation NOR flash technology with 0.14 μm^2 cell size," in *IEDM Tech. Dig.*, 2001, pp. 2.4.1–2.4.4.

[8] A. Chimenton, P. Pellati, and P. Olivo, "Overerase phenomena: an insight into flash memory reliability," *Proc. IEEE*, vol. 91, no. 4, pp. 617–626, Apr. 2003.

[9] T. Sugizaki, M. Kobayashi, M. Ishidao, H. Minakata, M. Yamaguchi, Y. Tamura, Y. Sugiyama, T. Nakahishi, and H. Tanaka, "Novel multibit SONOS type flash memory using a high-κ charge trapping layer," in *Symp. VLSI Technol. Dig.*, 2004, pp. 27–28.

[10] J. W. Liou, C. J. Huang, H. H. Chen, and G. Hong, "Characterization of process-induced mobile ions on the data retention in flash memory," *IEEE Trans. Electron Devices*, vol. 50, no. 4, pp. 995–1000, Apr. 2003.

[11] M. Janai, B. Eitan, A. Shappir, E. Lusky, I. Bloom, and G. Cohen, "Data retention reliability model of NROM nonvolatile memory products," *IEEE Trans. Device Mater. Reliab.*, vol. 4, no. 3, pp. 404–415, Sep. 2004.