A Scalable Noise De-Embedding Technique for On-Wafer Microwave Device Characterization

Ming-Hsiang Cho, Guo-Wei Huang, *Member, IEEE*, Yueh-Hua Wang, and Lin-Kun Wu, *Member, IEEE*

***Abstract*—In this letter, we present a scalable and efficient noise de-embedding procedure, which is based on transmission-line theory and cascade configurations, for on-wafer microwave measurements of silicon MOSFETs. The proposed de-embedding procedure utilizes one open and one thru dummy structures to eliminate the parasitic effects from the probe pads and the input/output interconnects of a device-under-test (DUT), respectively. This method can generate the scalable distributed interconnect parameters to efficiently and precisely remove the redundant parasitics of the DUTs with various device sizes and arbitrary interconnect dimensions.**

***Index Terms*—Calibration, de-embedding, MOSFET, noise, S-parameters.**

I. Introduction

With the downscaling device channel length as well as the increasing operation frequency, on-wafer measurement and device modeling work on silicon MOSFETs have become more and more significant for RF/microwave circuit design. To extract the intrinsic device performance from measurements, the unnecessary parasitics of the probe pads and input/output interconnects must be exactly removed from the measured data. In previous literature [1]–[3], several parasitic de-embedding methods based on physical equivalent-circuit models have been developed and extensively utilized over the past decade. These physics-based methods treat the device-under-test (DUT) as an intrinsic device connected to the external parasitics, which come from the probe pads and interconnects, in parallel-series configurations. As the operation frequency becomes higher and/or the interconnect length becomes longer, nevertheless, these equivalent-circuit assumptions may be inappropriate. Recently, a cascade-based de-embedding scheme [4] has been presented, which models the probe pads, interconnects, and the intrinsic device in cascade configurations and does not require any equivalent-circuit representation. On the other hand, for the characterization of devices in various sizes, the conventional de-embedding methods mentioned above may occupy considerable chip area for their corresponding dummy structures. Although the ground-shielded measuring technique has been introduced to offer the fixture scalability and mitigate the chip-area consumption [5], the scalability of the interconnect parameters for parasitic de-embedding has not been comprehensively studied yet. In our previous work [6], a scalable S-parameter de-embedding method based on transmission-line theory and cascade-configuration concept [4] for microwave on-wafer characterization has been presented, and the de-embedding procedure has been verified using thru dummy devices. In this study, we further take the noise parameters into account in the de-embedding procedure and also validate the applicability of the proposed method with measurements on silicon MOSFETs. We find that this scalable de-embedding method is indeed suitable for on-wafer S-parameter and noise measurements, especially the on-wafer automatic characterization [7], of multitype and multisize devices. To substantiate the proposed method, MOSFETs fabricated using a standard 0.25-μm five-level CMOS process were characterized from 1 to 18 GHz.

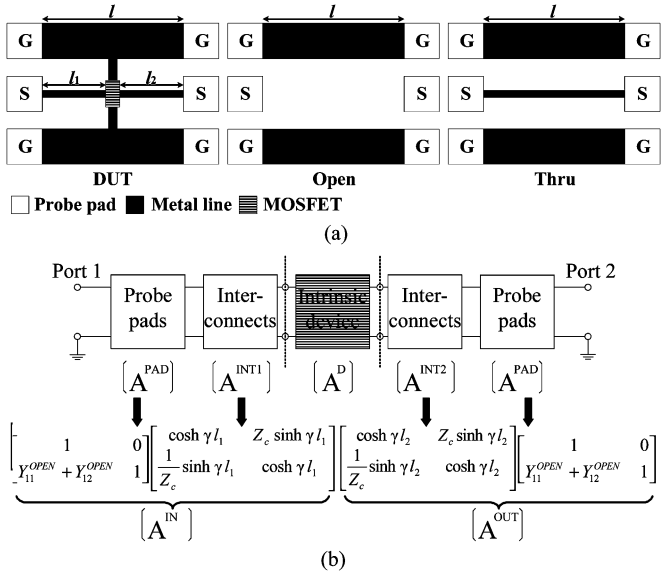

Fig. 1. Proposed de-embedding method. (a) DUT and its corresponding dummy structures. (b) Schematic diagram.

II. Theory of Noise De-Embedding

The proposed de-embedding method is illustrated in Fig. 1. It should be noted that the shield-based structures are not employed in this work for more general consideration. The on-wafer test structures were implemented on silicon substrate for microwave characterization of active devices. Unlike the conventional de-embedding methods, which consume a great deal of chip area for dummy patterns, the proposed new theory requires only two dummy structures for parasitic subtraction. After taking away the probe-pad parasitics with the

Manuscript received March 2, 2005; revised May 25, 2005. The review of this letter was arranged by Associate Editor F. Ellinger.

M. H. Cho and G.-W. Huang are with National Nano Device Laboratories, Hsinchu 300, Taiwan, R.O.C. (e-mail: mhcho@mail.ndl.org.tw).

Y.-H. Wang and L.-K. Wu are with the Department of Communication Engineering, National Chiao Tung University, Hsinchu 300, Taiwan, R.O.C.

Digital Object Identifier 10.1109/LMWC.2005.856685

open dummy, the per-unit-length transmission-line parameters of the thru dummy can be evaluated [6]. Then, DUTs with various device sizes and interconnect lengths can be individually de-embedded with the application of the interconnect scalability.

Similar to the conventional cascade-based method [4], a thru device can be simply modeled in cascade connection. After de-embedding the pad parasitics from $[A^{\rm INT}] = [A^{\rm PAD}]^{-1}[A^{\rm THRU}][A^{\rm PAD}]^{-1}$ and converting the $ABCD$ chain matrix $[A^{\rm INT}]$ to its S-parameter matrix $[S^{\rm INT}]$, where the superscript "-1" denotes the inverse of the matrix and $[A^{\rm INT}]$, $[A^{\rm PAD}]$, and $[A^{\rm THRU}]$ are, respectively, the $ABCD$ chain matrices of the intrinsic interconnects, probe pads, and thru dummy, the interconnect characteristic impedance Z_c and propagation constant γ can be calculated as [8]

$$Z_c = \pm Z_0 \sqrt{\frac{\left(1+S_{11}^{\rm INT}\right)^2 - \left(S_{21}^{\rm INT}\right)^2}{\left(1-S_{11}^{\rm INT}\right)^2 - \left(S_{21}^{\rm INT}\right)^2}} \tag{1}$$

and

$$\gamma = -\frac{1}{l}\ln\left(\left(\frac{1-\left(S_{11}^{\rm INT}\right)^2+\left(S_{21}^{\rm INT}\right)^2}{2S_{21}^{\rm INT}} \pm K\right)^{-1}\right) \tag{2}$$

where Z_0 is the impedance of the S-parameter measurement system, l is the interconnect length, and

$$K = \left(\frac{\left(1-\left(S_{21}^{\rm INT}\right)^2+\left(S_{11}^{\rm INT}\right)^2\right)^2 - \left(2S_{11}^{\rm INT}\right)^2}{\left(2S_{21}^{\rm INT}\right)^2}\right)^{1/2}. \tag{3}$$

For the extraction of Z_c and γ, the "$\pm$" signs in (1) and (2) are used to correct the unreasonable solutions, such as negative attenuation constants [8].

Based on the above results, the $ABCD$ chain matrices of the input and output interconnects with arbitrary line lengths can be generated by respectively substituting the interconnect lengths l_1 and l_2 into the $ABCD$ chain matrix of a lossy transmission line as

$$\left[A^{{\rm INT}i}\right] = \begin{bmatrix} \cosh\gamma l_i & Z_c\sinh\gamma l_i \\ \frac{1}{Z_c}\sinh\gamma l_i & \cosh\gamma l_i \end{bmatrix}, \quad i = 1, 2. \tag{4}$$

The proposed S-parameter and noise de-embedding procedure based on cascade connection is listed as follows.

1) Measure the scattering parameters $[S^{\rm DUT}]$, $[S^{\rm OPEN}]$, and $[S^{\rm THRU}]$ of the DUT, open, and thru, respectively.
2) Measure the noise parameters $NF_{\rm min}^{\rm DUT}$, $R_n^{\rm DUT}$, and $Y_{\rm opt}^{\rm DUT}$ of the DUT and calculate the correlation matrix $\left[C_A^{\rm DUT}\right]$ [9].
3) Convert $\left[S^{\rm OPEN}\right]$ to its admittance matrix $\left[Y^{\rm OPEN}\right]$ and calculate the $ABCD$ chain matrix $\left[A^{\rm PAD}\right]$ of the probe pads from

$$\left[A^{\rm PAD}\right] = \begin{bmatrix} 1 & 0 \\ Y_{11}^{\rm OPEN}+Y_{12}^{\rm OPEN} & 1 \end{bmatrix}. \tag{5}$$

4) Calculate the intrinsic interconnect parameters using $[A^{\rm INT}] = [A^{\rm PAD}]^{-1}[A^{\rm THRU}][A^{\rm PAD}]^{-1}$.
5) Convert $[A^{\rm INT}]$ to its S-parameter matrix $[S^{\rm INT}]$ and calculate the interconnect characteristic impedance Z_c and propagation constant γ based on (1) and (2).
6) Create the $ABCD$ chain matrices $[A^{\rm INT1}]$ and $[A^{\rm INT2}]$ of the input and output interconnects by, respectively, substituting the interconnect lengths l_1 and l_2 into (4).
7) Calculate the $ABCD$ chain matrices of the input port $[A^{\rm IN}]$ and the output port $[A^{\rm OUT}]$ using $[A^{\rm IN}] = [A^{\rm PAD}][A^{\rm INT1}]$ and $[A^{\rm OUT}] = [A^{\rm INT2}][A^{\rm PAD}]$, respectively.
8) Convert $[S^{\rm DUT}]$ to its $ABCD$ chain matrix $[A^{\rm DUT}]$ and calculate the $ABCD$ chain matrix $[A^D]$ of the intrinsic device using $[A^D] = [A^{\rm IN}]^{-1}[A^{\rm DUT}][A^{\rm OUT}]^{-1}$.
9) Convert $[A^D]$ to $[S^D]$, where $[S^D]$ is the intrinsic scattering matrix of the DUT.
10) Convert $[A^{\rm IN}]$ and $[A^{\rm OUT}]$ to their impedance matrices $[Z^{\rm IN}]$ and $[Z^{\rm OUT}]$, respectively.
11) Calculate the noise correlation matrices $\left[C_Z^{\rm IN}\right]$ and $\left[C_Z^{\rm OUT}\right]$ from $\left[C_Z^{\rm IN}\right] = 2kT{\rm Re}([Z^{\rm IN}])$ and $\left[C_Z^{\rm OUT}\right] = 2kT{\rm Re}([Z^{\rm OUT}])$, respectively, where k is the Boltzmann's constant and T is the absolute temperature.
12) Convert $\left[C_Z^{\rm IN}\right]$ and $\left[C_Z^{\rm OUT}\right]$ to their chain matrices $\left[C_A^{\rm IN}\right]$ and $\left[C_A^{\rm OUT}\right]$ using $\left[C_A^{\rm IN}\right] = \left[T^{\rm IN}\right]\left[C_Z^{\rm IN}\right]\left[T^{\rm IN}\right]^H$ and $\left[C_A^{\rm OUT}\right] = \left[T^{\rm OUT}\right]\left[C_Z^{\rm OUT}\right]\left[T^{\rm OUT}\right]^H$, respectively, where the superscript "H" denotes the Hermitian conjugate of the matrix, and the transformation matrix $\left[T^{\rm IN}\right]$ and $\left[T^{\rm OUT}\right]$ are

$$\left[T^{\rm IN}\right] = \begin{bmatrix} 1 & -A_{11}^{\rm IN} \\ 0 & -A_{21}^{\rm IN} \end{bmatrix} \tag{6}$$

and

$$\left[T^{\rm OUT}\right] = \begin{bmatrix} 1 & -A_{11}^{\rm OUT} \\ 0 & -A_{21}^{\rm OUT} \end{bmatrix}. \tag{7}$$

13) Calculate the intrinsic correlation matrix $[C_A] = [A^{\rm IN}]^{-1}\left(\left[C_A^{\rm DUT}\right] - \left[C_A^{\rm IN}\right]\right)([A^{\rm IN}]^H)^{-1} - [A^D]\left[C_A^{\rm OUT}\right][A^D]^H$ [9].
14) Calculate the intrinsic noise parameters $NF_{\rm min}$, R_n, and $Y_{\rm opt}$ from the noise correlation matrix $[C_A]$ using

$$NF_{\rm min} = 1 + \frac{1}{kT}\Big({\rm Re}(C_{A12}) + \sqrt{C_{A11}C_{A22} - ({\rm Im}(C_{A12}))^2}\Big) \tag{8}$$

$$R_n = \frac{C_{A11}}{2kT} \tag{9}$$

and

$$Y_{\rm opt} = \frac{\sqrt{C_{A11}C_{A22} - \left({\rm Im}\left(C_{A12}\right)\right)^2} + j{\rm Im}(C_{A12})}{C_{A11}}. \tag{10}$$

III. Results and Discussion

The on-wafer S-parameter and noise measurements were performed with ATN NP5B Noise Parameter Measurement System. To validate the proposed scalable de-embedding procedure for active devices, three n-MOSFETs with the same device dimensions and various interconnect lengths between

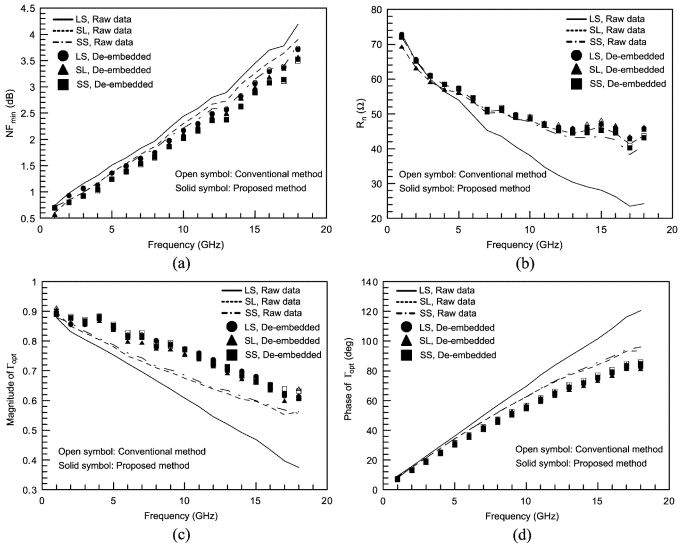

Fig. 2. Noise parameters versus frequency characteristics (a) $NF_{\min}$, (b) R_n, (c) $|\Gamma_{\rm opt}|$, and (d) $\angle\Gamma_{\rm opt}$ of three different n-MOSFETs—LS, SL, and SS obtained from measurement results (lines), conventional de-embedding method (open symbols), and proposed de-embedding method (solid symbols). The DUTs are biased at $V_{\rm DS} = 1.5$ V and $V_{\rm GS} = 1.15$ V ($I_{\rm DS} = 13.3$ mA).

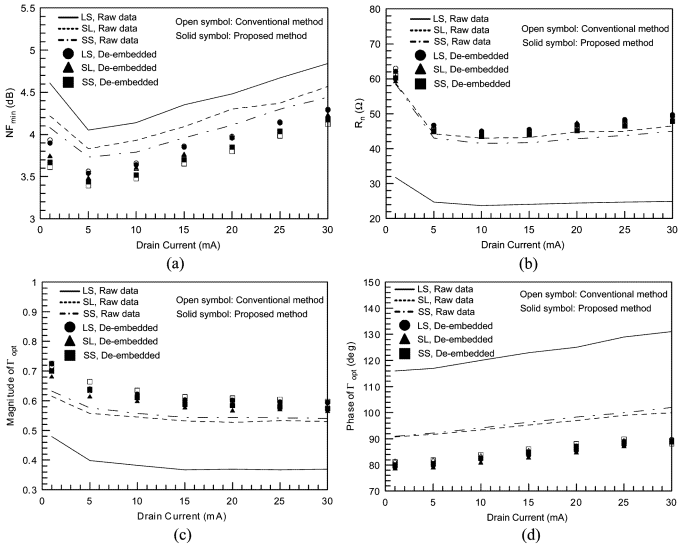

Fig. 3. Noise parameters versus drain current characteristics (a) $NF_{\min}$, (b) R_n, (c) $|\Gamma_{\rm opt}|$, and (d) $\angle\Gamma_{\rm opt}$ of three different n-MOSFETs obtained from measurement results (lines), conventional method (open symbols), and proposed method (solid symbols) at 18 GHz. The DUTs are biased at $V_{\rm DS} =$ 1.5 V and $I_{\rm DS} =$ 1–30 mA.

the probe pads and DUT—LS ($l_1 = 200$ μm, $l_2 = 20$ μm), SL ($l_1 = 20$ μm, $l_2 = 200$ μm), and SS ($l_1 = 20$ μm, $l_2 = 20$ μm), and their corresponding dummy structures were designed and fabricated. The channel length and width of the n-MOSFET are 0.24 and 110 μm (10 μm$\times$ 11), respectively. The interconnect width and the dimensions of probe pads are 10 and 70 μm $\times$ 70 μm, respectively. Fig. 2 shows the measured and de-embedded noise parameters—minimum noise figure ($NF_{\min}$), equivalent noise resistance (R_n), and optimized input reflection coefficient ($\Gamma_{\rm opt}$) versus frequency characteristics of the three MOSFETs biased at $V_{\rm DS} = 1.5$ V and $V_{\rm GS} = 1.15$ V. These results indicate that the intrinsic noise parameters obtained from the conventional cascade-based method [4] and proposed method are in good agreement over the entire frequency range. Fig. 3 exhibits the measured and de-embedded noise parameters versus drain current characteristics of the three MOSFETs at 18 GHz. The interconnects at input port of LS are longer than those of SL and SS and thus have more impact on the measured noise parameters. However, after finishing the noise de-embedding, the intrinsic noise parameters of the three MOSFETs obtained from the conventional cascade-based method and proposed scalable method are approximately the same. Based on the above findings, we can use this proposed de-embedding method instead of the conventional one to efficiently calculate the intrinsic noise parameters of the MOSFETs.

IV. Conclusion

In this study, a general noise de-embedding method suitable for on-wafer device characterization has been presented and verified with various devices. This method requires only one open and one thru dummy structures to generate the scalable and repeatable interconnect parameters for parasitic subtraction. Therefore, the consumption of chip area for dummy structures can be minimized. Compared with the conventional cascade-based method, the proposed one can eliminate the unwanted parasitics of the DUTs more efficiently.

References

[1] M. C. A. M. Koolen, J. A. M. Geelen, and M. P. J. G. Versleijen, "An improved de-embedding technique for on-wafer high-frequency characterization," in *Proc. IEEE Bipolar Circuits Technol. Meeting*, 1991, pp. 188–191.

[2] H. Cho and D. E. Burk, "A three-step method for the de-embedding of high-frequency S-parameter measurements," *IEEE Trans. Electron Devices*, vol. 38, no. 6, pp. 1371–1371, Jun. 1991.

[3] T. E. Kolding, "A four-step method for de-embedding gigahertz on-wafer CMOS measurements," *IEEE Trans. Electron Devices*, vol. 47, no. 4, pp. 734–740, Apr. 2000.

[4] C. H. Chen and M. J. Deen, "A general noise and S-parameter deembedding procedure for on-wafer high-frequency noise measurements of MOSFETs," *IEEE Trans. Microw. Theory Tech.*, vol. 49, no. 5, pp. 1004–1004, May 2001.

[5] T. E. Kolding, "Shield-based microwave on-wafer device measurements," *IEEE Trans. Microw. Theory Tech.*, vol. 49, no. 6, pp. 1039–1039, Jun. 2001.

[6] M. H. Cho, G. W. Huang, K. M. Chen, and A. S. Peng, "A novel cascade-based de-embedding method for on-wafer microwave characterization and automatic measurement," in *IEEE MTT-S Int. Dig.*, Jun. 2004, pp. 1237–1240.

[7] G. W. Huang, D. Y. Chiu, K. M. Chen, Y. M. Deng, and S. C. Wang, "An automatic program suitable for on-wafer characterization, and statistic analysis of microwave devices," in *61st ARFTG Conf. Dig.*, Jun. 2003, pp. 157–161.

[8] W. R. Eisenstadt and Y. Eo, "S-parameter-based IC interconnect transmission line characterization," *IEEE Trans. Compon., Hybrids, Manufact. Technol.*, vol. 15, no. 5, pp. 483–483, Aug. 1992.

[9] H. Hillbrand and P. H. Russer, "An efficient method for computer-aided noise analysis of linear amplifier networks," *IEEE Trans. Circuits Syst.*, vol. CAS-23, no. 4, pp. 235–235, Apr. 1976.