A Novel Dynamic Threshold Voltage MOSFET (DTMOS) Using Heterostructure Channel of $Si_{1-y}C_y$ Interlayer

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***Abstract*—We have demonstrated the fabrication of dynamic threshold voltage MOSFET (DTMOS) using the $Si_{1-y}C_y(y = 0.005)$ incorporation inerlayer channel. Compare to conventional Si-DTMOS, the introduction of the $Si_{1-y}C_y$ interlayer for this device is realized by super-steep-retrograde (SSR) channel profiles due to the retardation of boron diffusion. A low surface channel impurity with heavily doped substrate can be achieved simultaneously. This novel $Si_{1-y}C_y$ channel heterostructure MOSFET exhibits higher transconductance and turn on current.**

***Index Terms*—DTMOS, super-steep-retrograde (SSR) channel, $Si_{1-y}C_y$.**

I. Introduction

As MOS devices continue to be scaled down, the low supply voltage is desirable to minimize the power consumption. The dynamic threshold MOSFET (DTMOS) structure offers a promising technology to achieve both high speed and low power performance [1], [2]. By shorting the gate to the body, the threshold voltage operating under the DT-mode is reduced by forward biasing of the body, so its current drive can be significantly enhanced in the on state. In addition, the subthreshold swing could be attain to the ideal value ($\sim$ 60 mV/dec). To enhance the driver current under DT-mode, large body factor, γ, is necessary to increase the threshold voltage reduction. The γ factor was strongly depended on the substrate impurity doping concentration. In order to take full advantage of the high current drive inherent in DTMOS, Chang *et al.* proposed the use of super-steep-retrograde (SSR) indium-channel profile [3], [4]. On the other hand, Takagi *et al.* also proposed a novel SiGe channel heterostructure DTMOS for reducing the threshold voltage in spite of keeping impurity doping level at the body region [5].

Transient enhanced diffusion (TED) of boron and phosphorus during annealing of implantation damage can be suppressed by incorporation of substitutional carbon [6][7]. $Si_{1-y}C_y$ layer have been applied to suppress boron diffusion in heterojunction bipolar transistors (HBTs) [10], [11]. The incorporation of substitutional carbon in silicon can reduce fast diffusion spices of boron diffusion in silicon. An explanation for this behavior has been provided that the substitutional carbon present in the silicon substrate acts as the sink for silicon self-interstitial and the carbon spices are displaced by the silicon self-interstitial during thermal treatment processes. In this letter, a novel $Si_{1-y}C_y$ heterostructure n-channel DTMOS with boron implantation was studied. Compare to those two samples, with and without $Si_{1-y}C_y$ interlayer, it shows superiority over conventional DTMOS. We have successfully achieved the low threshold voltage and heavily doped substrate DTMOS with superior characteristics in terms of the higher transconductance and saturation current.

Manuscript received May 13, 2005; revised July 5, 2005. This work was supported in part by the Electronics Research and Service Organization, Industrial Technology Research Institute under Contract C93079. The review of this letter was arranged by Editor K. T. Kornegay.

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Digital Object Identifier 10.1109/LED.2005.856011

II. Experimental

Two samples, with and without (w/o) carbon incorporation, were prepared. Samples in this letter were grown epitaxially on (100) silicon wafer in ultrahigh vacuum chemical vapor deposition (UHVCVD) system with a thin 5-nm $Si_{1-y}C_y(y = 0.005)$ layer and 30 nm silicon cap layer. The substrates were implanted with 2×10^{13} cm^{-2} BF_2 at 75 keV and annealed at 950 °C for 30 s. The 6-nm gate oxide was grown, followed by the deposition of a 200-nm polysilicon gate. After gate patterning, a self-aligned n+ poly Si gate and source/drain ion implantation with P of 1×10^{15} cm^{-2} was formed at 40 keV. The body contact junction was implanted and annealed by BF_2 in the rapid thermal process (RTP) system at the same substrate annealing conditions. Afterwards, a passivation layer was deposited and patterned to complete contact metallization. The gate and body contacts were provided separately. Electrical characteristics were performed using a HP4156 system.

III. Results and Discussion

The channel profiles were measured by the secondary ion mass spectroscopy (SIMS) for with and without $Si_{1-y}C_y$ layer shown in Fig. 1. The profiles were measured after all thermal cycles. Compare to control sample, the samples with the $Si_{1-y}C_y$ layer exhibit a super-steep-retrograde channel profile. In the presence of carbon, the boron concentration was dropped from 1.8×10^{18}cm^{-3} to $\sim 10^{17}$cm^{-3} over a distance of 30 nm. By introducing carbon atom, the carbon significantly reduces TED of boron atom. The substitutional carbon provides a sink for excess interstitials in crystalline Si which suppressing interstitial-enhanced boron diffusion. The efficacy of incorporation carbon

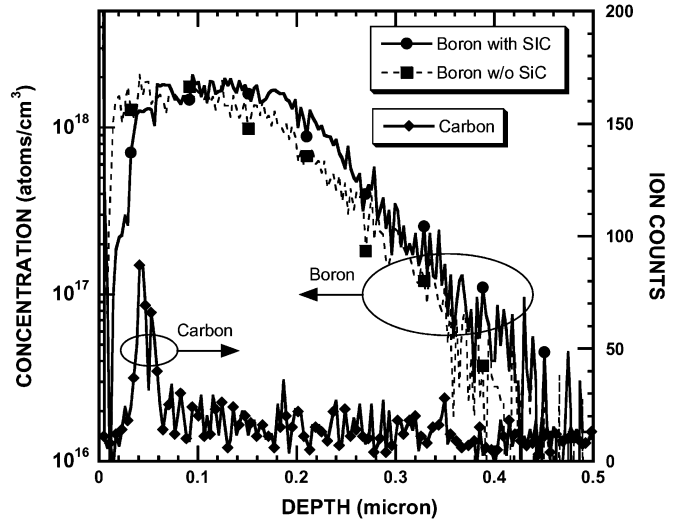

Fig. 1. SIMS measurements of boron and carbon diffusion profile in the channel region.

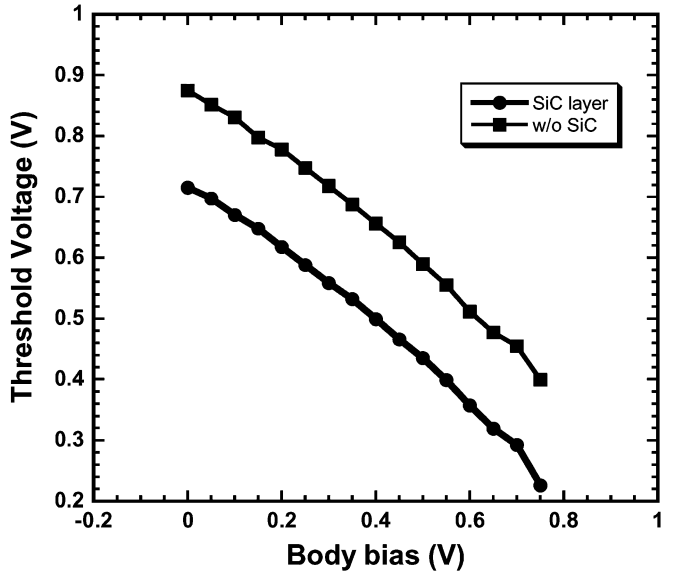

Fig. 2. Threshold voltage versus different body bias for a $W/L = 10\ \mu$m/5 μm NMOSFET.

has been attributed to its ability to locally suppress the silicon self-interstitial concentration [6]–[9].

From SIMS analysis (shown previously in Fig. 1), the sample with $Si_{1-y}C_y$ layer has lower surface dopant concentration than the control sample while they have the same substrate doping concentration. It can therefore have a higher bulk impurity and does not increase the threshold voltage $(V_{\rm th})$. Fig. 2 shows the body effects of n-channel MOSFET with and without $Si_{1-y}C_y$ interlayer samples. A separate terminal was used to control the body voltage. The threshold voltage at zero body bias is denoted for its initial threshold voltage. They have almost the same slope because of its similar substrate concentration. However, the surface concentration for the $Si_{1-y}C_y$ sample is lower than that of w/o $Si_{1-y}C_y$ interlayer samples. We found the $Si_{1-y}C_y$ sample indeed depicts a lower threshold voltage for lightly doped channel surface.

Fig. 3 shows the drain current versus gate voltage in subthreshold region which the device size is $W/L = 10\mu$m/5 μm. The drain voltage was 0.1 V. In the DT-mode operation, the

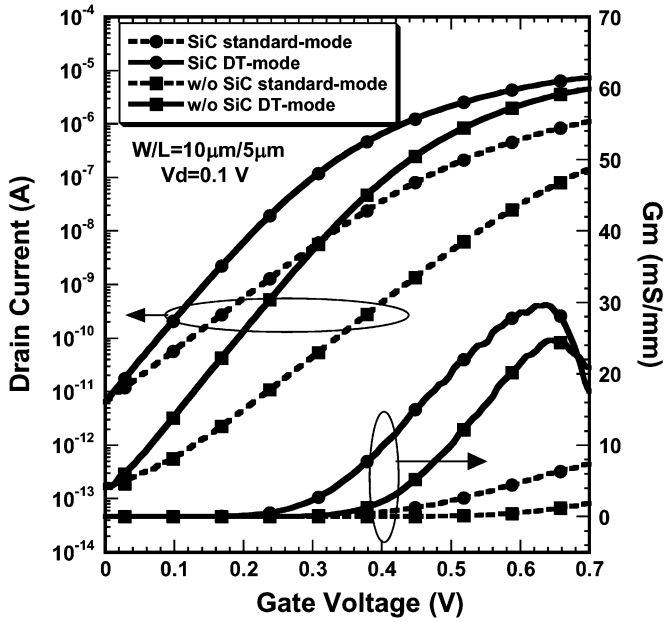

Fig. 3. Subthreshold characteristics of NMOSFET under standard-mode and DT-mode. Drain current and transconductance (V_m) for the samples with and without $Si_{1-y}C_y$ layer.

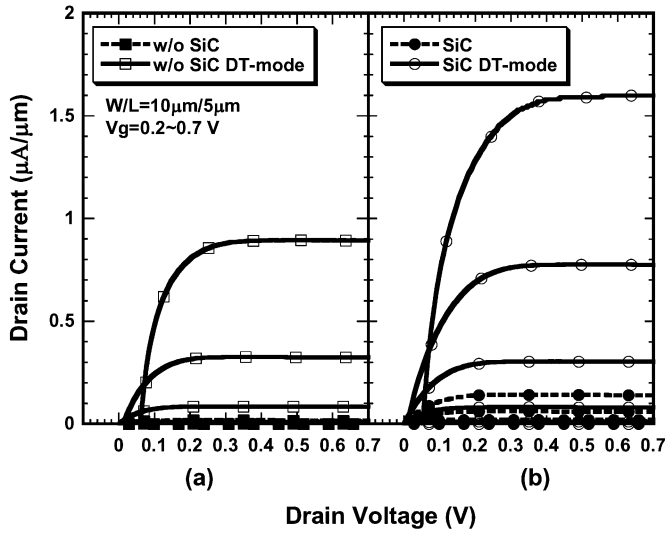

Fig. 4. Drain current of (a) without $Si_{1-y}C_y$, and (b) with $Si_{1-y}C_y$ devices in standard-mode and DT-mode. Gate voltage varies from 0.2 to 0.7 V in 0.1 V step.

gate and body contacts are tied to together (i.e., $V_G = V_{\rm sub}$) and standard mode operation (i.e., $V_{\rm sub} = 0$ V). The subthreshold swing for both samples show nearly ideal value (about 60 mV/dec.) which has been explained by Assaderaghi *et al.* [2]. Corresponding transconductance (G_m) is also shown in Fig. 3, it shows 1.2 times higher G_m between with and w/o $Si_{1-y}C_y$ samples. We believe this is due to the lower surface doping concentration and the larger body factor of $Si_{1-y}C_y$ sample. A low impurity surface channel and the heavily doped body enhances the body bias effect, and devices show the combination of low $V_{\rm th}$ and high body factor, simultaneously. In addition, in both operation modes, the G_m shows it superiority over the sample w/o $Si_{1-y}C_y$ interlayer. From Figs. 1 and 2, the channel surface impurity doping concentration determines the impurity

scattering phenomenon. The output characteristics of with and w/o $Si_{1-y}C_y$ layer under standard and DT-mode operation varies from 0.2 to 0.7 V with a 0.1 V step. The current drives of those two samples in the standard and DT-mode for the device size of $W/L = 10$ μm/5 μm were shown in Fig. 4(b), respectively. The drain current for the sample with $Si_{1-y}C_y$ layer is 1.8 times larger than that of Si DTMOS. In addition, the saturation current under DT-mode was larger than that under standard mode. It is worthy to note here that the disaster under DT-mode in $V_G = 0.7$ V was due to the leakage current between the substrate and source terminals diode, which limit the operation voltage of DT-mode to $V_G < 0.7$ V.

IV. Conclusion

We have developed a novel n-channel $Si_{1-y}C_y$ interlayer heterostructure DTMOS structure. This layer could effectively reduce the diffusion of boron beneath the channel region. A low surface channel impurity with heavily doped substrate can be achieved simultaneously. The excellent performances obtained in the $Si_{1-y}C_y$ interlayer DTMOS are due to both the same substrate doping concentration and lower channel surface impurity concentration. So its surface impurity scattering could be reduces and it can offer a superior performance in future scaled devices. This device achieves 1.2 times higher G_m and 1.8 times larger drain current. It appears to be a very promising technology for nano-scale device and ultra-low voltage application.

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