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An interfacial investigation of high-dielectric constant material hafnium oxide on Si substrate☆

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Abstract

In this study, the hump in the capacitance–voltage (C–V) curves, variation of leakage current, interfacial layer increase, and electron trapping in non-surface treated hafnium oxide (HfO_2) samples were observed and investigated. From the results of the investigation, it was found that both rapid thermal oxidation and NH_3 surface treatments improved the C–V curves. In addition, it was observed that samples treated with ammonia exhibited a lower leakage current when compared with the others. From the results of the dielectric leakage current study, a severe electron trapping effect was exhibited under higher electric field stress. Finally, the conduction mechanism in the HfO_2 thin film was dominated by Frenkel–Poole emission in a high electric field.

Keywords: Dielectrics; Electrical properties and measurements; Surface and interface state; Transmission electron microscopy (TEM)

1. Introduction

The continuous shrinkage in Metal-Oxide-Semiconductor Field Effect Transistor dimensions is accompanied by a scaling of gate oxide thickness. It is well known that the scaling of conventional SiO_2 is approaching the predicted limit due to large direct tunneling leakage current, thereby presenting a fundamental challenge to continual scaling. Therefore, an alternative gate dielectric material is needed to replace SiO_2. High dielectric constant (high-k) materials are the potential candidates because a thicker film is utilized to reduce the leakage current while maintaining the same gate capacitance. Such a suitable high-k material should have a wide band gap, high barrier height for both electrons and holes, and good thermal stability. As many investigations of high-k materials have reported [1], hafnium oxide (HfO_2) is considered as one of the candidates with the most potential. In this experiment, Metal Organic Chemical Vapor Deposition (MOCVD) technology is used to deposit an HfO_2 film. Two forms of surface treatment, Rapid Thermal Oxidation and NH_3 surface treatment, were studied for their effects on the electrical characteristics of HfO_2 thin films. Planar Metal-Insulator-Semiconductor capacitors were utilized to realize the measurements of the electrical characteristics such as leakage current, electron trapping effect, and the extraction of the conduction mechanism in HfO_2 thin film.

2. Experimental details

To begin, the p-type Si wafers were cleaned with standard RCA clean. The samples were divided into two groups. One group was distinguished as being without any surface treatment before HfO_2 deposition, while the other was classified as having undergone surface treatment before HfO_2 deposition. The two surface treatments used for this

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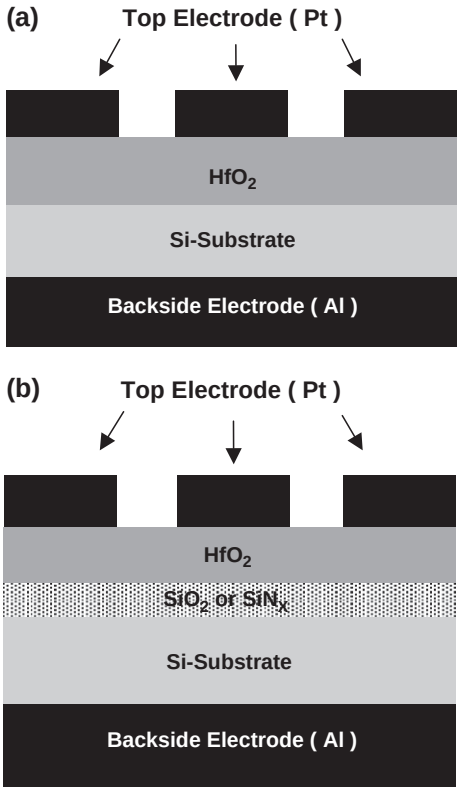

Fig. 1. MIS capacitor structure in this study: (a) Direct HfO_2 deposition without surface treatment, and (b) RTO and NH_3 surface treatment prior to the HfO_2 deposition. An interfacial layer grew after these surface treatments.

study include rapid thermal oxidation (RTO) and ammonia (NH_3) surface treatment. RTO is intended to deposit an ultra thin SiO_2 layer (~10 Å, measured by an optical measurement system-ellipsometer) at 700 °C followed by annealing at 1100 °C using a rapid thermal process system. The NH_3-treatment was performed in a high temperature furnace at 800 °C for 1 h. After the NH_3-treatment, a SiN_X layer (~10 Å) was deposited. A MOCVD system with a gas flow of O_2/N_2O at 250/250 sccm and a pressure of 5 mbar was used to deposit the HfO_2 film at 400 °C. The thickness of the HfO_2 films were 100 Å and 50 Å for the non-surface treated and surface treated samples, respectively. After HfO_2 deposition, a high temperature post deposition annealing was performed at 600, 800, and 1000 °C, for 30 s, respectively. The gate electrode and the backside contact were created by a Physical Vapor Deposition system. The dual electron gun system was used to deposit the Pt film (1000 Å) as the top gate electrode, and the thermal evaporation system was employed to deposit the Al film (5000 Å) as the backside contact. The MIS capacitor structure used in this study is shown in Fig. 1. The capacitance–voltage (C–V) and current density–electric field (J–E) characteristics were investigated by HP-4284 and HP-4156C systems. Transmission electron microscopy (TEM) was used to determine the exact thickness, and to identify the interface between HfO_2 and Si substrate and the interface between HfO_2 and gate electrode.

3. Results and discussions

3.1. Thermal stability

After the deposition of high-k materials, other high temperature processes, such as source/drain activation, are sometimes performed during very large scale industrial fabrication of integrated circuits. Such high-temperature treatments are likely to change the morphology and properties of high-k thin films [2]. Fig. 2 shows the capacitance equivalent thickness (CET) of HfO_2 samples without surface treatment after various post deposition annealing (PDA) at 600, 800, and 1000 °C. The CET is almost the same as the as-deposited samples after post deposition annealing at 800 °C. However, the CET increases drastically after 1000 °C PDA. This is due to the significant increase in the thickness of the interfacial layer between the HfO_2 and the Si substrate. The exact composition of such interfacial layer is not yet clear, but it is believed that the dielectric constant of the interfacial layer is much lower than that of HfO_2. Therefore, the presence of the additional interfacial layer would significantly increase the CET and thus reducing the effective dielectric constant.

Fig. 3 exhibits the current density–electric field (J–E) curves of the HfO_2 samples at various PDA temperatures. The electric field is defined as the gate bias divided by the CET. For the as-deposited samples with 600 and 800 °C PDA, a higher annealing temperature leads to higher leakage current. Since a higher PDA temperature could possibly cause the dielectric materials to crystallize, it contributes to a larger leakage current. The capacitance of PDA 600 and 800 °C at strong accumulation are 1.05 μF/cm^2 and 1.11 μF/cm^2, respectively. The capacitance did not decrease significantly at 800 °C PDA. Therefore, the effect of dielectric crystallization is much more obvious than the growing of a thicker interfacial layer. For the 1000 °C-

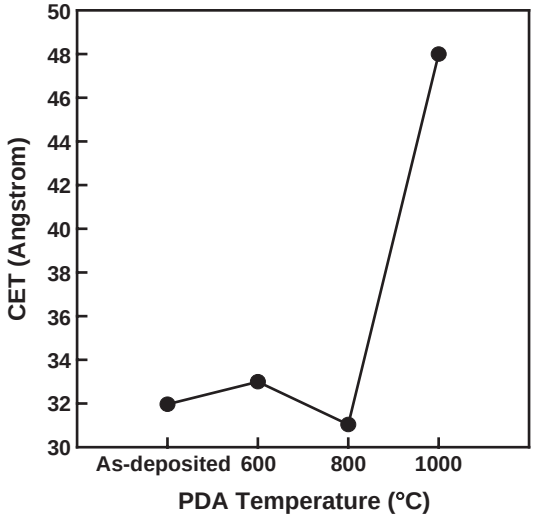

Fig. 2. CET of HfO_2 samples after post deposition annealing temperatures of 600, 800, and 1000 °C, respectively.

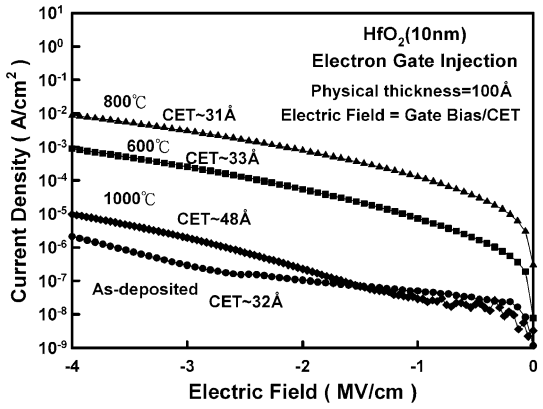

Fig. 3. J–E curves of HfO_2 samples with various PDA temperatures.

annealed sample, the thicker interfacial layer helps resist large leakage current. Fig. 4(a), (b), and (c) show the influence of PDA temperatures on HfO_2 in TEM analyses. In Fig. 4 (c), an obvious change of growth in the interfacial layer can be observed at 1000 °C PDA. The increased thickness is about 30 Å, which results in the lower leakage current in the HfO_2 thin film after the 1000 °C PDA.

3.2. Effects of surface treatments

Fig. 5 shows the comparison of the C–V characteristics between surface-treated and non-surface-treated samples. The hump of the C–V curve can be observed in the samples without surface treatment. Both RTO and NH_3 surface treatments significantly reduced the C–V hump that was observed in the non-surface-treated sample. It was observed that both surface treatments changed the interfacial layer at the dielectric/Si interface, and improved the dielectric properties [3]. In Fig. 6, the leakage currents of the samples with various surface treatments are shown. The NH_3 surface treatment not only improved the C–V curves, but also reduces the leakage current. This is due to the introduction of nitrogen which actually increases the dielectric constant of the interfacial layer in the NH_3 treated samples. After the HfO_2 deposition at the same physical thickness (50 Å), the capacitance of RTO and NH_3 surface treatment at strong accumulation are measured at 1.39 μF/cm^2 and 1.60 μF/cm^2, respectively. The results indicate that the higher capacitance of the NH_3 treated samples is due to the increasing dielectric constant of the interfacial layer. Moreover, the NH_3 pre-treatment provides strong Si–N bonds and sufficient barrier height for the interfacial layer to suppress the leakage current [3,4].

3.3. Electron trapping effect

Fig. 7 shows the leakage current of the as-deposited HfO_2 film after a gate injection stress, after which, a reduction of leakage current became evident. This is due to the fact that electrons were captured in the HfO_2 film, and it is these captured electrons that resisted subsequent injected electrons, resulting in the electron trapping effect that was observed in the as-deposited HfO_2 samples. The as-deposited HfO_2 thin film samples without any PDA treatment have considerable initial traps. Therefore, electron trapping becomes significant after the gate injection stress. Fig. 8 shows the leakage current of the PDA treated HfO_2 samples after a gate injection stress. The 600, 800, and 1000 °C PDA all show nearly identical results. Due to high temperature annealing reducing the defects in the HfO_2 thin film, electron trapping is eliminated in high temperature

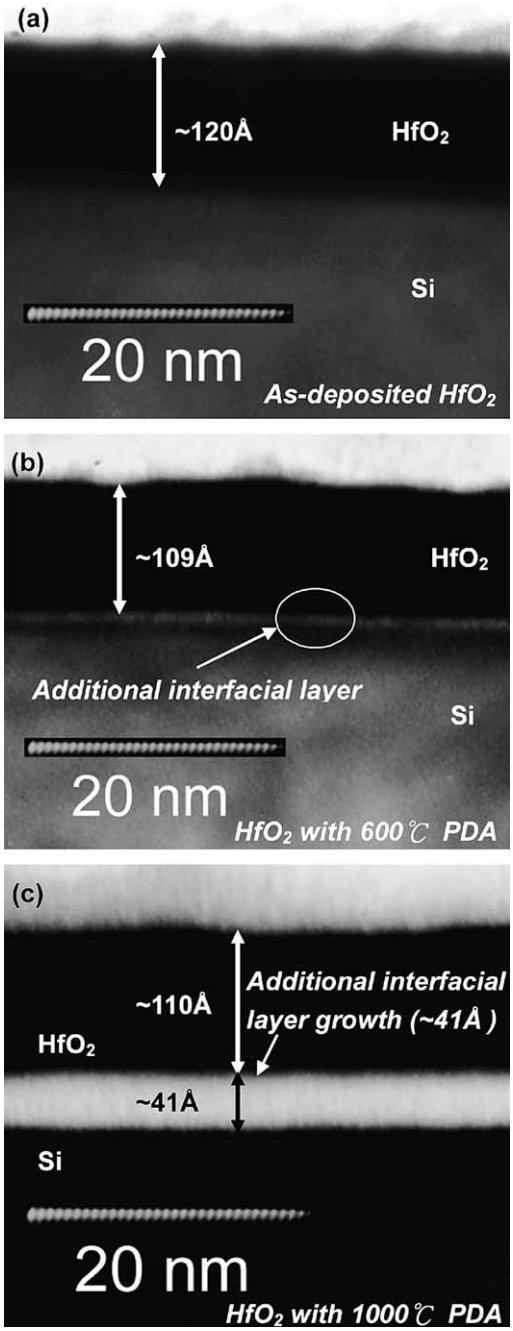

Fig. 4. Transmission electron microscopy (TEM) of HfO_2 samples with various PDA temperatures: (a) As-deposited HfO_2; (b) HfO_2 with 600 °C PDA; and (c) HfO_2 with 1000 °C PDA.

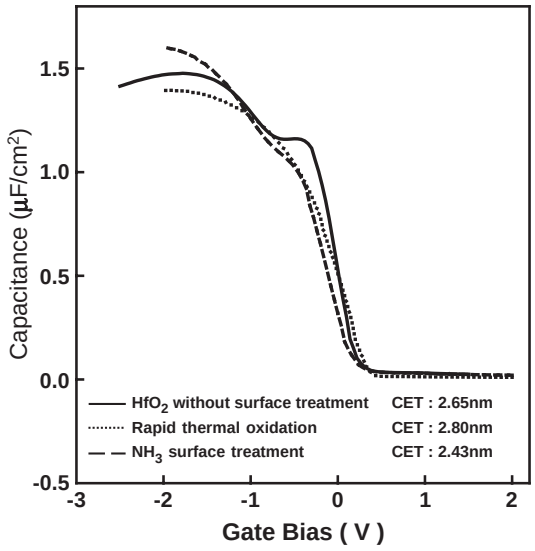

Fig. 5. C–V curves of RTO and NH_3 surface treatment.

annealed samples. Fig. 9(a) shows the comparison of the electron trapping effects under high electric field stress. Electron trapping effects were observed in all samples, but a more extensive electron trapping effect was observed in the HfO_2 samples without surface treatment. In Fig. 9(b), the change in the leakage current after a high electric field stress is demonstrated. The electron trapping effect in RTO or NH_3 treated samples was not as severe when compared to samples without surface treatment.

3.4. Carrier conduction mechanism

Among electrical characteristics, the carrier conduction mechanism in the insulator was worthy enough to be measured. Typically, two possible mechanisms are explored in the metal–insulator interface: Schottky emission and Frenkel–Poole emission [5]. The Schottky–Richardson emission, generated by the thermionic effect, is caused by electron transport across the potential energy barrier via

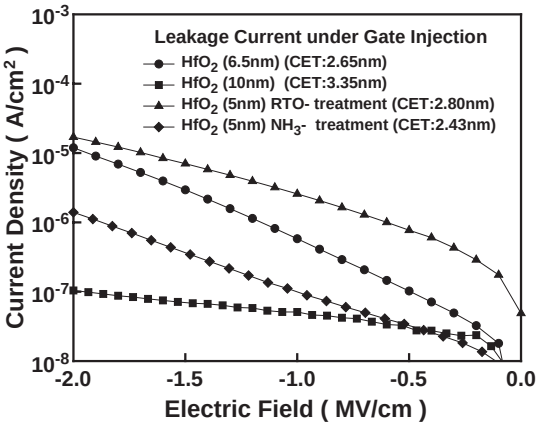

Fig. 6. J–E curves of RTO and NH_3 surface treatment.

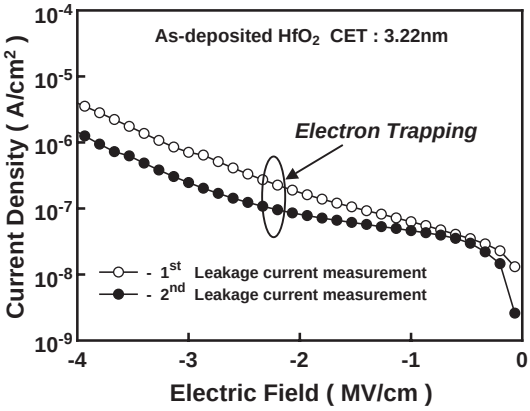

Fig. 7. Leakage current after gate injection stress of as-deposited HfO_2 samples. The electron trapping effect can be observed.

field-assisted lowering at a metal–insulator interface. The leakage current equation is as follows:

$$J = A^* T^2 \exp\left(\frac{\beta_s E^{1/2} - \phi_s}{k_B T}\right) \quad (1)$$

where $\beta_s=(e^3/4\pi\varepsilon_0\varepsilon)^{1/2}$, A^* is the effective Richardson constant, and ϕ_s is the contact potential barrier. The slope can be extracted in $\ln J$ vs. $E^{1/2}$ plots.

$$\ln J = \frac{\beta_s}{k_B T}\sqrt{E} + \left[\ln\left(A^* T^2\right) - \frac{\phi_s}{k_B T}\right]$$

$$slope = \frac{\beta_s}{k_B T}. \quad (2)$$

The Frenkel–Poole emission is due to field-enhanced thermal excitation of trapped electrons in the insulator into the conduction band. The leakage current equation is as follows:

$$J = J_0 \exp\left(\frac{\beta_{FP} E^{1/2} - \phi_{FP}}{k_B T}\right) \quad (3)$$

where $J_0=\sigma_0 E$ is the low-field current density, σ_0 is the low-field conductivity, $\beta_{FP}=(e^3/4\pi\varepsilon_0\varepsilon)^{1/2}$, e is the elec-

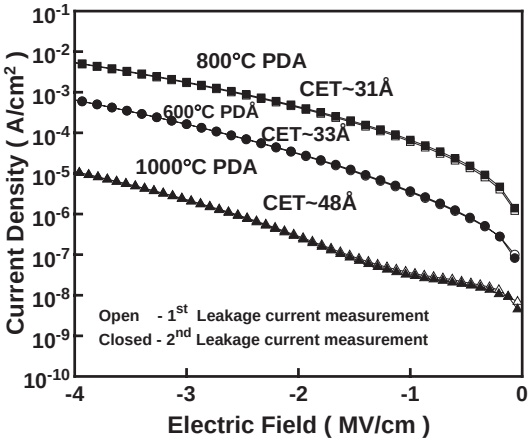

Fig. 8. Leakage current after gate injection stress of HfO_2 with various PDA temperatures. Electron trapping was eliminated after annealing.

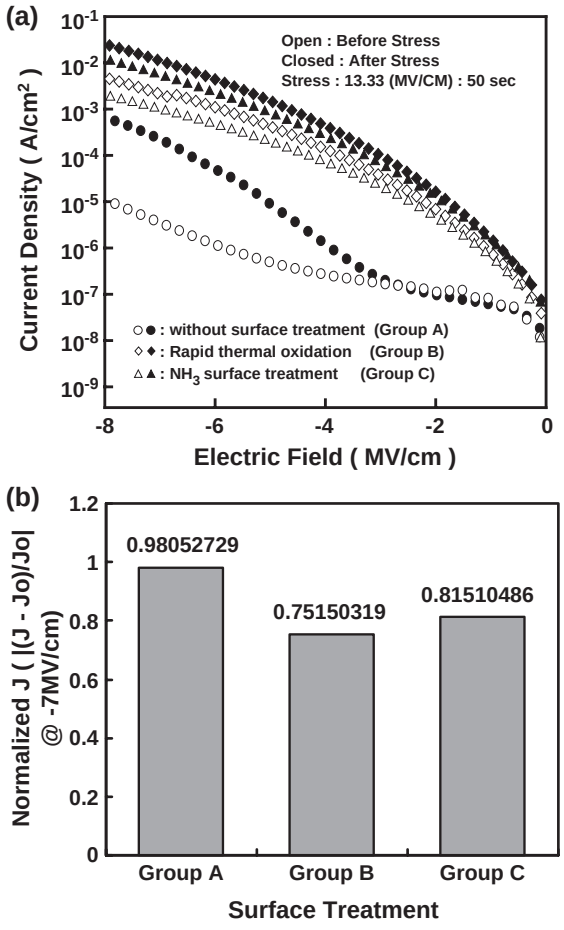

Fig. 9. (a) The comparison of the electron trapping effect under high electric field stress. Severe electron trapping was observed in HfO_2 samples without surface treatment. (b) The change of the leakage current after the high electric field stress. (Group A: without surface treatment, Group B: RTO, Group C: NH_3 surface treatment. J and J_0 are the leakage current before and after electric stress, respectively.)

tronic charge, ε_0 is the permittivity of free space, ε is the high frequency relative dielectric constant, T is the absolute temperature, E is the applied electric field, K_B

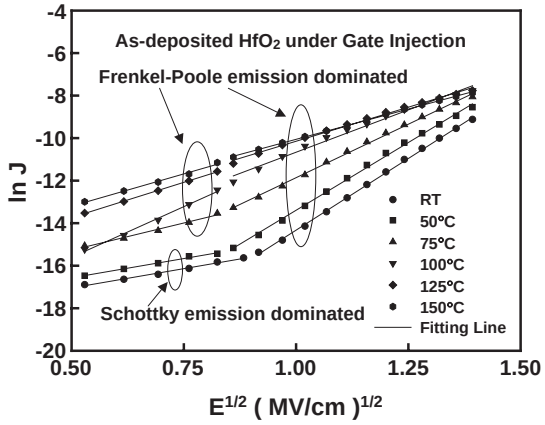

Fig. 10. Conduction mechanism fitting of as-deposited HfO_2 samples under gate injection.

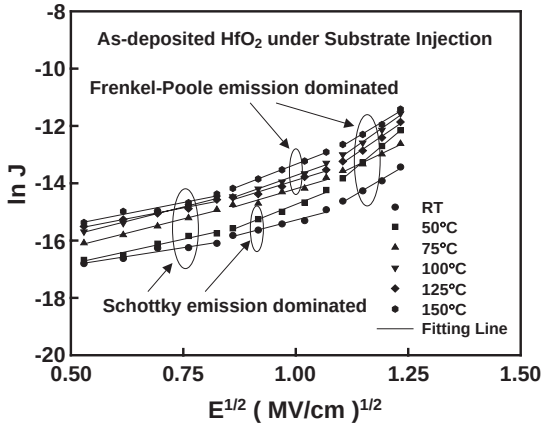

Fig. 11. Conduction mechanism fitting of as-deposited HfO_2 samples under substrate injection.

is the Boltzmann constant, and ϕ_{FP} is the contact potential barrier.

The slope can be extracted in ln J vs. $E^{1/2}$ plots.

$$\ln J = \frac{\beta_{\mathrm{FP}}}{k_{\mathrm{B}}T}\sqrt{E} + \left[\ln(J_0) - \frac{\phi_{\mathrm{FP}}}{k_{\mathrm{B}}T}\right]$$

$$slope = \frac{\beta_{\mathrm{FP}}}{k_{\mathrm{B}}T}. \tag{4}$$

From the above equations, the leakage current behaviors of insulating films can be investigated further by the current density (J)–electric field (E) characteristics, such as ln J vs. $E^{1/2}$ plots. It is found that the leakage current density is linearly related to the square root of the applied electric field. The linear variations of the current correspond either to the Schottky emission or to the Frenkel–Poole conduction mechanism [6]. For trap states with coulomb potentials, the expression is virtually identical to that of the Schottky emission. The barrier height, however, is the depth of the trap potential well, and the quantity β_{FP} is larger than in the case of the Schottky emission by a factor of 2. Distinguishing between the two processes can be done by comparing the theoretical value of β with the obtained experimental values through the calculating of the slope in the ln$J$-$E^{1/2}$ curves. The dielectric constant of HfO_2 is 13 extracted by C–V measurement, and the theoretical β values are 3.36×10^{-23} for the Frenkel–Poole and 1.68×10^{-23} for the

Table 1
β value extracted from this experiment

Gate injection	Substrate injection
β at room temperature (RT) : 5.58×10^{-23}	β at room temperature (RT) : 1.69×10^{-23}
β at 50 °C : 5.71×10^{-23}	β at 50 °C : 2.80×10^{-23}
β at 75 °C : 4.86×10^{-23}	β at 75 °C : 2.22×10^{-23}
β at 100 °C : 4.12×10^{-23}	β at 100 °C : 2.86×10^{-23}
β at 125 °C : 3.54×10^{-23}	β at 125 °C : 2.67×10^{-23}
β at 150 °C : 3.34×10^{-23}	β at 150 °C : 3.57×10^{-23}

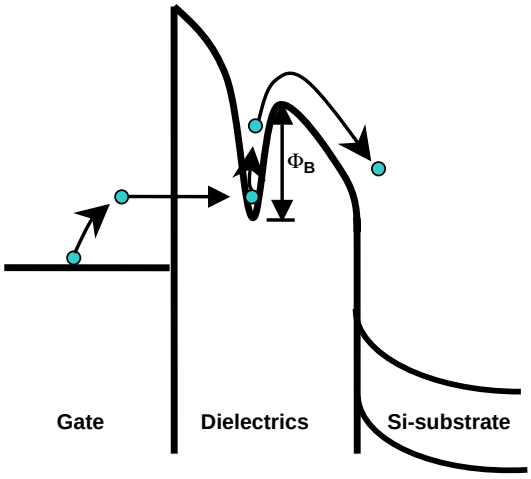

Fig. 12. Schematic band diagram of Frenkel–Poole emission.

Schottky emission. Figs. 10 and 11 show the curve-fitting results of the As-deposit HfO_2 samples under gate and substrate injection. From the slopes of the fitted curves, the experimental β value was extracted and is shown in Table 1.

In the cases of gate and substrate injection, the conduction mechanism in as-deposited HfO_2 thin film is dominated by the Schottky emission in a lower electric field, and by the Frenkel–Poole emission in a higher electric field. When the samples are under a higher electric field, the tunneling effect becomes obvious. [7,8] This tunneling effect enhances the Frenkel–Poole emission. A schematic band diagram of the Frenkel–Poole emission is shown in Fig. 12. Therefore, it can be concluded that the conduction mechanism in a higher electric field is evidently dominated by the Frenkel–Poole emission. In addition, the interfacial layer grew after the PDA treatments, as shown in Fig. 4. The interface changed to the SiO_2-like or silicate-like layer [9,10], and has a sufficient barrier height to suppress the Schottky emission, resulting in the conduction mechanism of the HfO_2 thin film being dominated by the Frenkel–Poole emission in a high electric field.

4. Conclusions

In closing, the thermal stability of the high dielectric constant material HfO_2, deposited by MOCVD was investigated under various high temperature PDA treatments. It was found that a higher annealing temperature leads to higher leakage current. Since the higher PDA temperature makes the dielectric materials crystallize, it contributes to a larger leakage current. For the 1000 °C-annealed sample, the thicker interfacial layer helps resist a large leakage current, and consequently reduces it. The NH_3 surface treatment not only improved the C–V curves, but also reduced the leakage current. The NH_3 pre-treatment provides strong Si–N bonds and a sufficient barrier height for the interfacial layer to suppress the leakage current. The as-deposited HfO_2 thin film without any PDA treatment has considerable initial traps and a severe electron trapping effect. This electron trapping effect can be suppressed by high temperature annealing. Rapid thermal oxidation and NH_3 surface treatments can also improve the electron trapping effect in the HfO_2 film. It was also found that the conduction mechanism in the HfO_2 thin film is dominated by the Frenkel–Poole emission in a high electric field.

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