ESD Protection Design for 1- to 10-GHz Distributed Amplifier in CMOS Technology

Ming-Dou Ker, *Senior Member, IEEE*, Yuan-Wen Hsiao, *Student Member, IEEE*, and Bing-Jye Kuo

***Abstract*—Two distributed electrostatic discharge (ESD) protection schemes are presented and applied to protect distributed amplifiers (DAs) against ESD stresses. Fabricated in a standard 0.25-μm CMOS process, the DA with the first protection scheme of the equal-sized distributed ESD (ES-DESD) protection scheme, contributing an extra 300 fF parasitic capacitance to the circuit, can sustain the human-body model (HBM) ESD level of 5.5 kV and machine-model (MM) ESD level of 325 V and exhibits the flat-gain of 4.7 $\pm$1 dB from 1 to 10 GHz. With the same amount of parasitic capacitance, the DA with the second protection scheme of the decreasing-sized distributed ESD (DS-DESD) protection scheme achieves better ESD robustness, where the HBM ESD level over 8 kV and MM ESD level is 575 V, and has the flat-gain of 4.9$\pm$1.1 dB over the 1 to 9.2-GHz band. With these two proposed ESD protection schemes, the broad-band RF performances and high ESD robustness of the DA can be successfully codesigned to meet the application specifications.**

***Index Terms*—Decreasing-sized distributed ESD (DS-DESD), distributed amplifier (DA), electrostatic discharge (ESD), equal-sized distributed ESD (ES-DESD), resistive ladder.**

I. Introduction

DISTRIBUTED broad-band amplifiers have many applications, such as television, pulsed radars, and broad-band optical communication. Distributed amplifiers (DAs) employ a topology where the capacitance contributed by the gain stages are separated, but the output currents still combine together. Inductive elements are used to separate and compensate the capacitances at the inputs and outputs of adjacent gain stages. The combination of series inductive elements and shunt capacitances forms a lumped artificial transmission line with specific characteristic impedance. The value of the characteristic impedance can be adjusted according to the terminal impedance to achieve good matching over a very wide bandwidth.

Early DAs were implemented by using vacuum tubes and high-speed GaAs MESFETs [1]–[6]. Recently, DAs were also realized in CMOS technology and reported for the advantages of both a lower cost and a potentially higher state of integration [7]–[13]. The advantage of an integrated DA would be the capability to use arbitrary line impedances instead of the typical 50-Ω interface. A DA utilizing parasitic packaging and bondwire inductors has been realized in a 0.8-μm CMOS process to achieve a gain of 5$\pm$1.2 dB over the 300-kHz to 3-GHz band [7]. Implemented in a 0.6-μm CMOS process, a fully integrated DA using on-chip planar square inductors has achieved a measured passband gain of 6.1 dB from 0.5 to 4 GHz with 5.5-GHz unity-gain frequency [8]. Besides, a fully differential DA in the same process has performed 5.5-dB passband gain from 0.5 to 7.5 GHz and 8.5-GHz unity-gain frequency [9]. A three-stage DA designed with coplanar strip lines has achieved a low-frequency gain of 5 dB and the unity-gain frequency of 15 GHz in a 0.18-μm CMOS process [10]. Two DAs employing high impedance coplanar waveguides as inductive elements has shown 8- and 10-dB gains up to 10 GHz, respectively [11]. Using the cascade topology, another two broad-band CMOS DAs fabricated in a 0.18-μm CMOS process were reported with 7.3$\pm$0.8 dB gain from 0.6 to 22 GHz [12], and 10.6$\pm$0.5 dB gain over the 0.5- to 14-GHz bandwidth [13], respectively. The operating frequencies of DAs have been going higher and the gains have been elevated larger. However, electrostatic discharge (ESD) protection, which is a very important reliability issue in IC fabrication, is neither considered nor mentioned in those works.

Recently, broad-band ESD protection schemes were reported in several previous works [14]–[16]. A distributed ESD protection scheme using transmission lines to match the capacitances of the ESD protection devices had been demonstrated [14]. The quantitative calculation to analyze the performance degradation of the RF circuits due to ESD protection had been discussed [15]. Another broad-band technique by using monolithic T-coils to match the parasitic capacitance of the ESD protection elements had been reported [16].

In this paper, the DAs codesigned with two new proposed ESD protection schemes are proposed and verified in a standard 0.25-μm CMOS process. By dividing one ESD protection device into several equal-sized parts and placing each of them before each gain stage, the first ESD protection scheme is called the equal-sized distributed ESD (ES-DESD) protection. Applied in DAs, the second ESD protection schem [the decreasing-sized distributed ESD (DS-DESD) protection] divides one large ESD protection device into several parts with different sizes, and allocates them from input port to the gate-line terminal with descending sizes. The broad-band performances and ESD robustness of the DA without ESD protection and DAs with ES-DESD or DS-DESD protection schemes have been verified and compared in this work [17].

II. Distributed Amplifier

A. Simple DA Structure

A simple DA structure is shown in Fig. 1. To be fabricated in a standard 0.25-μm CMOS process with five-layer Al-metal

Manuscript received January 17, 2005; revised March 31, 2005. This work was supported by National Science Council (NSC), Taiwan, R.O.C., under Contract NSC93-2215-E-009-014.

M.-D. Ker and Y.-W. Hsiao are with the Nanoelectronics and Gigascale Systems Laboratory, Institute of Electronics, National Chiao-Tung University, Hsinchu 300, Taiwan, R.O.C. (e-mail: mdker@ieee.org).

B.-J. Kuo is with the MediaTek Incorporation, Hsinchu 300, Taiwan, R.O.C.

Digital Object Identifier 10.1109/TMTT.2005.854208

0018-9480/$20.00 © 2005 IEEE

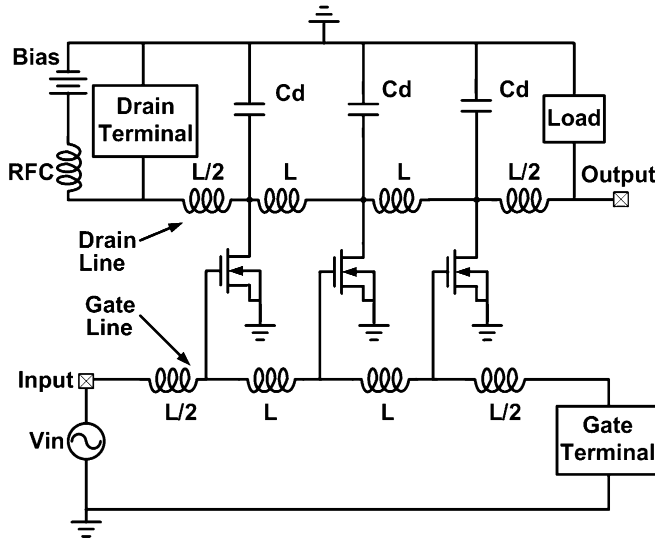


Fig. 1. Basic scheme of the DA.

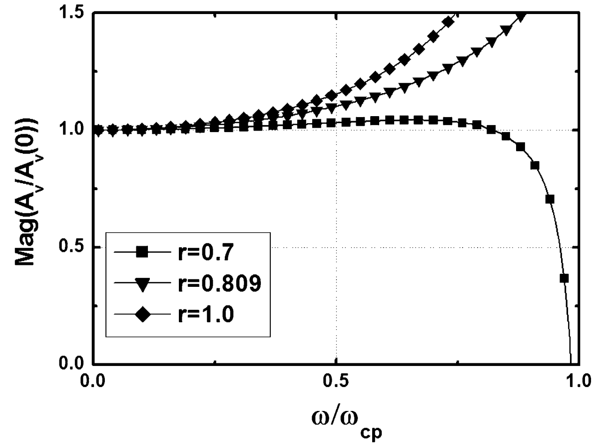


Fig. 2. Normalized gain response of the DA under different staggering factors, where $r = 1$ corresponds to the unstaggered case.

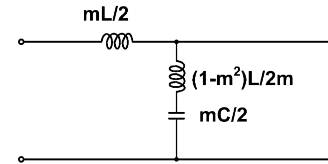


Fig. 3. Low-pass m-derived half section.

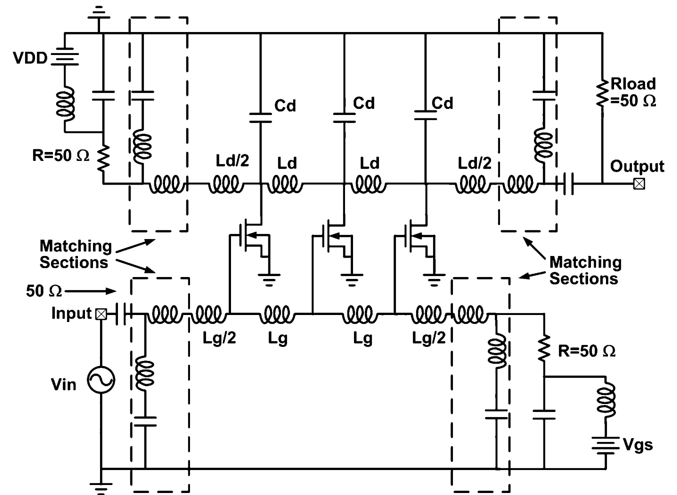


Fig. 4. Modified DA with staggering technique and m-derived half section.

interconnects, this DA will be codesigned with the distributed ESD protection scheme. A three-stage DA with a flat gain of 5 dB over a 10-GHz bandwidth was expected to be achieved. The number of stages was decided according to the consideration of the layout area, the inductor loss, and the power consumption. The input and output were matched to 50 Ω, and the phase shift was designed to be approximately linear over the passband. The supply voltage of the DAs in the 0.25-μm CMOS process is 2.5 V.

The gate-inductors and the parasitic gate-capacitances form the artificial gate-line. Similarly, the drain-inductors and the drain-capacitances construct the artificial drain-line. The cutoff frequency of the artificial transmission line is defined as $\omega_c = 2/\sqrt{LC}$. According to the circuit structure shown in Fig. 1, a peak in the gain response will appear near the cutoff frequency of the transmission line. Since a flat gain response across the passband is preferred, this effect should be reduced. The staggering technique [18] was employed in this design. The dependence of the gain response of the DA on the staggering factor is shown in Fig. 2. Defined as the ratio of the drain-line to the gate-line cutoff frequencies, the staggering factor of about 0.7 has been analyzed as the optimum value from Fig. 2, [18].

The impedance looking into the termination of the L–C artificial transmission line (Z_{oT}) can be expressed as

$$Z_{oT} = \sqrt{\frac{L}{C}\left(1 - \frac{\omega^2 LC}{4}\right)} = \sqrt{\frac{L}{C}\left(1 - \frac{\omega^2}{\omega_c^2}\right)} \quad (1)$$

The L, C, and ωc are the inductance, capacitance, and cutoff frequency of the L–C artificial transmission line, respectively. The impedance looking into the L–C artificial transmission line will exhibit a strong deviation from the nominal impedance near the line's cutoff frequency. One way to realize the image-impedance match is to insert m-derived half sections between the lines and each termination or each port [19]. Such half sections can greatly improve the impedance match. The m-derived half circuit is illustrated in Fig. 3, where the optimum value of $m = 0.6$ is applied to this DA circuit. With the combination of the staggering technique and the m-derived half section, the basic DA is modified and shown in Fig. 4.

B. Ideal DA

With the given topology and the design specifications, the circuit parameters can be obtained. After some minor tuning based on those component values in the given CMOS process, the DA circuit schematic is shown in Fig. 5 with the matching component values. The additional capacitance has been added to fulfill the required Cd value in Fig. 4. The simulated result of S21-parameter of this DA is shown in Fig. 6, where it performs approximately 5.1±0.3 dB over 16 GHz. The simulated results of RF performance on S11-, S22-, and S12-paremeter almost achieve the value below -10 dB over 16 GHz, as shown in Fig. 6. The

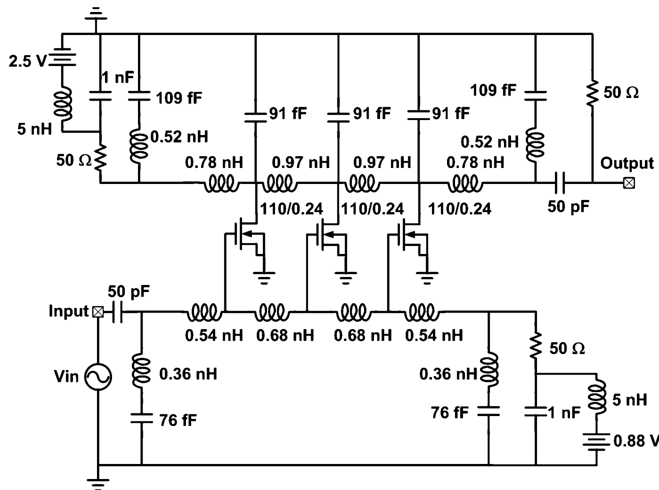


Fig. 5. Initial DA according to the theorems.

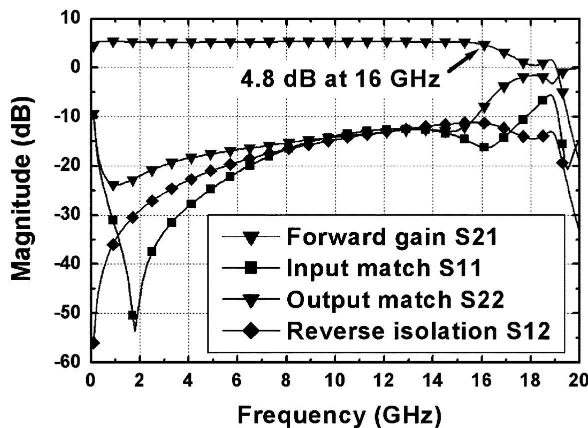


Fig. 6. Simulated results of RF performance on S21-, S11-, S22-, and S12-parameters of the initial DA in Fig. 5.

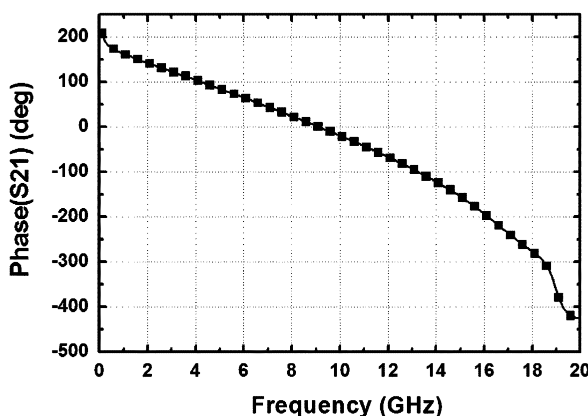


Fig. 7. Simulated phase shift of S21-parameter of the initial DA in Fig. 5.

simulated phase shift of the S21-parameter in Fig. 7 is approximately linear, which means the time delay is almost constant over the bandwidth from 0.5 to 18 GHz. As observed, the simulated results fit well to the conventional theory. However, with the consideration of the parasitics of the passive components, especially the on-chip spiral inductors, the situation could be different.

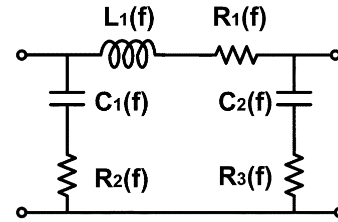


Fig. 8. Frequency-dependent π-model of on-chip inductor.

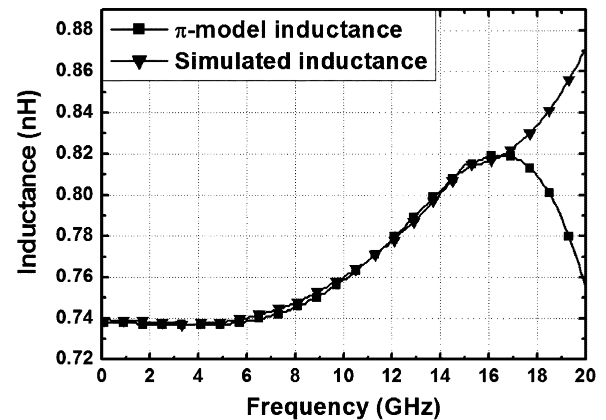


Fig. 9. Comparison of inductance among the lumped π-model and the simulated spiral inductor.

C. Inductor Modeling

Due to the mutual influences among the components, to optimize a DA with physical components becomes a complicated design cycle. Because of the complexities, an auto-optimization solution is employed. To utilize this solution, the passive component models need to be constructed first. Among those passive components, on-chip spiral inductors are the most important and critical for the complicated parasitic effects. Thus, an on-chip spiral inductor library should be built up first.

The method to generate inductor models is a combination of the analytic methods, measured data, simulated data, and some other techniques [20], [21]. In this work, six on-chip spiral inductors have been generated by the lumped π-model shown in Fig. 8 and modeled from 1 to 3.5 turns with the step of 0.5 turn. The basic structures, including the inner radius of 55 μm, top metal width of 10 μm, and the spacing between two metals of 2 μm, of these inductors were kept the same. The inductance curve of the lumped model, illustrated in Fig. 9, fits well to the simulation curve of the on-chip spiral inductor up to 16 GHz. Therefore, these lumped models can still be employed to replace the simulated spiral inductors for optimizing the RF performance of the DA.

D. Optimized DA

After building an on-chip spiral inductor library, the auto-optimization can be operated in the ADS simulator. A general DA structure was set up as that in Fig. 5, with all variable passive component values. Then, the optimization targets were set up in the EM simulator. First, the S-parameters except S21-parameter were chosen to be less than -10 dB over the 16-GHz bandwidth. The forward gain S21 was kept more than 5 dB over the

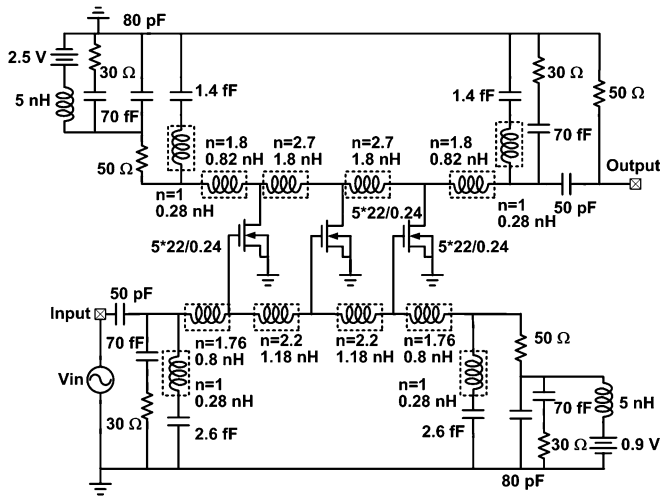


Fig. 10. Randomly optimized DA.

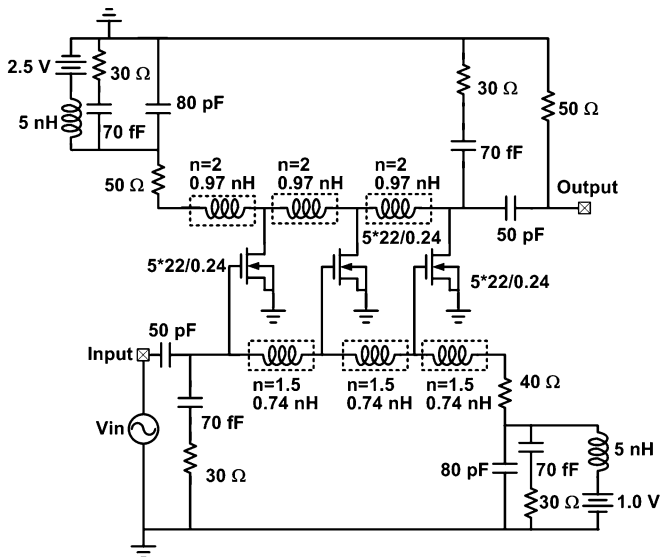


Fig. 11. Feasibly optimized DA.

same bandwidth. Second, the difference of the time delay over the 16-GHz bandwidth was controlled to the minimum. The inductor model can be adjusted by changing the turns. The DA is kept in optimization cycles until these goals can not be approached. The optimized structure with the component values is shown in Fig. 10. Observed in Fig. 10, the turns of the inductors were random values between 1 and 3.5, which were difficult to be implemented in physical design. So, we had to reoptimize the circuit with the feasible turn values which are between 1 and 3.5 with the step of 0.5. After replacing the ideal inductors with the feasible on-chip spiral inductors, the feasible DA is shown in Fig. 11. The m-derived half sections were removed, for the reason that the on-chip inductors could not reach the arbitrary turns required in the optimization process. Without the m-derived half sections, the S21-parameter does not attenuate very rapidly around the cutoff frequency compared to the ideal-inductor one and the randomly optimized one, as shown in Fig. 12.

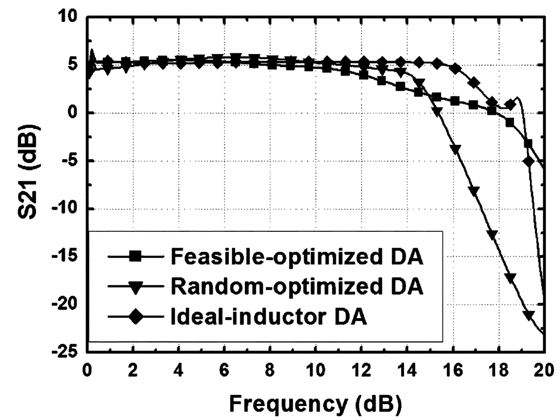


Fig. 12. Comparison of S21-parameters among the feasibly optimized, randomly optimized, and ideal-inductor DAs.

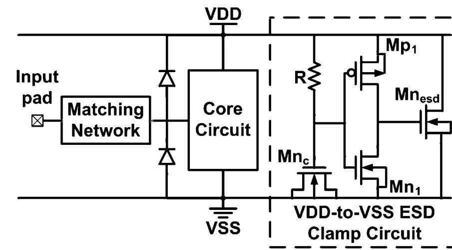


Fig. 13. Traditional ESD protection design with a pair of diodes connected to the input pad and a VDD-to-VSS ESD clamp circuit.

For the area saving and the simplicity to compare the DAs with different ESD protection schemes, the performance of the feasible DA in such a 0.25-μm CMOS process was acceptable.

III. Distributed Amplifier With ESD Protection Design

A. *Concept of Distributed ESD Protection*

The ESD protection is very important during IC manufacturing. Since the DA is the front-end of the whole system, the ESD protection is indispensable. The parasitic capacitance and resistance from the ESD protection circuit will degrade the performance of DA in impedance match and noise figure. To avoid these, the ESD protection components should be built with low capacitances and high Q factors. The shallow-trench-isolated (STI) diodes fit these two requirements [22]. Besides, they can sustain a very high ESD protection level with the cooperation of a turn-on efficient VDD-to-VSS ESD clamp circuit [23]. However, the broad-band matching over 10 GHz is infeasible with the traditional ESD protection scheme [24], which uses a pair of diodes connected to the input pad with a VDD-to-VSS ESD clamp circuit, as shown in Fig. 13. To achieve a comparable broad-band input match of the DA after inserting the ESD protection circuit, the ESD protection components must be separated as the MOSFETs in the DA. The extra parasitic capacitance of each ESD protection component can be absorbed into each section of the artificial gate-line. Hence, the value of the characteristic impedance in each section changed little and the matching condition can still be maintained.

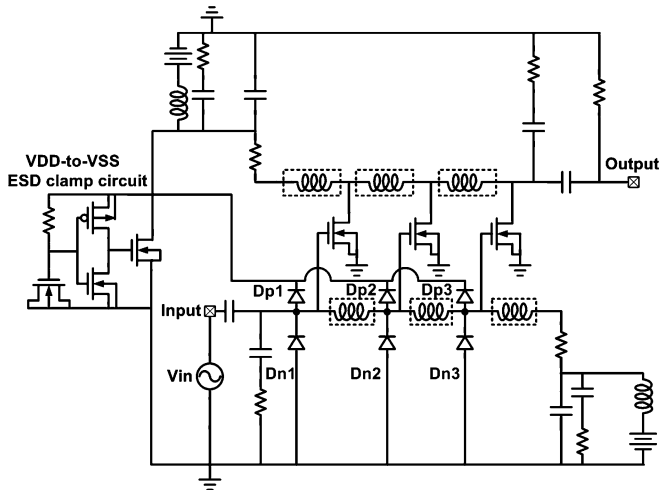


Fig. 14. DA with distributed ESD (DESD) protection circuit. The dimensions of the devices in DA are the same as those in Fig. 11.

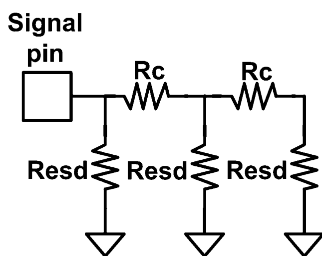


Fig. 15. Resistive ladder model of the DESD protection circuit during the ESD event.

B. New Proposed Distributed ESD Protection Circuits

According to the distributed ESD topology in [15], a DA is codesigned with the ES-DESD protection scheme, as shown in Fig. 14. The STI diodes, used as ESD protection devices, were divided into three sections with equal sizes to conform to the gain stages of the DA. With the turn-on-efficient VDD-to-VSS ESD clamp circuit, the DA with the ES-DESD protection scheme was supposed to have high ESD robustness. Under the ESD stress, the DA with ES-DESD protection can be approximately modeled as a simple resistive ladder [14], as shown in Fig. 15, where Rc denotes the series resistance of the spiral inductor and Resd is the equivalent turn-on resistance of the ESD diode. The large values of Rc and Resd degraded the ESD robustness when the ESD-generated heat across them. Therefore, in order to enhance the ESD robustness, the Resd and Rc should be minimized. According to this consideration, the decreasing-sized distributed ESD (DS-DESD) protection scheme is proposed. The new proposed DS-DESD protection scheme by enlarging the size of ESD protection devices at the first ESD protection stage can reduce the Resd of the first stage, where is usually the most possible location to be damaged by ESD. With a relatively large device size at the first ESD protection stage, it can discharge ESD current more quickly at the first ESD protection stage, as compared to the ES-DESD protection scheme. Thus, the DA with the new proposed DS-DESD protection is believed to have better ESD robustness, as compared to that of the DA with the ES-DESD protection.

TABLE I
COMPONENT VALUES IN THE ESD PROTECTION CIRCUITS

	Circuit name	Matching type	Dp1+Dn1 (fF)	Dp2+Dn2 (fF)	Dp3+Dn3 (fF)
Group 1	DA1	ES-DESD	100	100	100
	DA2	DS-DESD	200	75	25
Group 2	DA3	ES-DESD	200	200	200
	DA4	DS-DESD	400	150	50

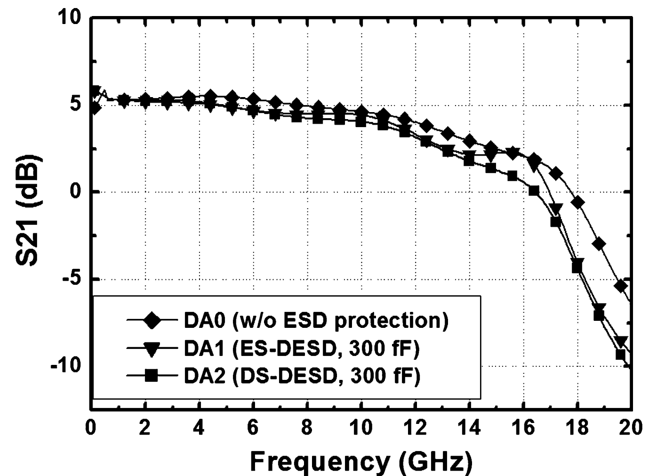


Fig. 16. Simulated results of RF performance on S21-parameters of the DAs without and with the distributed ESD (DESD) protection circuits. The total parasitic capacitance of all ESD diodes is 300 fF.

C. Broad-band Performance of DA Without and With ESD Protection

For a broad-band circuit, the S-parameters, the noise figure, and the phase shift are the main factors to determine the RF performance. The simulations of the DA without the ESD protection and the DAs with the ES-DESD protection or DS-DESD protection were operated to examine how much the degradation of the performance would be after inserting the ESD protection circuit into the DA.

In the ES-DESD and DS-DESD protection schemes, two amounts of the total parasitic capacitances contributed by all the ESD protection diodes were chosen. The first amount was 300 fF and the second one was 600 fF. The parasitic capacitances of the ESD protection diodes in these ESD protection circuits are listed in Table I.

In the first group, S21-parameters and the phase shifts of the DA0 (DA without the ESD protection), DA1 (ES-DESD protection with 300 fF), and DA2 (DS-DESD protection with 300 fF) were compared in Figs. 16 and 17, respectively. As seen from Fig. 16, DA0 had the best performance, and DA2 had the worst frequency response among these three circuits. However, the difference of the passband-gain among these three circuits was small. The phase shifts of these three types of DAs in Fig. 17 were three straight lines from low frequency to about 14 GHz, which had no apparent difference.

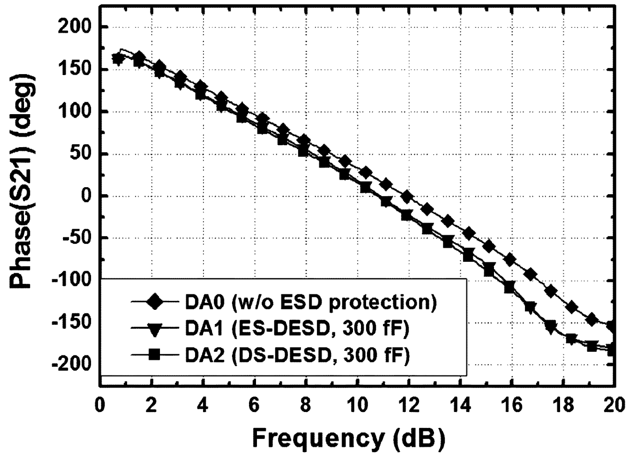


Fig. 17. Simulated phase shifts of the DAs without and with the distributed ESD (DESD) protection circuits. The total parasitic capacitance of all ESD diodes is 300 fF.

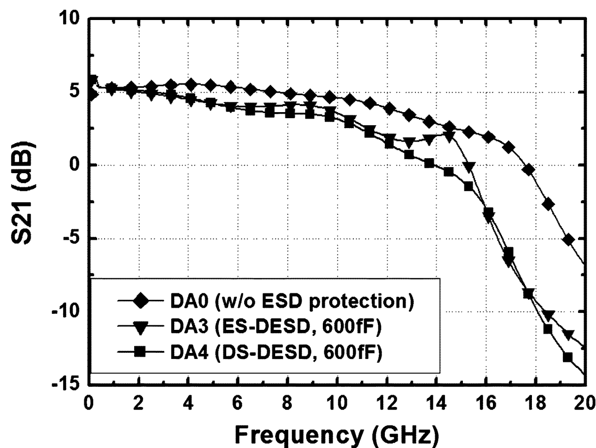


Fig. 18. Simulated results of RF performance on S21-parameters of the DAs without and with the distributed ESD (DESD) protection circuits. The total parasitic capacitance of all ESD diodes is 600 fF.

In the second group, the total parasitic capacitance was twice the amount of the first group. Hence, the S21-parameters of DA3 (ES-DESD protection with 600 fF) and DA4 (DS-DESD protection with 600 fF) degraded more seriously than those of DA1 and DA2 in the first group, as shown in Fig. 18. Still, the DA with the DS-DESD protection had the worst frequency response. The phase shifts of the circuits in the second group were compared in Fig. 19. The phase shifts of DA3 and DA4 were less linear than those of DA1 and DA2 because of the larger parasitic capacitances contributed by the ESD protection circuits. From the simulation results, to provide the distributed ESD (DESD) protection to a DA and to take care of the broad-band performance simultaneously, the sizes of the ESD diodes can not be too large. Thus, the DAs with the DESD protection scheme in the first group with total parasitic capacitance of 300 fF (contributed by ESD protection diodes) were preferred.

IV. Experimental Results

One DA without ESD protection (DA0) and five DAs with ESD protection circuits have been fabricated in a standard

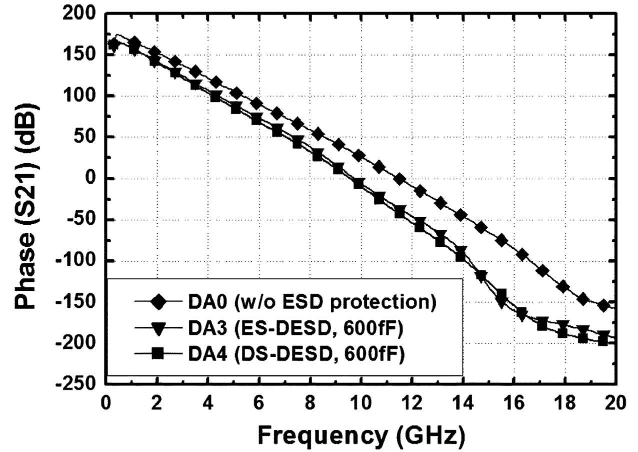


Fig. 19. Simulated phase shifts of the DAs without and with the distributed ESD (DESD) protection circuits. The total parasitic capacitance of all ESD diodes is 600 fF.

TABLE II
Parasitic Capacitances of the ESD Protection Diodes in the Fabricated DAs With ESD Protection

DA with ESD protection	Matching type	Dp1+Dn1 (fF)	Dp2+Dn2 (fF)	Dp3+Dn3 (fF)
DA1	ES-DESD	100	100	100
DA2	DS-DESD	200	75	25
DA3	ES-DESD	200	200	200
DA4	DS-DESD	400	150	50
DA5	ES-DESD	300	300	300

0.25-μm CMOS process. The parasitic capacitances contributed by the ESD protection diodes in the five DAs with ESD protection are listed in Table II. The die photo of these fabricated DAs is shown in Fig. 20. In the following subsections, the broad-band performances, including the S-parameters, the noise figures, and the phase shifts of these six DAs will be measured and compared. The ESD protection levels of these six DAs will be also tested and compared with failure analysis.

A. Broad-band RF Performance

The S-parameters of these six DAs have been measured on-wafer with two-port ground-signal-ground (G-S-G) probes from 1 to 18 GHz. The 20-GHz S-parameter measurement system (HP85122A) is used to characterize the behavior of the circuits. The S21-parameter of the DA without ESD protection compared to that of the simulated one is shown in Fig. 21. The probed response, shown in Fig. 21, correlates well with the response of the post-simulation, but still some differences exist. The post-simulation was operated with the addition of the interconnects used in layout. The effects of the interconnects were obtained from the EM simulator of ADS momentum. The simulated response is 5 dB with $\pm$ 1-dB flatness from 1 GHz to 10 GHz and a unity-gain frequency of 15.1 GHz. However, the measured response is 5 dB with $\pm$1-dB flatness from 1 to 11.4 GHz and a unity-gain frequency of 16.7 GHz. The deviation of the RF performance can be attributed to several reasons,

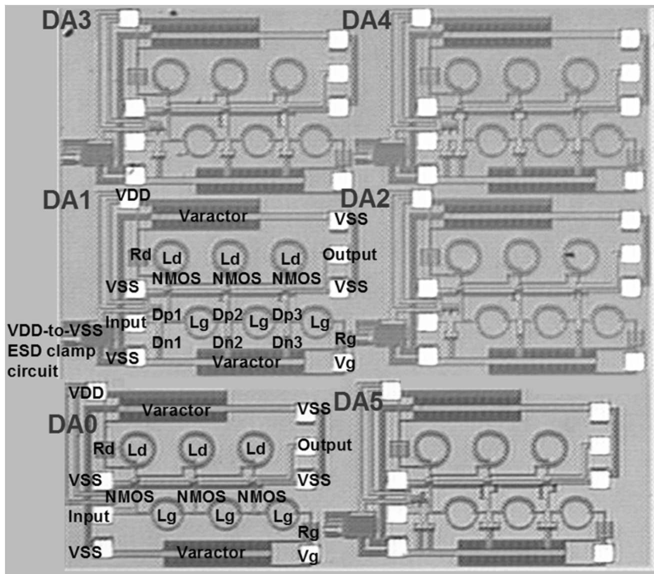


Fig. 20. Die photo of the DAs without and with the ESD protection circuits. The DA1–DA5 have ESD protection, but the DA0 which is a reference for RF performance comparison has no ESD protection.

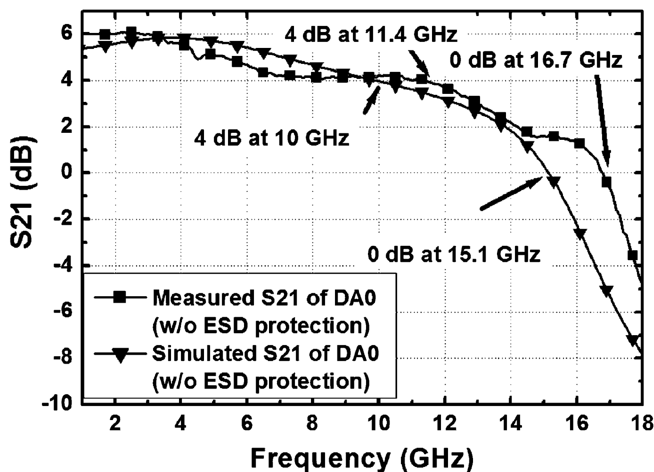


Fig. 21. Measured S21-parameter compared to the post-simulated S21-parameter of the DA without the ESD protection circuit.

including the inaccuracy of the simulated spiral inductors, the temperature coefficients of the resistors, and the imprecise estimation of the pad effects, etc.

The coupling between the inductors was not considered in the circuit design. Since the inductances used in this circuit are quite small, the coupling between the inductors is also rather small. As shown in Fig. 21, there is a slight difference between the simulated and measured broad-band RF performances of the DAs. The measured RF performance is degraded as compared to the simulated one. However, the degradation is fairly slight below the frequency of 14 GHz. Thus, the coupling between the inductors can be ignored without causing major design errors in the target of 1- to 10-GHz DAs.

According to the simulation results of S21-parameters in Figs. 16 and 18, the DA without ESD protection achieves the best gain response among all the DAs. With the same total

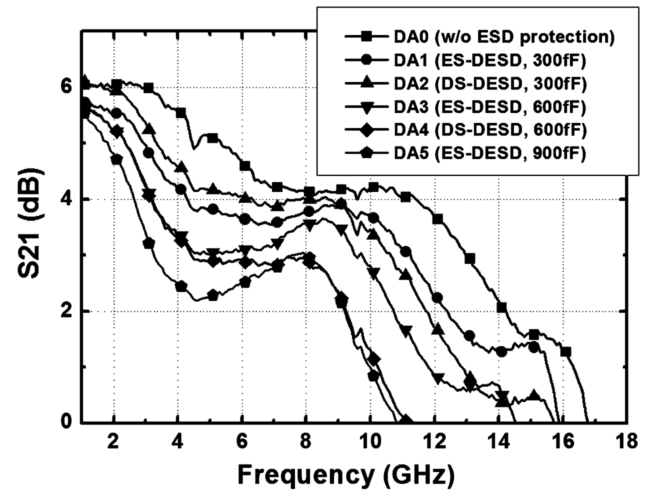


Fig. 22. Comparison of the measured S21-parameters among the DA without ESD protection and the DAs with ESD protection.

parasitic capacitance contributed by ESD protection diodes, the DAs with ES-DESD protection perform better in S21-parameter than the DAs with DS-DESD protection. The measured results of the DA without ESD protection and five DAs with ESD protection, as compared in Fig. 22, conform to the simulated performances with the exception that DA2 achieves a better gain response than DA1. The reason for this measured result is that the decreasing parasitic capacitances of the ESD protection diodes compensating the miller effect in each gain stage with the increasing gain. With the increasing total parasitic capacitance of the ESD diodes in the DAs with ESD protection, the S21-parameters in these DAs are degraded. Hence, only DA1 and DA2 have the comparable performance to DA0.

The S-parameters, except S21, of the simulated and implemented DAs without ESD protection, DA1, and DA2 are shown in Fig. 23(a)–(c). The measured S11-parameter of the DA without ESD protection, as illustrated in Fig. 23(a), corresponds well to the simulated one and meets the specification of less than -10 dB. The measured S11-parameter of DA1 degrades less than that of DA2, but they both do not meet the specification anymore.

As shown in Fig. 23(b) and (c), the measured S22-parameters and S12-parameters of these three implemented circuits exhibit better output matching and reverse isolation than the simulated ones of the DA without ESD protection. As shown in Fig. 24, the simulated and measured phase shifts of the DA without ESD protection both present roughly linear curves from 1 to 16 GHz, but DA1 and DA2 only maintain the same situation up to 14 GHz.

The noise figure was measured by the high frequency modeling system (HP85122A) and the noise parameters extraction software (ATN NP5B) from 1 to 18 GHz. The results are compared in Fig. 25. The measured data of DA0 achieve the lowest value of 4.4 dB at 6 GHz. The lowest value in measurement is larger than that of 3.6 dB in simulation. In DA1 and DA2, the lowest noise figures are 0.5 and 0.6 dB higher than that of the measured DA without ESD protection. It means that the ESD protection diodes contribute extra noise.

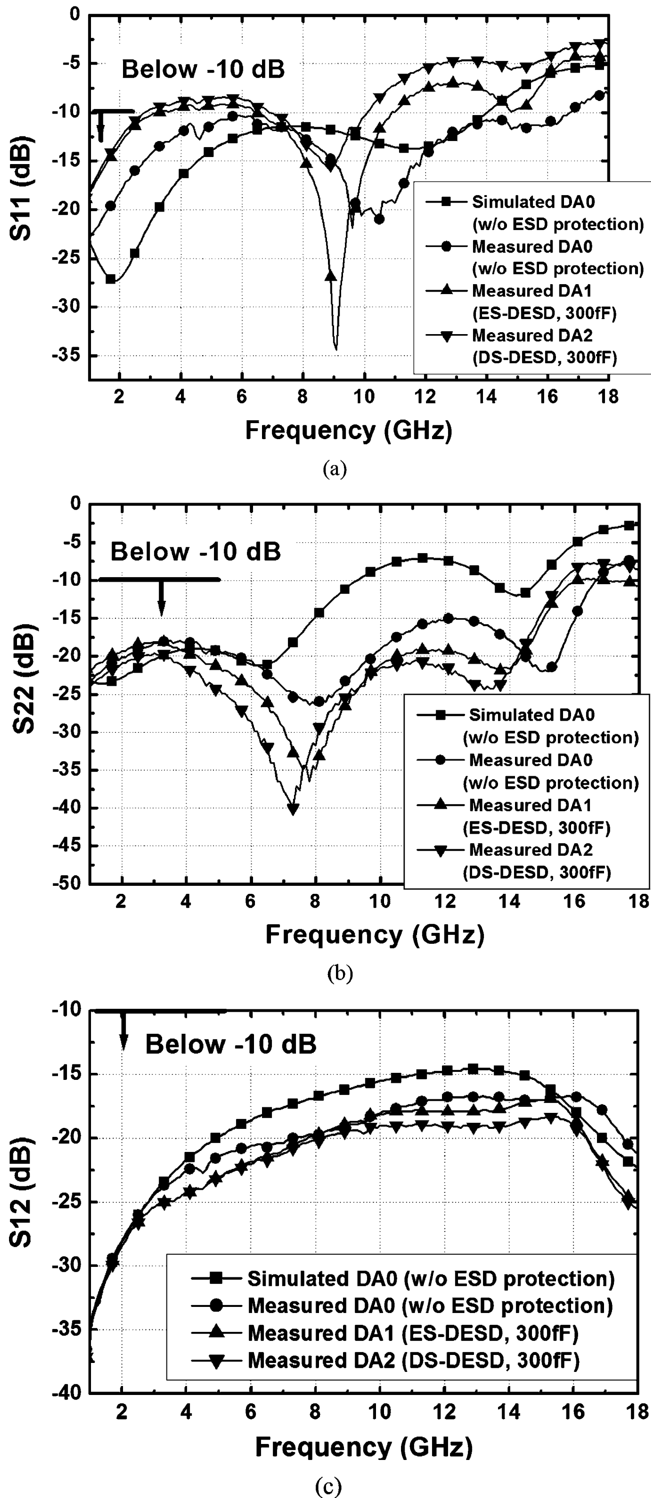


Fig. 23. (a) S11-parameters, (b) S22-parameters, and (c) S12-parameters among the simulated and fabricated DA0s without ESD protection, DA1 with ES-DESD protection, and DA2 with DS-DESD protection.

B. ESD Robustness

To compare the ESD robustness, DA0 (the DA without the ESD protection) and five DAs with ESD protection were tested according to the criterion of 30% *I–V* curve shift at 1-μA current. The results of the human-body model (HBM) [25] ESD stresses and the machine model (MM) [26] ESD stresses are

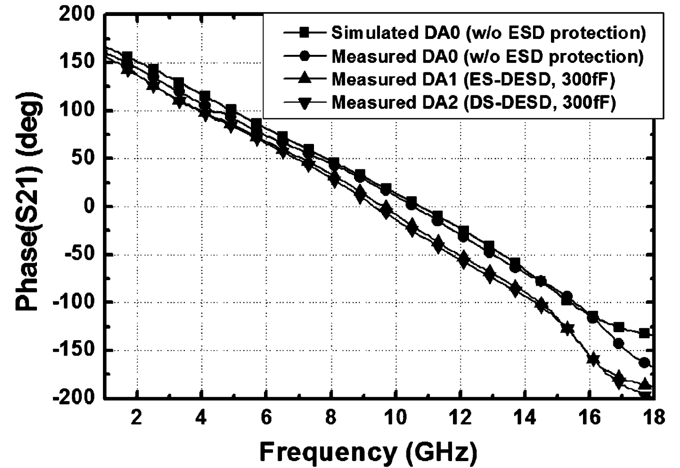


Fig. 24. Phase shifts among the simulated and fabricated DAs without ESD protection, DA1 with ES-DESD protection, and DA2 with DS-DESD protection.

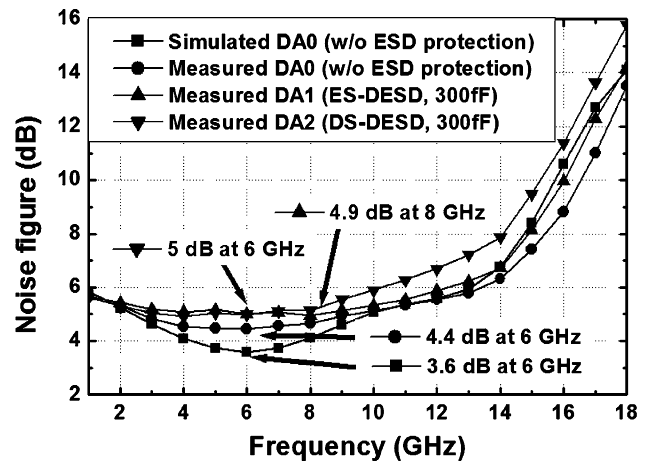


Fig. 25. Noise figures among the simulated and fabricated DAs without ESD protection, DA1 with ES-DESD protection, and DA2 with DS-DESD protection.

shown in Table III. As seen in Table III, the DA without ESD protection only sustains a very low ESD protection level, which is far below the ESD specifications for commercial ICs which are 2 kV in HBM and 200 V in MM.

The ESD robustness of the DA is substantially improved after inserting the distributed ESD protection circuit. The enhancement of ESD robustness is significant in that DA1 (employing the ES-DESD protection scheme) achieves the HBM ESD level of 5.5 kV and the MM ESD level of 325 V. Furthermore, equipped with the equally total parasitic capacitance of ESD protection diodes in DA1, DA2 with the DS-DESD protection scheme sustains the even higher ESD level of more than 8 kV in HBM and 575 V in MM. With larger ESD protection diodes, contributing larger parasitic capacitances, the ESD robustness of the DA with ESD protection is better and the DS-DESD protection scheme exhibits higher ESD robustness than the ES-DESD one.

Table IV summarizes the performances of the published CMOS DAs compared with the DA without ESD protection, DA1, and DA2 in this work. DA1 and DA2 exhibit satisfactory

TABLE III
HBM AND MM ESD TEST RESULTS

Mode	HBM (kV)		MM (V)	
	Negative-to-VDD stress	Positive-to-VSS stress	Negative-to-VDD stress	Positive-to-VSS stress
DA without ESD protection	0.2	0.25	≈20	≈20
DA1 (ES-DESD, 300fF)	7.5	5.5	400	325
DA2 (DS-DESD, 300fF)	>8	>8	650	575
DA3 (ES-DESD, 600fF)	>8	>8	675	575
DA4 (DS-DESD, 600fF)	>8	>8	850	750
DA5 (ES-DESD, 900fF)	>8	>8	1000	800

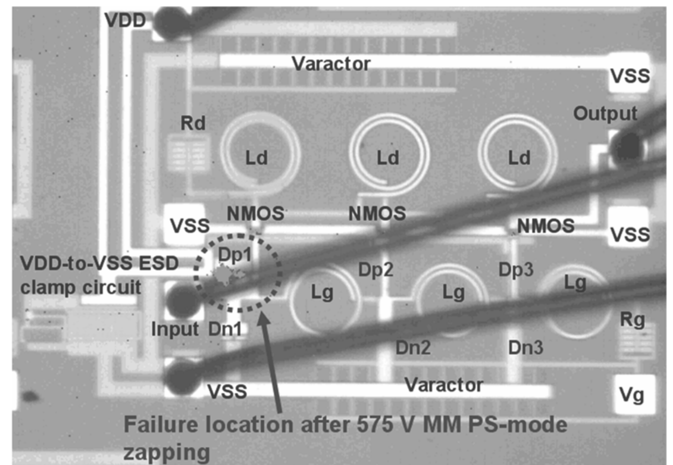
TABLE IV
COMPARISONS AMONG THE PUBLISHED CMOS DAs

	Band-Width (GHz)	Gain (dB)	NF (dB)	S11 (dB)	S22 (dB)	ESD level	Ref.
0.8 μm CMOS	0.3 - 3.0	5.0 ± 1.2	5.1 - 7.0	< -6.0	< -9.0	NA	[7]
0.6 μm CMOS	0.5 - 4.0	6.5 ± 1.2	5.3 - 8.0	< -7.0	< -10.0	NA	[8]
0.6 μm CMOS	0.5 - 7.5	5.5 ± 1.5	8.7 - 13.0	< -6.0	< -9.5	NA	[9]
0.18 μm CMOS	-	5.0	-	< -14.0	-	NA	[10]
0.18 μm CMOS	1.0 - 10.0	8.0 ± 1.0	-	-	-	NA	[11]
0.18 μm CMOS	0.6 - 22.0	7.3 ± 0.8	4.3 - 6.1	< -8.0	< -9.0	NA	[12]
0.18 μm CMOS	0.5 - 14.0	10.6 ± 0.9	3.4 - 5.4	< -11.0	< -12.0	NA	[13]
0.25-μm CMOS DA0 (without ESD protection)	1.0 - 11.4	5.0 ± 1.0	4.4 - 5.6	< -10.0	< -15.0	NA	This work
0.25-μm CMOS DA1 (ES-DESD, 300fF)	1.0 - 10.0	4.7 ± 1.0	4.9 - 5.7	< -9.0	< -18.0	HBM 5.5 kV, MM 325 V	This work
0.25-μm CMOS DA2 (DS-DESD, 300fF)	1.0 - 9.2	4.9 ± 1.1	5.0 - 5.6	< -8.5	< -19.5	HBM 8.0 kV, MM 575 V	This work

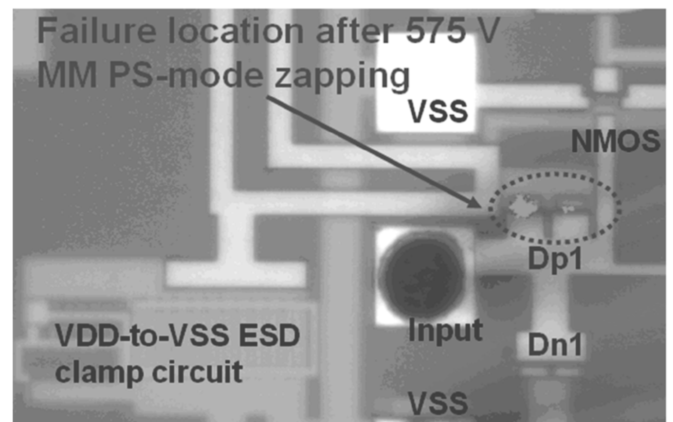
broad-band performances and succeed in providing excellent ESD protection.

C. Failure Analysis

The EMMI (photon emission microscope) pictures in Fig. 26 have confirmed that the ESD damage, indicated by the arrow, is located on the junction of the first p-diode with a large shining area after the positive-to-VSS (PS-mode) MM ESD stress. In PS-mode, the input pad is zapped by a positive ESD stress and the VSS pad is grounded. From the resistive ladder model in Fig. 15, during the ESD event, most ESD current is surely discharged through the shortest path, namely the first section of ESD protection circuit. This evidence has confirmed that the DS-DESD scheme can indeed achieve better ESD performance than the ES-DESD scheme in DA application.



(a)



(b)

Fig. 26. EMMI photographs to show the location of ESD damage in DA2 with DS-DESD protection after positive-to-VSS (PS-mode) MM ESD stress. (a) Whole view of DA2 with DS-DESD protection. (b) Zoomed-in view of the damaged location on the p-diode (Dp1) at the first section of ESD protection.

V. CONCLUSION

Two new types of broad-band ESD protection schemes used to protect the DA have been proposed and successfully investigated in a standard 0.25-μm CMOS process. From the experimental results, the DA, employing the ES-DESD protection scheme with the total parasitic capacitance of 300 fF contributed by the ESD protection diodes in the input port, has high ESD robustness (the HBM ESD level of 5.5 kV and the MM ESD level of 325 V) with only a little degradation on the broad-band RF performance. The decreasing-sized distributed ESD (DS-DESD) protection scheme, applied to the DA with the total parasitic capacitance of 300 fF contributed by the ESD diodes in the input port, has enhanced the ESD robustness to a higher level (the HBM ESD level of more than 8 kV and the MM ESD level of 575 V) and has not deteriorated the broad-band RF performance much. Hence, the proposed two ESD protection schemes are useful and feasible to codesign the RF performance and ESD robustness of DA in broad-band applications.

REFERENCES

[1] T. Wong, *Fundamentals of Distributed Amplification*. Norwood, MA: Artech House, 1993.

[2] E. W. Strid and K. R. Gleason, "A DC-12 GHz monolithic GaAsFET distributed amplifier," *IEEE Trans. Microw. Theory Tech.*, vol. MTT–30, no. 7, pp. 969–975, Jul. 1982.

[3] Y. Ayasli, R. L. Mozzi, J. L. Vorhaus, L. D. Reynolds, and R. A. Pucel, "A monolithic GaAs 1–13-GHz traveling-wave amplifier," *IEEE Trans. Microw. Theory Tech.*, vol. MTT-30, no. 7, pp. 976–981, Jul. 1982.

[4] K. B. Niclas, W. T. Wilser, T. R. Kritzer, and R. R. Pereira, "On theory and performance of solid-state microwave distributed amplifiers," *IEEE Trans. Microw. Theory Tech.*, vol. MTT-31, no. 6, pp. 447–456, Jun. 1983.

[5] K. B. Niclas, R. D. Remba, R. R. Pereira, and B. D. Cantos, "The declining drain line lengths circuit—A computer derived design concept applied to a 2–26.5-GHz distributed amplifier," *IEEE Trans. Microw. Theory Tech.*, vol. MTT-34, no. 4, pp. 427–434, Apr. 1986.
[6] S. N. Prasad, J. B. Beyer, and I.-S. Chang, "Power-bandwidth considerations in the design of MESFET distributed amplifiers," *IEEE Trans. Microw. Theory Tech.*, vol. 36, no. 7, pp. 1117–1123, Jul. 1988.
[7] P. J. Sullivan, B. A. Xavier, and W. H. Ku, "An integrated CMOS distributed amplifier utilizing packaging inductance," *IEEE Trans. Microw. Theory Tech.*, vol. 45, no. 10, pp. 1969–1975, Oct. 1997.
[8] B. M. Ballweber, R. Gupta, and D. J. Allstot, "A fully integrated 0.5–5.5-GHz CMOS distributed amplifier," *IEEE J. Solid-State Circuits*, vol. 35, no. 2, pp. 231–239, Feb. 2000.
[9] H.-T. Ahn and D. J. Allstot, "A 0.5–8.5-GHz fully differential CMOS distributed amplifier," *IEEE J. Solid-State Circuits*, vol. 37, no. 8, pp. 985–993, Aug. 2002.
[10] B. Kleveland, C. H. Diaz, D. Vook, L. Madden, T. H. Lee, and S. S. Wong, "Monolithic CMOS distributed amplifier and oscillator," in *Proc. IEEE Int. Solid-State Circuits Conf. Dig. Tech. Papers*, 1999, pp. 70–71.
[11] B. M. Frank, A. P. Freundorfer, and Y. M. M. Antar, "Performance of 1–10-GHz traveling wave amplifiers in 0.18-μm CMOS," *IEEE Microw. Wireless Compon. Lett.*, vol. 12, no. 9, pp. 327–329, Sep. 2002.
[12] R.-C. Liu, K.-L. Deng, and H. Wang, "A 0.6–22-GHz broad-band CMOS distributed amplifier," in *Proc. IEEE Radio Freq. Integrated Circuit Symp.*, 2003, pp. 103–106.
[13] R.-C. Liu, C.-S. Lin, K.-L. Deng, and H. Wang, "A 0.5–14-GHz 10.6-dB CMOS cascode distributed amplifier," in *Proc. IEEE VLSI Circuits Symp. Dig. Tech. Papers*, 2003, pp. 139–140.
[14] B. Kleveland, T. J. Maloney, I. Morgan, L. Madden, T. H. Lee, and S. S. Wong, "Distributed ESD protection for high-speed integrated circuits," *IEEE Electron Device Lett.*, vol. 21, no. 8, pp. 390–392, Aug. 2000.
[15] C. Ito, K. Banerjee, and R. W. Dutton, "Analysis and design of distributed ESD protection circuits for high-speed mixed-signal and RF ICs," *IEEE Trans. Electron Devices*, vol. 49, no. 8, pp. 1444–1454, Aug. 2002.
[16] S. Galal and B. Razavi, "Broad-band ESD protection circuits in CMOS technology," *IEEE J. Solid-State Circuits*, vol. 38, no. 12, pp. 2334–2340, Dec. 2003.
[17] M.-D. Ker, B.-J. Kuo, and Y.-W. Hsiao, "Co-design on broadband CMOS RF distributed amplifier with on-chip ESD protection circuit," in *Proc. 16th Asia Pacific Microwave Conf.*, 2004, p. 7.
[18] D. G. Sarma, "On distributed amplification," *Proc. Inst. Elect. Eng.*, pp. 689–697, 1954.
[19] D. M. Pozar, *Microwave Engineering*. Reading, MA: Addison-Wesley, 1990.
[20] J. R. Long and M. A. Copeland, "The modeling, characterization, and design of monolithic inductors for silicon RF ICs," *IEEE J. Solid-State Circuits*, vol. 32, no. 3, pp. 357–369, Mar. 1997.
[21] S. S. Mohan, M. M. Hershenson, S. P. Boyd, and T. H. Lee, "Simple accurate expressions for planar spiral inductances," *IEEE J. Solid-State Circuits*, vol. 34, no. 10, pp. 1419–1424, Oct. 1999.
[22] R. M. D. A. Velghe, P. W. H. de Vreede, and P. H. Woerlee, "Diode network used as ESD protection in RF applications," in *Proc. EOS/ESD Symp.*, 2001, pp. 337–345.
[23] M.-D. Ker, "Whole-chip ESD protection design with efficient VDD-to-VSS ESD clamp circuits for submicron CMOS VLSI," *IEEE Trans. Electron Devices*, vol. 46, no. 1, pp. 173–183, Jan. 1999.
[24] M.-D. Ker, W.-Y. Lo, C.-M. Lee, C.-P. Chen, and H.-S. Kao, "ESD protection design for 900-MHz RF receiver with 8-kV HBM ESD robustness," in *Proc. IEEE Radio Frequency Integrated Circuit Symp.*, 2002, pp. 427–430.
[25] *Electrostatic Discharge (ESD) Sensitivity Testing Human Body Model (HBM)*, 1997. EIA/JEDEC Standard EIA/JESD22-A114-A.
[26] *Electrostatic Discharge (ESD) Sensitivity Testing Machine Model (MM)*, 1997. EIA/JEDEC Standard EIA/JESD22-A115-A.

Ming-Dou Ker (S'92–M'94–SM'97) received the B.S. degree in electronics engineering and the M.S. and Ph.D. degrees from National Chiao-Tung University, Hsinchu, Taiwan, R.O.C., in 1986, 1988, and 1993, respectively.

In 1994, he joined the Very Large Scale Integration (VLSI) Design Department, Computer and Communication Research Laboratories (CCL), Industrial Technology Research Institute (ITRI), Taiwan, R.O.C., as a Circuit Design Engineer. In 1998, he became a Department Manager with the VLSI Design Division, CCL/ITRI. In 2000, he became an Associate Professor with the Department of Electronics Engineering, National Chiao-Tung University, where he is now a Full Professor. He has been invited to teach or help ESD protection design and latchup prevention by hundreds of design houses and semiconductor companies in Taiwan, R.O.C., Silicon Valley, San Jose, CA, Singapore, and Mainland China. His research interests include reliability and quality design for nanoelectronics and gigascale systems, high-speed or mixed-voltage I/O interface circuits, special sensor circuits, and thin-film transistor (TFT) circuits. In the field of reliability and quality design for CMOS ICs, he has authored or coauthored over 200 technical papers in international journals and conferences. He holds over 180 patents on reliability and quality design for ICs, which including 95 U.S. patents. His inventions on ESD protection design and latchup prevention method have been widely used in modern IC products.

Dr. Ker has serviced as member of the Technical Program Committee and Session Chair of numerous international conferences. He is currently serving as Associate Editor for the IEEE TRANSACTIONS ON VERY LARGE SCALE INTEGRATION (VLSI) SYSTEMS. He was elected as the first President of the Taiwan ESD Association in 2001. He has also been the recipient of numerous research awards presented by ITRI, the National Science Council, National Chiao-Tung University, and the Dragon Thesis Award presented by the Acer Foundation. In 2003, he was selected as one of the Ten Outstanding Young Persons in Taiwan, R.O.C., by the Junior Chamber International (JCI).

Yuan-Wen Hsiao (S'03) was born in Taiwan, R.O.C., in 1982. He received the B.S. degree from the Department of Electronics Engineering, National Chiao-Tung University (NCTU), Hsinchu, Taiwan, R.O.C., in 2004. He is currently working toward the Ph.D. degree in the Institute of Electronics, NCTU.

His current research interests include high-speed I/O circuits and ESD protection design for mixed-signal and RF ICs.

Bing-Jye Kuo was born in Taiwan, R.O.C., in 1978. He received the B.S. degree from the Department of Electronics Engineering and the M.S. degree from the Institute of Electronics, National Chiao-Tung University (NCTU), Hsinchu, Taiwan, R.O.C., in 2000 and 2004, respectively.

Since 2002, he has been with the Nanoelectronics and Gigascale Systems Laboratory, NCTU. In 2004, he joined MediaTek Incorporation, Hsinchu, as a Design Engineer responsible for the on-chip RF ESD protection circuit design and transmitter circuit design. His current research interests include GSM transmitter circuit design and on-chip RF ESD protection circuit design.