Low-Power Fully Integrated and Tunable CMOS RF Wireless Receiver for ISM Band Consumer Applications

Simon Cimin Li, Hong-Sing Kao, Chia-Pei Chen, and Chung-Chih Su

***Abstract*—A 0.25-μm single-chip CMOS single-conversion tunable low intermediate frequency (IF) receiver operated in the 902–928-MHz industrial, scientific, and medical band is proposed. A new 10.7-MHz IF section that contains a limiting amplifier and a frequency modulated/frequency-shift-key demodulator is designed. The frequency to voltage conversion gain of the demodulator is 15 mV/kHz and the dynamic range of the limiting amplifier is around 80 dB. The sensitivity of the IF section including the demodulator and limiting amplifier is -72 dBm. With on-chip tunable components in the low-power low-noise amplifier (LNA) and *LC*-tank voltage-controlled oscillator circuit, the receiver measures an RF gain of 15 dB at 915 MHz, a sensitivity of -80 dBm at 0.1% bit-error rate, an input referred third-order intercept point of -9 dBm, and a noise figure of 5 dB with a current consumption of 33 mA and a 2450 μm $\times$ 2450 μm chip area.**

***Index Terms*—Demodulator, frequency synthesizer, low intermediate frequency (IF) receiver, low-noise amplifier (LNA), low-power receiver, mixer, RF CMOS, single-conversion receiver.**

I. Introduction

THE DEMAND for low-cost wireless systems has soared in the recent past. There is a rapidly growing market for low-power short-range wireless systems for alarm systems, sensors, and controls. Because of their limited range and low data rates, these short-range systems often operate in the industrial, scientific, and medical (ISM) bands. There is a tradeoff among the antenna size, power consumption, and design feasibility that depends on the operation frequency. The ISM band of 915 MHz was selected for this paper as a compromise among these parameters.

The unrivaled growth of the wireless telecommunication systems has led to persistent demand for small, low-cost, low-power RF terminals. RF front-end design is pushed toward an ultimate goal of full integration in economical CMOS technology, rendering significant space, cost, and power reductions.

Manuscript received January 16, 2004; revised May 29, 2004, August 20, 2004, and January 8, 2005. This work was supported in part by the National Science Council, Republic of China, under Contract NSC-86-88-2221-E-224-018. This paper was recommended by Associate Editor T. B. Tarim.

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Digital Object Identifier 10.1109/TCSI.2005.852926

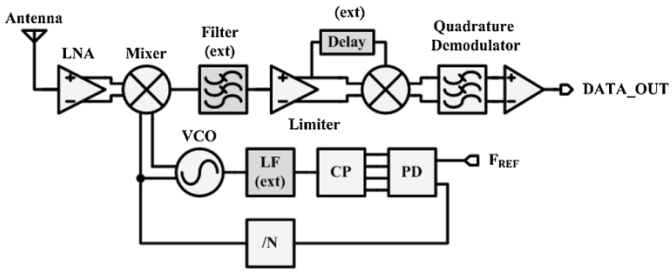

Fig. 1. Proposed low-power low-IF 915 MHz ISM receiver.

To meet such demand, much work has been focused on realizing fully integrated single-chip receiver (Rx) within CMOS technologies [1]–[6].

In this paper, a fully integrated single-chip wireless receiver integrated circuit (IC) is intended for use in the unlicensed 902–928 MHz ISM band as part of a system that communicates at rates between 2 and 390 kbps. The single-chip receiver IC contains a low-noise amplifier (LNA), a mixer, a frequency synthesizer, and a quadrature demodulator. It also features the capability of on-chip tuning in the analog front-end design. The architecture of the fully integrated and tunable CMOS heterodyne receiver is shown in Fig. 1.

The IC is housed in a 32-lead low-profile quad flat pack (LQFP) plastic package, and provides all the functions necessary to implement a binary frequency-shift key (BFSK) demodulation receiver system for many applications in the field of wireless communication. Based on the low-IF single conversion architecture, the receiver is implemented in the 0.25-μm CMOS SP5M technology. Section II reviews receiver architectures including heterodyne and homodyne techniques, and it focuses on the proposed low-power low-IF single conversion receiver and their tradeoffs. The design of building blocks with on-chip tuning facility such as the low-noise amplifier (LNA), mixer, frequency synthesizer, voltage-controlled oscillator, and quadrature demodulator is presented in Section III, respectively. The experimental results of the single-chip receiver are summarized in Section IV, and a conclusion is provided.

II. Low-Power Low-IF Single Conversion Rx

As IC technologies evolve, complexity, cost, power consumption, and the amount of components have been the primary criteria in receiver architectures design, so the relative importance of each of these criteria changes, allowing approaches that once seemed impractical to return as plausible solutions. There are

two main types of receivers used in wireless telecommunication systems based on phase or frequency modulation: the heterodyne and homodyne receiver. The difference between them is in whether intermediate frequency (IF) is used or not. Heterodyne and homodyne receivers are often called IF and zero-IF receivers, respectively. The low-power Rx architectures with a higher integrability such as zero-IF and low-IF Rxs are preferred topologies, while as CMOS fabrication technology can provide an economical solution over its bipolar counterpart. There are many unanswered questions in implementing the whole receiver in CMOS devices instead of bipolar junction transistors, which has hitherto been the usual way to implement low-power wireless receivers.

A typical zero-IF Rx, direct conversion architecture, widely used in paging receivers is attractive when very low-power consumption is at premium [7]. If the IF is not at dc, an image reject filter or another arrangement may be needed to suppress the image channel [8], and inevitably this consumes substantial power. An active low-pass channel-select filter at zero IF always obtains a given dynamic range with lower power than a bandpass filter with the same passband centered at some nonzero IF [9]. The impasse of zero-IF Rxs is $1/f$ noise and mismatch or self-mixing related offsets that corrupt the required signal at low frequencies. The low-IF ($<$ 11 MHz) ISM Rx alleviates this problem by setting the IF frequency to typically one-half the channel bandwidth [1]. Fig. 1 shows the proposed low-power low-IF 915 MHz ISM heterodyne Rx. While selecting a 30-kHz channel at a center frequency of 900 MHz, that prohibitively needs large Q's in bandpass, filtering is performed at progressively lower center frequencies. Channel-selection filtering is performed at low IF, which relaxes the requirements for the channel-selected filter. The tradeoff between image rejection and channel selection typically requires a relatively high IF, making it difficult to integrate the IF filter monolithically. For full integration of high-end RF systems, the low-IF Rx seems the best solution. Recent researches have demonstrated in several reported RF CMOS circuits in the global positioning systems (GPS) [10] or Bluetooth [11]–[13]. Therefore, for intended use in the unlicensed 902–928 MHz ISM band, low-IF heterodyne Rx is the best choice for a conventional RF system product design.

III. Building Blocks of Low-IF ISM Receiver

A. Low-Power Tunable LNA

The design of LNA associates in a single transistor the foremost front-end design tradeoffs: impedance matching, power consumption, signal linearity, noise figure, and RF bandwidth. LNAs with a common-gate input, though convenient for providing a good 50-Ω matching, provide an inherently higher noise figure. The noise, input matching, and stability requirements limit the acceptable LNA topologies to only a few. Widely used examples are inductively degenerated cascode topologies as they provide both a high reverse isolation (thus ensuring stability) and an input resistance that can be set to 50 Ω by design. To achieve a relatively low noise figure and a reasonable input match, an input-matched cascode LNA

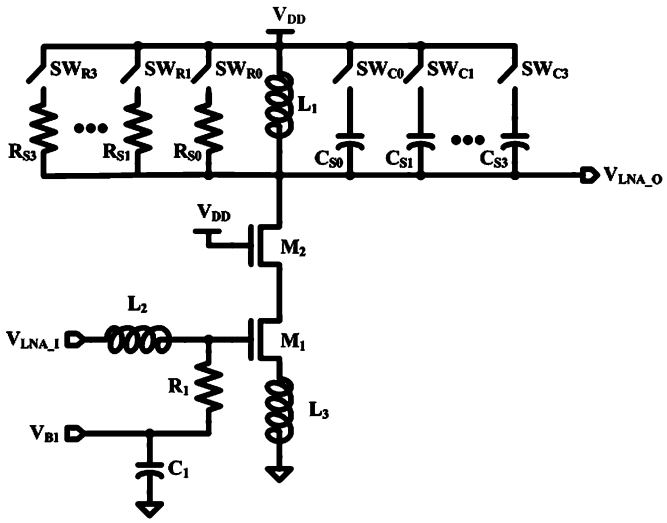

Fig. 2. Tunable LNA circuit diagram.

topology with the inductive source degeneration (Fig. 2) is employed in the front-end design. To avoid uncertainties due to bond-wire inductance, both inductors connected with source (L_3) and drain (L_1) are integrated on the chip. Single-stage cascode LNAs have higher input referred third-order intercept point (IIP3) in comparison to multistage LNAs [14]. However, they tend to have a slightly lower power gain and reverse isolation S_{12}. A low S_{12} complicates simultaneous input and output matching of the LNA and its optimization. The cascode transistor as shown in Fig. 2 provides improved reverse isolation without adding excessive noise in the circuit. This can also reduce the Miller effect capacitance at the input. There is an on-chip impedance matching network at the output, which can match the output impedance to the external load of 50 Ω, it corresponding to the input of the IR filter. Since the required S_{11} is typically only -10 dB, an extra degree of freedom can be introduced by realizing a nonperfect input match. The input power of the RF source is defined by

$$P_{\text{in}} = \frac{V_{\text{LNA\_}I}^2}{4R_s} \tag{1}$$

where R_s is the 50 Ω impedance matched between the source and L_2. The output power of the LNA is determined by the equivalent resistance of tunable resistive load $(R_{Si}, i = 0, 1\text{–}3)$ as indicated in Fig. 2 and by the current injected into the tuned load and one of the resistors after L_1

$$P_{\text{out}} = i_{\text{out}}^2 R_{\text{TL}}. \tag{2}$$

R_{TL} represents a combination of equivalent parallel resistance of the load inductor L_1. The self-inductance is tuned out by the excess capacitance at that node. The output current is given by [15], [16]

$$i_{\text{out}}^2 = i_{\text{in}}^2 \left(\frac{\omega_{HP}}{\omega_O}\right)^2 = \frac{4P_{\text{in}}R_s}{(R_s + R_{\text{in}})^2}\left(\frac{\omega_{HP}}{\omega_O}\right)^2. \tag{3}$$

For a given frequency (ω_{HP}) the highest level of power gain is obtained by making the input impedance R_{in} (seen into the gate of M_1) as low as possible. This means that even though less

power is engaged at the LNA input, the power is exploited more efficiently to generate output current and, hence, output power. It is further seen [15] that the power gain of the LNA increases with increasing ω_{HP}, i.e., with decreasing threshold voltage headroom [16] with deeper submicron CMOS technology.

The cascode circuit of Fig. 2 incorporates inductive degeneration to create a real part in the input impedance. Neglecting the gate–drain and source–bulk capacitance, we can write

$$Z_{\text{in}} \approx \left(\frac{g_{m1}}{C_{GS1}} + s\right) L_3 + \frac{1}{sC_{GS1}}. \tag{4}$$

Thus, a proper choice of g_{m1}, L_3, and C_{GS1} yields a real part of 50 Ω. In practice, the last two terms may not resonate at the frequency of interest, necessitating the use of off-chip components at the input. At high frequencies, the required value of L_3 becomes comparable with the inductance of the ground bond wire, requiring multiple bonds or accurate modeling of the wire inductance. Also, the reduction of the equivalent transconductance as a result of degeneration may magnify the noise contributed by M_2. This is because the parasitic capacitance at the drain of M_1 provides some gain from the gate of M_2 to the output. Cascode LNAs have also been implemented in differential form [2], [17]. While differential operation lowers the sensitivity to common-mode disturbance, it requires higher power dissipation to achieve the same noise figure as a single-ended counterpart. A single-ended LNA, in comparison with a differential LNA, dissipates approximately $1/4$ of the power [18] for the same noise and linearity of referred input. However, a single-ended LNA is more susceptible to pick up the substrate noise. Besides, the antenna signal is commonly single-ended; a means of conversion to differential form, e.g., a transformer is inevitable. A transformer either on-chip or off-chip, however, represents a bulky device.

The LNA should provide adequate gain and linearity in the RF input band of 902–928 MHz. As g_m is small at low bias current, a large gain can only be achieved with high load impedance. In order to achieve the minimum external components for low cost and highly integrated consideration, the input of the LNA is single-ended input without external baluns. As we optimize the production yield against process variation as is concerned, the center frequency and gain of the LNA are tunable via selective switches (SW_{Ri} and SW_{Ci}) for combination the resistive $(R_{Si}, i = 0, 1\text{–}3)$ and/or capacitive $(C_{Si}, i = 0, 1\text{–}3)$ load. The proposed tunable LNA, operating at ISM band, draws 4.5 mA from a 3.3-V supply, yielding a total power consumption of merely 14.85 mW. The input reflection coefficient is -13 dB. The power gain of the LNA is 12 dB, while the reverse isolation is more than 23 dB. The IIP3 of the LNA is -11 dBm, which is more than sufficient for the ISM application.

B. Low-Power Downconversion Mixer

Downconversion mixers in the received path perform frequency translation by multiplying the signals at two distinct differential inputs, called the RF port and the local oscillator (LO) port. The incoming RF signal amplified by the LNA is usually single-ended and translated by the mixer to a lower IF. Since

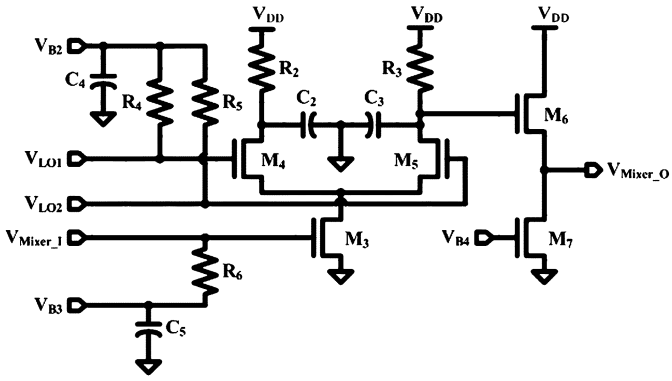

Fig. 3. Downconversion mixer circuit diagram.

MOS transistors have a much higher IIP3 than bipolar transistors, the required linearization and LO drive in CMOS active mixers distinguish their design from their bipolar counterparts. Fig. 3 shows a single-balanced low-power downconversion CMOS mixer topology. The single-balanced configuration exhibits less input-referred noise than the double-balanced topology for a given power dissipation. A likely drawback of the single-balanced mixer is the LO-IF feedthrough. Note that M_4 and M_5 operate as a differential pair, and thus amplify the LO signal. If the IF is not much lower than the LO frequency then a first-order low-pass filter following the mixer may not adequately suppress the LO feedthrough without attenuating the IF signal. An IF bandpass filter (10.7 MHz with a bandwidth of 200 kHz) in this receiver architecture for a downmixing radio signal of 915 MHz is chosen for diminishing the effects of LO feedthrough. In Fig. 3, M_3 can be linearized with no need for explicit degeneration by simply increasing the gate-source overdrive voltage $(V_{GS} - V_{TH})$. This of course trades with the bias current or with the transistor aspect ratio, raising the power consumption or lowering the device transconductance. CMOS mixers typically demand large LO swings so that the switching pairs [e.g., M_4 and M_5 in Fig. 3] do not remain on simultaneously for a considerable period of time. Increasing the switching devices width can lower the required swing, but at the cost of increasing their noise contribution and higher capacitance in the RF signal path. Thus, the choice of device dimensions and bias currents play a critical role in performance. In particular, the downconversion mixer(s) must achieve high linearity and a reasonable noise figure under the constraint of required low-power consumption. The interface between the LNA and the mixer are capacitively coupled with a linearized transconductance. The value of V_{B3} establishes the mixer bias current, while R_6 is chosen large enough not to load down the gate circuit (and to also reduce its noise contribution). In practice, an IF bandpass filter acting as a channel-select filter (with bandwidth 200 kHz) would be used to remove the LO and other undesired spectral components from the output.

With a noise figure of 6 dB and an IIP3 of -4.9 dBm, a single-balanced mixer has a conversion gain of 3 dB with acceptable degradation in the overall noise and nonlinearity. It requires a low bias current of 0.5 mA to achieve downconversion in the receiver.

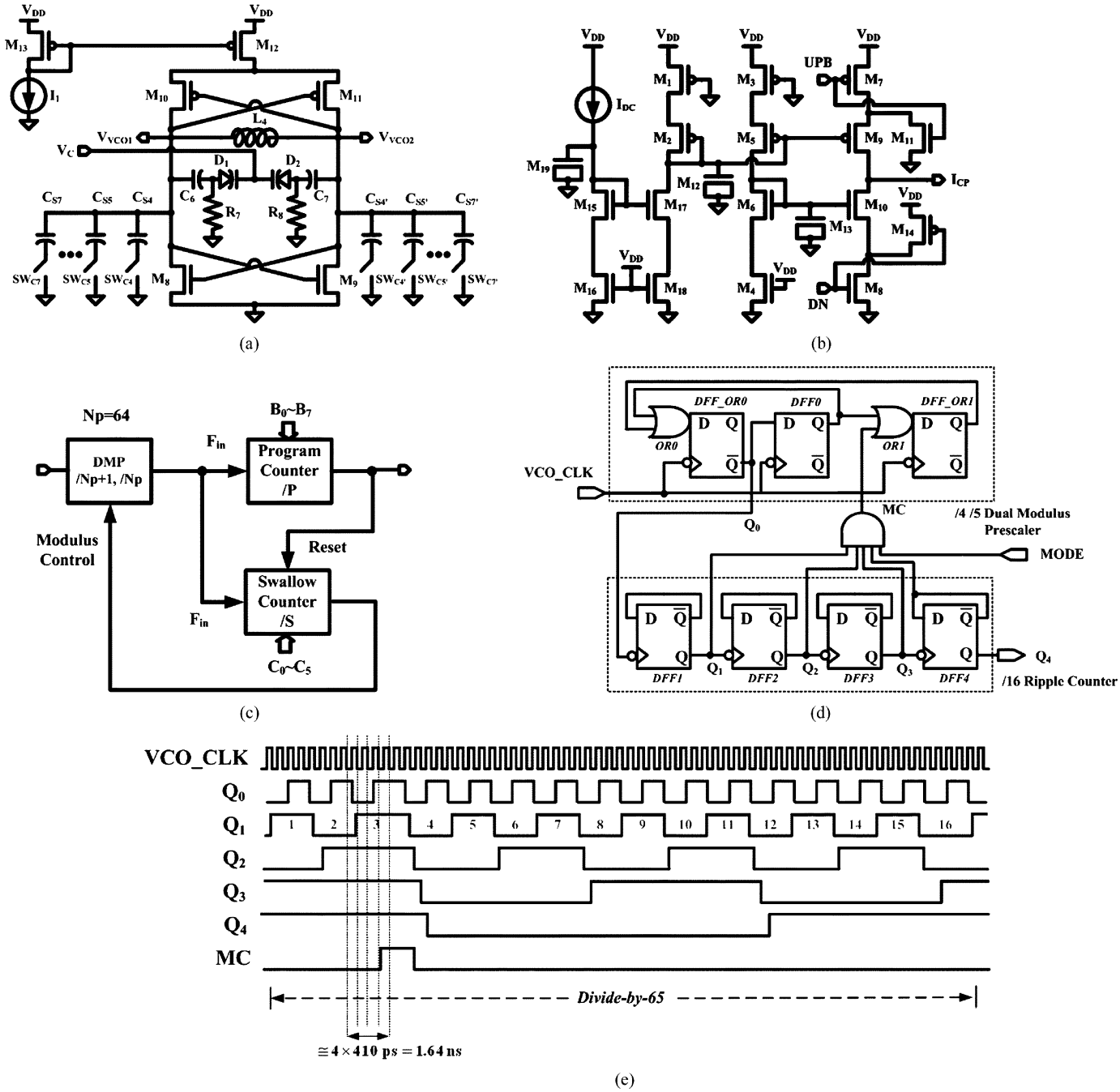

Fig. 4. (a) Tunable *LC*-tank VCO circuit diagram. (b) Charge pump schematic. (c) Architecture of frequency divider. (d) Logic block diagram of the prescaler. (e) Timing diagram of the prescaler.

C. Baseband Interface

After the RF signal is downconverted to the baseband, it must be channel-select filtered, IF amplified, demodulated, and data sliced. The channel-select filter is a low-cost discrete ceramic bandpass filter with a center frequency of 10.7 MHz and a bandwidth of 200 kHz. As the RF and IF sections of receivers incorporate external components and hence perform a lesser portion of the signal processing stage task, the design of baseband interface between the downconversion mixer and the following stage becomes progressively more challenging. Moreover, noise-linearity-power tradeoffs limit the amount of gain provided by the RF and IF circuits. Since the signal at the mixer output is in the range of tens of microvolts and the interferers are quite large (e.g., 60 dB above the signal level), both the noise and the nonlinearity of the IF amplifier are critical. Consequently, the baseband interface must process small signals in the presence of large interferers. To avoid the reduction in the mixer voltage gain, the IF amplifier must exhibit a relatively high input impedance. Considering the interface between the mixer and the baseband section as shown in Fig. 1, the channel-select filter suppresses out the channel interferers, allowing the IF amplifier to be a nonlinear, high-gain amplifier.

D. Frequency Synthesizer With Tunable Voltage-Controlled Oscillator

The frequency synthesizer, as shown in Fig. 1, consists of an *LC*-tank voltage-controlled osicillator (VCO), a crystal os-

cillator, a programmable frequency divider, a phase-frequency detector (PFD), a charge pump (CP), and a loop filter. To fully integrate the phase-locked loop (PLL) frequency synthesizer, phase noise and spurious suppression must be traded off against integrated capacitance and settling time. Again, there is no substitute for cubic inches since large external capacitors can implement the large time constant of the loop filter without large resistors (i.e., noise). The *LC*-tank VCO is the most key component in the frequency synthesizer. Fig. 4(a) shows the circuit diagram of a tunable *LC*-tank VCO. The architecture of VCO in this design is a complementary *LC* oscillator. nMOS and pMOS are connected as cross coupled to generate negative resistance. If this negative resistance could compensate for the loss of *LC* tank, the circuit will start oscillation. L_4 is the on-chip spiral inductor with a 3.7-nH inductance. The series resistance of the spiral inductor is around 4.6 Ω, and its quality factor is 4.2 at 1 GHz. The varactor is implemented by a P+/N-well junction capacitor. The capacitance of the varactor is controlled by reversed bias of the P+/N-well junction. To reduce sensitivity to power supply, the dc blocking capacitors are connected in series to the varactor with a grounded resistor. The other advantage of this topology is that the controlled voltage can be a full swing between supply voltage and the ground. M_8 and M_9 (M_{10} and M_{11}) are cross connected for the positive feedback to form the negative resistor. M_{11} acts like a tunable current source to control the output swing of the VCO. By means of selective switches (SW_{Ci}), linear capacitors ($C_{Si}, i = 4, 5\text{–}7$) are utilized to universal tune the VCO frequency band to improve the yield rate in mass production. An autotuning mechanism will be implemented in the future to reduce test costs.

Fig. 4(b) shows the schematic of the CP circuit. The sinking or/and sourcing current depends on the command of UPB to M_7 and the command of DN to M_8, therefore M_7 and M_8 are switches. M_{11} will discharge the parasitic capacitance on the drain of M_7 while M_7 is off. Otherwise, the charge will leak to the loop filter. Also, M_{14} will discharge the parasitic capacitance on the drain of M_8 while M_8 is off. It can be observed that the sinking/sourcing current tends to zero when PLL is locked near the edge of the up/down command.

In a typical PLL type frequency synthesizer, a frequency divider is usually used to select the desired lock frequency. The architecture of the frequency divider incorporates a high speed dual-modulus prescaler (DMP), a low-speed programmable counter, and a low-speed swallow counter, as depicted in Fig. 4(c). Initially, DMP divides the input frequency by $\mathrm{Np}+1$. The swallow counter counts the DMP output pulses until S pulses are reached. Then the DMP modulus control is changed, which forces the divide ratio of DMP to be changed to Np. The DMP output pulses are also counted in the program counter. Fig. 4(d) and (e) show a logic block and associated timing diagram of the prescaler. If the program counter has counted P pulses, it will reset itself and the swallow counter. The total divide ratio of the frequency divider can be represented as

$$N = (Np+1)\cdot S + Np\cdot(P-S) = Np\cdot P + S. \qquad (5)$$

The use of a variable modulus prescaler at high frequency instead of using a fixed frequency prescaler has the advantage that only the prescaler works at high frequency while the remaining divider circuitry works at much lower frequencies. This saves power, reduces the cost, and makes the layout of the divider relatively noncritical. The main contributors to the PLL synthesizer power consumption are the VCO (up to 70%, 23 mW) and the frequency divider (up to 30%, 9 mW). The phase noise contribution of the prescaler to the phase of frequency synthesizer is usually negligible. The overall noise from the prescaler is much lower than that of a crystal reference multiplied by the prescaler ratio [19].

The out-of-band phase noise of a PLL synthesizer is mainly determined by the VCO. The in-band phase noise, however, is determined by the remaining loop components and is multiplied by the division factor of the prescaler. In order to achieve a fine frequency resolution, a high division factor is needed, severely deteriorating the in-band noise and, consequently, the root mean-square (rms) phase error $\Delta\Phi_{\mathrm{rms}}$, which may not exceed 2° (i.e., -75 dBc/Hz in a 200-kHz band). In order to increase the flexibility of the frequency synthesizer for settling time, the loop filter is implemented by off-chip discrete components. The crystal oscillator also requires a discrete crystal providing a reference signal with high quality. A CP current of 200 μA is adopted in this design to achieve good stability, good transient behavior, low steady-state phase error, and low-power dissipation. A second-order loop filter is used to achieve loop bandwidth of 200 kHz.

E. IF Section

A low-voltage low-power 10.7-MHz IF section shown in Fig. 5(a) including a limiting amplifier and an frequency modulated (FM) FSK demodulator is proposed. The FSK means that the information in the transmitted data is encoded by using two different frequencies. These two frequencies differ from each other by the selected deviation. In principle the IF signals processing circuit performs limitation of signal magnitude and signal demodulation in FM/FSK. A limiting amplifier in FM/FSK applications is usually employed in the limitation of the signal magnitude [20]. However, it may reduce the sensitivity and therefore degrade the recovered data bit-error rate (BER) due to a large dc offset [21]. Signal demodulation in FM/FSK requires an FM/FSK demodulator with high frequency discrimination as a result of the narrow signal bandwidth of the FSK. In fact, FSK can be regarded as a discrete FM signal whose frequencies are equally spaced and centered at a nominal carrier frequency.

The limiting IF amplifier represents essentially a chain of gain cells, which expand the different magnitudes of input signal into saturation. The limiting amplifier is implemented by a cascade of identical gain cells that come with an auxiliary output driver as shown in Fig. 5(b). The limiting amplifier is designed with a proper dc feedback loop. With the dc feedback loop, the dc offset can be suppressed and will not saturate the following stage. To extract dc offset voltage, a large discrete capacitor is necessary to save chip area. The core of the gain cells, as shown in Fig. 5(b), is a source-coupled differential input pair M_1–M_2 with a diode-load M_3–M_4. M_6, M_7 and M_8 perform as a full-wave rectifier for converting the signal magnitude into

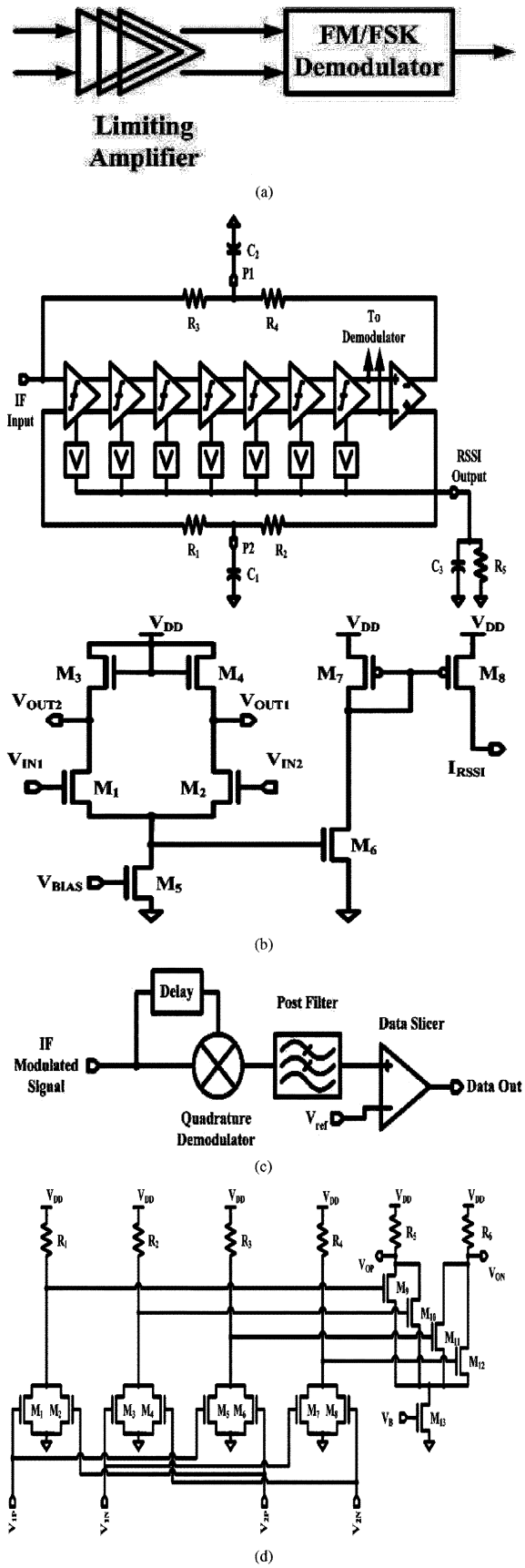

Fig. 5. (a) IF section. (b) Block diagram of the limiting amplifier with gain cell circuit. (c) Block diagram of the FM/FSK demodulator. (d) Proposed quadrature detector: multiplier circuit.

subsequent current. The outputs of each full-wave rectifier are connected in parallel to the external capacitor and resistor as shown in Fig. 5(b). Therefore, the resulting voltage in the external capacitor and resistor will be proportional to IF signal amplitude. At the same time, it must yield a low-pass function to alleviate the dc offset due to mismatch. Fig. 5(c) shows a block diagram of the FM/FSK demodulator. The FM/FSK demodulator employs a quadrature detector that is composed of an on-chip phase detector and an external tank phase shifter to achieve high discrimination function under low-voltage operation. The proposed quadrature detector [22], [23], based on the multiplier output which in turn is proportional to the product of two input variables, for FM/FSK demodulation is shown in Fig. 5(d). In this structure, a phase shifter shifts the phase of the incoming FM signal by an amount that is proportional to its instantaneous frequency. A phase detector (PD) is then used to detect the phase difference between the limiting amplifier output signal and its phase-shifted signal. Finally, a low-pass post filter is used to remove high-frequency noise and extract the demodulated output. This method converts frequency deviation into shift of the phase. Therefore, appropriate value of the phase shift can improve the frequency discrimination in demodulation. The frequency to voltage conversion gain of the demodulator is 15 mV/kHz and the dynamic range of the limiting amplifier is around 80 dB. The sensitivity of the IF section including the demodulator and limiting amplifier achieves -72 dBm. The proposed IF section dissipates a power of 14 mW.

IV. Experimental Results

A single-chip of low-IF 915 MHz receiver of single-conversion was fabricated by using a standard 1P5M CMOS technology of 0.25 μm. The fabricated receiver was measured under a nominal 3.3 V voltage supply, and it remained functional from 2.7 to 3.6 V and above. During measurement, the bare die was housed in a 32-lead LQFP plastic package. The dielectric of the PCB used in this work was standard FR4 with a relative dielectric constant of approximately 4.5 between 2–3 GHz. A socket with high frequency operation was used to contact the ICs instead of solder. Capacitors with different values were used as the bypass capacitors for $V_{\rm CC}$ and $V_{\rm DD}$ to filter out the noise with different frequencies. The self-resonance frequency of these capacitors must be sufficiently high to pass the output signals with small loss.

Due to the input impedance of LNA being designed to around 50 Ω over a large frequency bandwidth; the S_{11} of the receiver input is smaller than -9 dB. Fig. 6 shows S_{11} versus frequency. The minimum value of S_{11} was measured at 1 GHz. So, the receiver can achieve the maximum power transfer from the antenna. In order to obtain the maximum performance, no buffers were used after LNA for measurement.

The conversion gain of the RF front-end including the LNA and mixer is measured with a 10.7-MHz IF frequency. The LO signal is generated by an on-chip frequency synthesizer. The RF signal is fed by a RF signal generator. The frequency response of the RF front-end is shown in Fig. 7. The conversion gain is larger than 11 dB over the ISM band. Fig. 8 shows the noise figure of the RF front-end, which is less than 9 dB. The min-

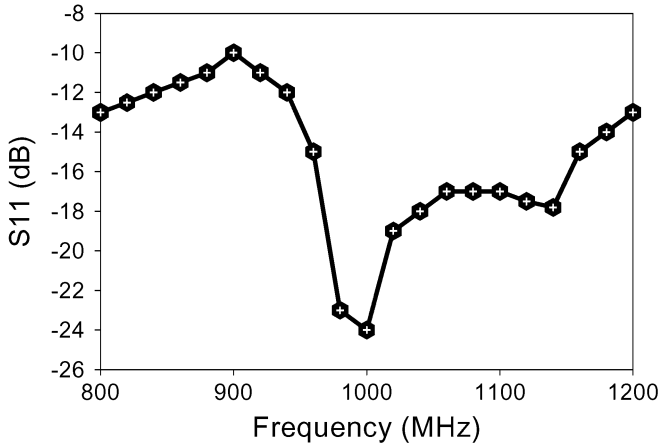

Fig. 6. S_{11} of the LNA.

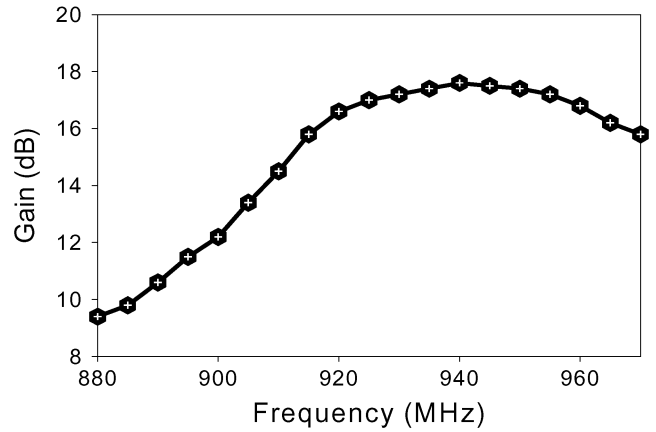

Fig. 7. Conversion gain of the ISM receiver's front-end.

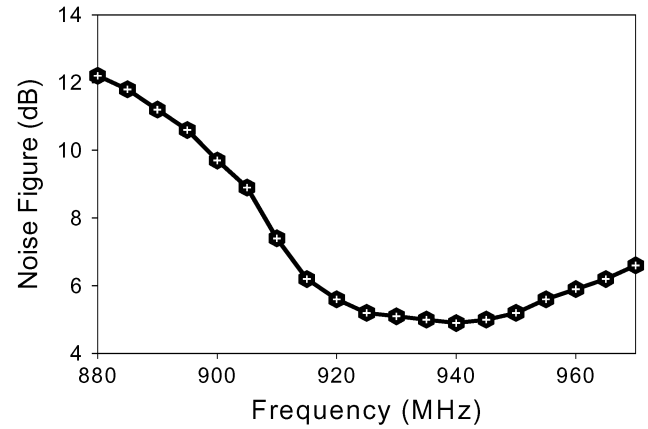

Fig. 8. Noise figure of the ISM receiver's front-end.

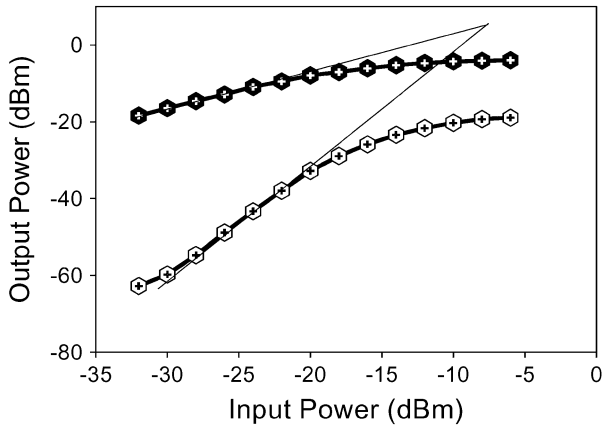

Fig. 9. IIP3 of the ISM receiver's front-end.

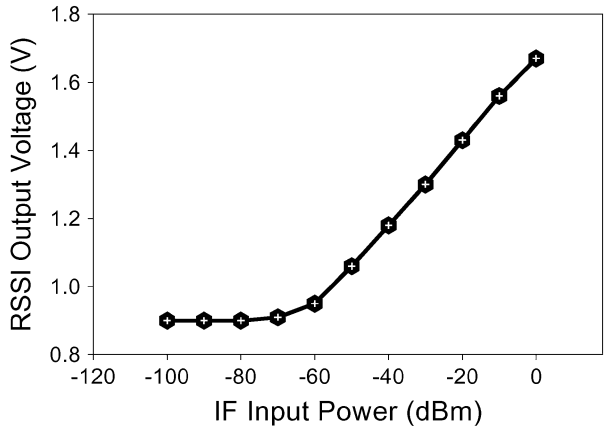

Fig. 10. RSSI output voltage.

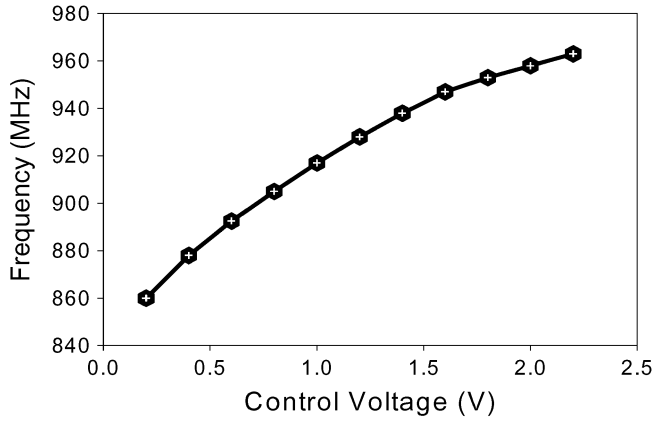

Fig. 11. VCO tuning range.

imum noise figure of 5 dB is obtained at the RF front-end with a maximum conversion gain. The IIP3 of the RF front-end is measured by two applied tones with spacing of 1 MHz. The IIP3 of the RF front-end is -8 dBm as shown in Fig. 9. This specification is appropriate for many applications such as wireless mouse, wireless keyboard, etc.

With 0.1% BER, the sensitivity at IF input of the receiver is -72 dBm. The maximum signal power of the demodulator can demodulate at IF input is 8 dBm. In an IF section, the limiting amplifier has a RSSI function. The RSSI output voltage versus the IF input power is shown in Fig. 10. When the IF input power is larger than -60 dBm, the curve is quite linear as shown in Fig. 10. In the limiter design, the current consumption is only 3 mA. The measured voltage gain is 78 dB over a 12-MHz bandwidth. In the proposed receiver, the quadrature demodulator is used to demodulate the FSK receiver signal. The current consumption is only 1 mA in the demodulator. The receiver data rate with 390 kbps can be achieved and the receiver sensitivity is -80 dBm with 0.1% BER. In Fig. 11, the tuning characteristic measured from the on-chip *LC* VCO shows a tuning frequency range of 110 MHz varying from 860 to 970 MHz as the

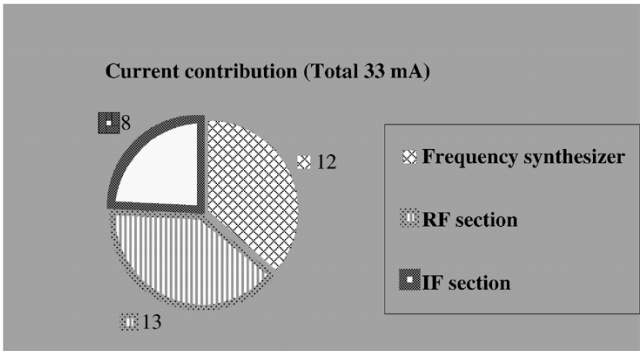

Fig. 12. Current contribution of the ISM receiver.

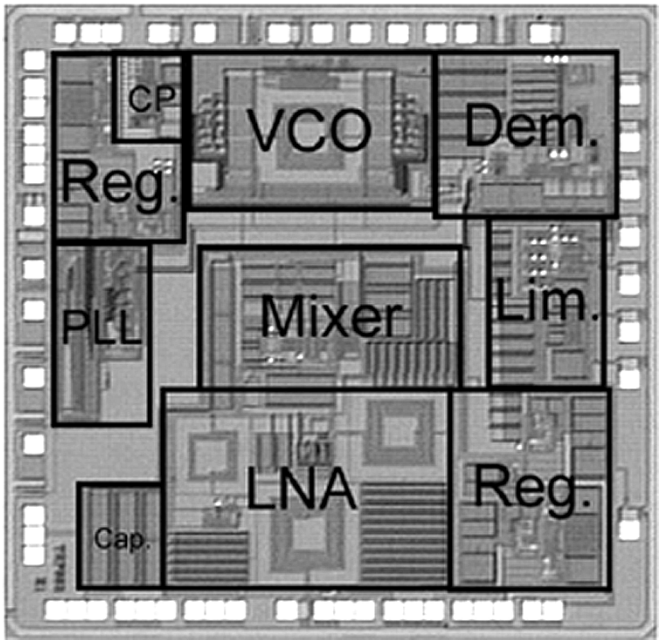

Fig. 13. Chip photograph.

controlled voltage is changed between 0.2 and 2.3 V. As the oscillation frequency of the quadrature VCO varies between minimum and maximum in terms of the tuned range, the simulated peak-to-peak voltage swing of the quadrature VCO is around 1 V_{P-P}. Therefore, the oscillation of the quadrature VCO occurs in the regime of limited current. This large swing signal can make the switching MOS in Gilbert mixer function properly and reduces the noise from the switching MOS.

Fig. 12 shows the current contribution of the receiver chip with a typical power supply voltage of 3.3 V. The current consumption of the RF section including a LNA and a mixer is 12 mA. The IF section consumes 8 mA with the frequency synthesizer dissipates 13 mA. A photomicrograph of the fabricated 915 MHz receiver chip is shown in Fig. 13. The die size is 2450 μm $\times$ 2450 μm. The input pin of the LNA is located in the middle of one side to minimize the length of the bonding wire. Thus, the influence of bonding wire variation can be minimized. Four on-chip spiral inductors are used in this design and they consume a large part of the chip area. Thus, reducing the number of the on-chip spiral inductors is an efficient way to reduce the chip area. The measured performances of the single-chip receiver are summarized in Table I. Table II sums up a comparison with previous works.

TABLE I
PERFORMANCE SUMMARY OF TUNABLE ISM RECEIVER

Power Supply Voltage	**2.7–3.6 V**
Current Consumption	**33 mA**
S_{11}	**–13 dB**
RF Gain	**15 dB**
IIP3	**–8 dBm**
Noise Figure	**5 dB**
Dynamic Range	**80 dB**
VCO Frequency Range	**860–963 MHz**
LO Leakage	**–50 dBm**
Data Rate	**390 kbps**
Sensitivity@0.1%BER	**–80 dBm**
Technology	**TSMC 0.25 μm SP5M CMOS**

TABLE II
COMPARISON WITH PREVIOUS WORKS

	Low-IF Receiver Architecture	Current Consumption @ Supply	Chip Area (mm^2)	NF (dB)	S_{11} (dB)	CMOS (μm)
Current Art	Single-Conversion (10.7 MHz) ISM (915 MHz)	33 mA @ 3.3 V	6	5	–13	0.25
[24]	Dual-Conversion (1st-190 MHz;2nd-140 kHz) GSM (900 MHz)	30 mA @ 2.5 V	8.8	5	–4	0.35

V. CONCLUSION

This paper describes a tunable low-power fully integrated FSK receiver, which is a monolithic, single-chip receiver IC specially optimized for wireless consumer applications in the ISM band of 915 MHz. The IC offers a high level of integration such that minimal external components (e.g., the channel-select filter, the discriminator, and the loop filter) are required. With on-chip selective switches for resistive and capacitive load, the center frequency and gain of receiver front-end can be tunable against the process variation. The receiver's sensitivity under binary FSK demodulation is -80 dBm with IF bandwidth of 200 kHz.

ACKNOWLEDGMENT

The authors wish to thank Prof. G. Turner-Walker for his proofread.

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