Excess Low-Frequency Noise in Ultrathin Oxide n-MOSFETs Arising From Valence-Band Electron Tunneling

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***Abstract*—Low-frequency flicker noise in analog n-MOSFETs with 15-Å gate oxide is investigated. A new noise generation mechanism resulting from valence-band electron tunneling is proposed. In strong inversion conditions, valence-band electron tunneling from Si substrate to polysilicon gate takes place and results in the splitting of electron and hole quasi-Fermi-levels in the channel. The excess low-frequency noise is attributed to electron and hole recombination at interface traps between the two quasi-Fermi-levels. Random telegraph signals due to the capture of channel electrons and holes is characterized in a small area device to support our model.**

***Index Terms*—Low-frequency noise, random telegraph signal, ultrathin oxide MOSFET, valence-band tunneling.**

I. Introduction

CMOS technology, which possesses the advantages of low cost, high integration, and low power, is finding more and more important applications in the area of mixed-mode and RF ICs. As compared with bipolar transistors, CMOS devices exhibit large noise, especially in the low-frequency domain where flicker noise is dominant [1]. Drain current flicker noise has become one of the key considerations in device geometrical scaling since it will affect the signal-to-noise ratio in operational amplifiers and in analog/digital and digital/analog converters. In addition, low-frequency flicker noise can be upconverted to undesired phase noise in RF circuits [2] and limits the channel spacing in communication systems. In order to reduce low-frequency noise, the physical origin of flicker noise in today's CMOS devices with gate oxide in direct tunneling regime should be further explored.

The origin of low-frequency flicker noise in MOSFETs with relatively thick gate oxides has been extensively studied. A unified noise model [3], [4] based on oxide charge tunnel trapping and detrapping has been adopted. The carrier number and mobility fluctuation resulting from trapped oxide charges is thought to be the source of flicker noise. In addition, some studies showed that the low-frequency noise may result from charge emission and capture at interface traps in weak inversion condition or in the very high frequency regime of noise power spectral density [5]. As gate oxide thickness is scaled into direct tunneling domain, oxide trap density should be much reduced. In addition, channel electrons would likely tunnel through an ultrathin gate oxide directly without being captured by oxide traps. However, the low-frequency noise in ultrathin oxide CMOS devices still exhibits a $1/f$ spectrum and possesses a significant level [6], [7]. The traditional oxide charge tunnel trapping and detrapping concept seems no longer suitable to explain the noise behavior in ultrathin oxide MOSFETs. Recently, a study for ultrathin gate oxide fully depleted/partially depleted silicon-on-insulator (SOI) MOSFETs has shown that linear kink effect induced by valence-band electron tunneling would increase the low-frequency noise spectral density S_I [8]. In this paper, we observe another source of low-frequency noise in ultrathin gate oxide bulk n-MOSFETs arising from valence-band electron tunneling [9], [10]. Detailed discussion on the physical mechanism of this excess noise will be given.

The time domain presentation of low-frequency noise is known as random telegraph signal (RTS) and has been studied in past decades [11]–[14]. Due to a single charge trapping and detrapping in a small area device, RTS exhibits two levels. The upper level corresponds to an empty trap, i.e., no electron occupation, and the duration of time is denoted by τ_H. The lower level corresponds to an electron occupied state and is denoted by τ_L. In many cases, τ_H corresponds to the time it takes to capture an electron, while electron release (emission) from traps governs τ_L [15].

In this work, the low-frequency noise in a 15-Å gate oxide n-MOSFET is investigated. The electron trapping and detrapping times (τ_H and τ_L) are characterized from RTS in a small area n-MOSFET. The power spectral density of normalized drain current noise $\left(S_{id}/I_d^2\right)$ and gate referred voltage noise $(S_{\rm vg})$ is also measured. In addition, the RTS time constants and noise power spectral density in 33 Å oxide n-MOSFETs, where valence-band tunneling is insignificant, are characterized for comparison. The drain bias in RTS and noise measurement in this paper is 0.2 V to ensure a uniform charge distribution in the channel. Finally, a new noise source due to valence-band electron tunneling will be proposed to explain the observed noise behavior.

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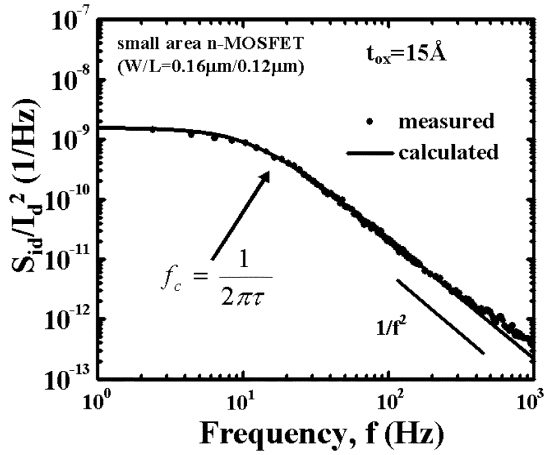

Fig. 1. Measured and calculated Lorentzian-like noise power spectral density in a small area n-MOSFET ($W/L = 0.16/0.12\ \mu$m, $t_{ox} = 15$ Å). The noise is measured at strong inversion ($V_d = 0.2$ V, $V_g = 1.1$ V). The cut-off frequency (f_c) is also shown in the figure.

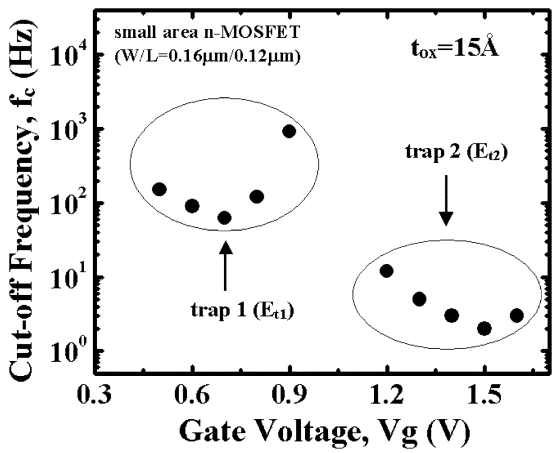

Fig. 2. Cut-off frequency versus gate voltage in a small area n-MOSFET ($W/L = 0.16/0.12\ \mu$m, $t_{ox} = 15$ Å). A trap (E_{t1}) is observed in weak inversion ($V_g \sim 0.7$ V) and another trap (E_{t2}) is in strong inversion ($V_g > 1.0$ V).

II. Results and Discussion

The noise characteristic in a small area ultrathin oxide n-MOSFET with a single trap time constant is first analyzed. Fig. 1 shows the measured and calculated noise power spectral density in a $W/L = 0.16/0.12\ \mu$m n-MOSFET. The gate oxide thickness is 15-Å. The noise has Lorentzian-like spectral distribution [15], characterized by a constant power spectral density at low frequencies and a roll-off with f^{-2} for high frequencies, .i.e.

$$S_{id} \propto \frac{\tau}{1+(2\pi f\tau)^2} \text{ and } \frac{1}{\tau} = \frac{1}{\tau_H} + \frac{1}{\tau_L}. \quad (1)$$

The cut-off frequency (f_c) corresponds to the 3-dB point of the spectrum and is related to the reciprocal characteristic time (τ) of the underlying trap ($f_c = 1/2\pi\tau$). The calculated result (solid line in Fig. 1) is based on τ_H and τ_L extracted from associated RTS (will be shown later) and is in good agreement with the measured power spectral density. Fig. 2 shows the gate voltage (V_g) dependence of f_c. Obviously, there exist two groups of trap frequency (or two trap energy levels) with one (E_{t1}) observed

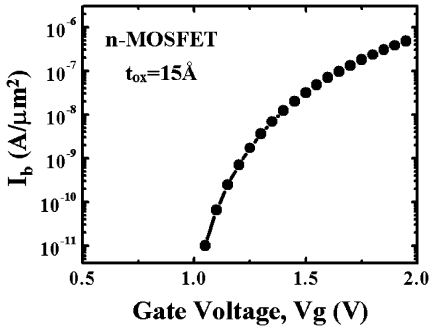

Fig. 3. Substrate current (I_b) versus gate voltage in a 15-Å oxide n-MOSFET. The I_b in the 15-Å oxide device drastically increases for $V_g > 1.0$ V (strong inversion regime), which indicates the occurrence of valence-band electron tunneling.

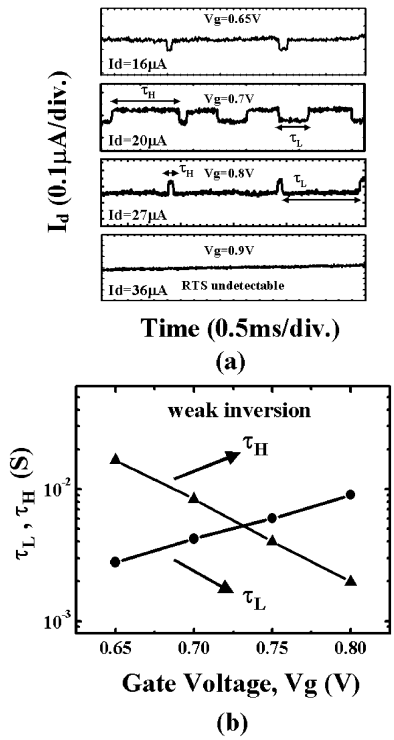

Fig. 4. (a) Typical RTS patterns at various gate voltages from $V_g = 0.65$ to 0.9 V in a small area n-MOSFET ($W/L = 0.16/0.12\ \mu$m, $t_{ox} = 15$ Å). RTS is undetectable at $V_g = 0.9$ V. (b) Average τ_L and τ_H (extracted from RTS) versus gate voltage in weak inversion regime.

in weak inversion ($V_g < 0.9$ V) and the other (E_{t2}) in strong inversion ($V_g > 1$ V). Furthermore, significant substrate current arises in the 15-Å oxide device in strong inversion regime ($V_g > 1$ V) in Fig. 3 because valence-band electron tunneling from the Si substrate to the polysilicon gate occurs and generated holes flow to the substrate [16].

Fig. 4(a) shows typical RTS patterns in a small area ($W/L = 0.16/0.12\ \mu$m) 15-Å gate oxide n-MOSFET in weak inversion ($V_g < 0.9$ V). As can be seen, τ_L increases and τ_H decreases as V_g increases from 0.65 to 0.9 V. Noticeably, RTS vanishes at $V_g = 0.9$ V in our measurement period. Fig. 4(b) shows the V_g dependence of average τ_L and τ_H (extracted from RTS) in weak inversion regime. The τ_L and τ_H in weak inversion correspond to the electron emission and capture times at the interface trap E_{t1}, as illustrated in Fig. 5(a). As V_g increases, τ_H

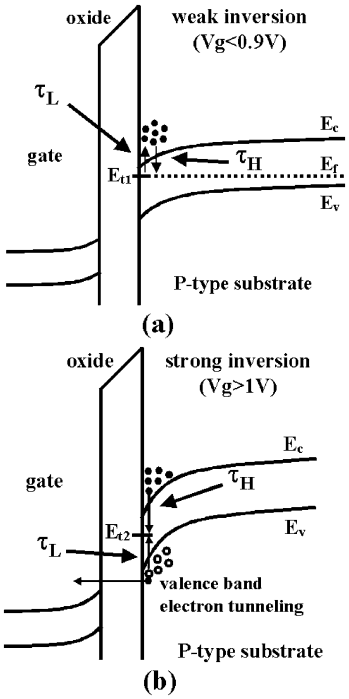

Fig. 5. (a) Band bending in weak inversion. The RTS results from electron capture (τ_H) and electron emission (τ_L) through the interface trap E_{t1}. (b) Band bending in strong inversion. The RTS results from electron capture (τ_H) and hole capture (τ_L) at E_{t2}. Channel hole creation due to valence-band electron tunneling is shown.

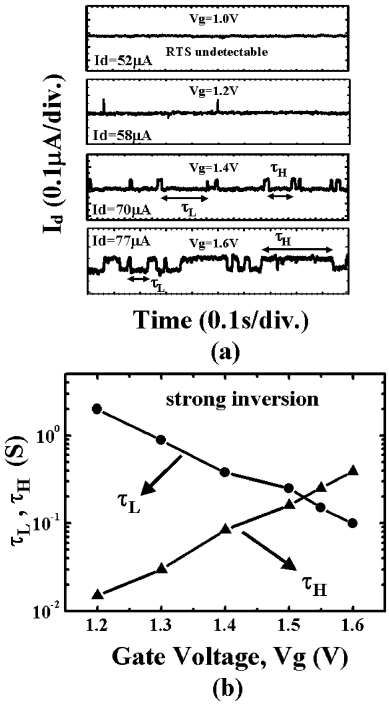

Fig. 6. (a) Typical RTS patterns at various gate voltages from $V_g = 1.0$ to 1.6 V in a small area n-MOSFET ($W/L = 0.16/0.12$ μm, $t_{ox} = 15$ Å). (b) Average τ_L and τ_H (extracted from RTS) versus gate voltage in strong inversion regime.

decreases and τ_L increases because of a larger channel electron population and thus a smaller electron capture time. Our result here is consistent with the findings for thicker gate oxides in previous publications [11]. In contrast, Fig. 6(a) shows the RTS patterns in strong inversion from $V_g = 1.0$ to 1.6 V. The RTS is still undetectable at $V_g = 1$ V and reappears for $V_g > 1$ V. Fig. 6(b) shows the V_g dependence of average τ_L and τ_H. Interestingly, we find that the RTS patterns in strong inversion regime ($V_g > 1$ V) exhibit an opposite trend. The V_g dependence of τ_H and τ_L in strong inversion is opposite to that in weak inversion. We repeated our measurement on different samples and the opposite trend of the V_g dependence is always obtained. Although the mobility fluctuation theory [17] can possibly explain the above opposite gate bias dependence of τ_H and τ_L from weak inversion to strong inversion, further analysis shows that number fluctuation should dominate in the entire range of our measurement gate bias. According to the calculated result in [17, Fig. 3], number fluctuation is dominant in the V_g range until $\Delta I_d/I_d$ changes sign. In our case, the measured $\Delta I_d/I_d$ versus V_g is shown in Fig. 7. The $\Delta I_d/I_d$ decreases with gate voltage but does not change sign in the entire range of measurement V_g.

In order to find out the cause of the opposite charge trapping and detrapping behavior from weak inversion to strong inversion, the trap electron occupation factor (f_t) is analyzed. The f_t can be evaluated as follows:

$$f_t = \frac{\tau_L}{\tau_L + \tau_H}. \tag{2}$$

Fig. 8(a) shows f_t versus V_g from weak inversion to strong inversion. In weak inversion regime (i.e., $V_g < 0.9$ V), gate oxide

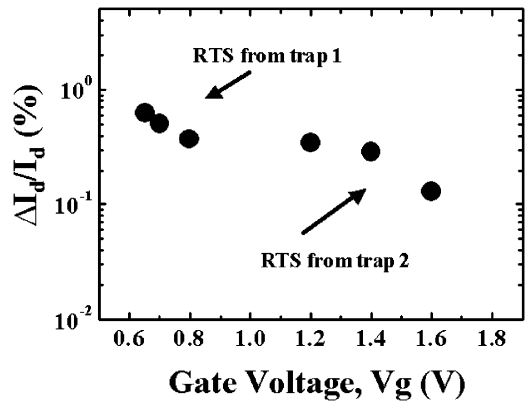

Fig. 7. $\Delta I_d/I_d$ versus measurement gate bias. The $\Delta I_d/I_d$ is extracted from the measured RTS.

tunneling is insignificant and the channel is in thermal equilibrium. f_t increases with V_g because of a larger band-bending. As f_t increases to 1, RTS is undetectable since the trap is always occupied by an electron. However, when V_g increases above 1.1 V, f_t begins to decline from unity with increasing V_g. This means, at a larger V_g, although the energy level of the interface trap moves more deeply with respect to the electron Fermi level, the chance of the trap being occupied by an electron is smaller. This result is obviously contradicting to the equilibrium case that $f_t(= 1/(1 + \exp(E_t - E_F)/kT))$ should increase as the trap energy becomes more negative with respect to the Fermi level. In other words, the Si channel in strong inversion should be in nonequilibrium condition and the cause is valence-band electron tunneling.

In addition to f_t, Fig. 8(b) shows the S_{id}/I_d^2 (measured at $f = 100$ Hz in a small area n-MOSFET) from weak inversion to

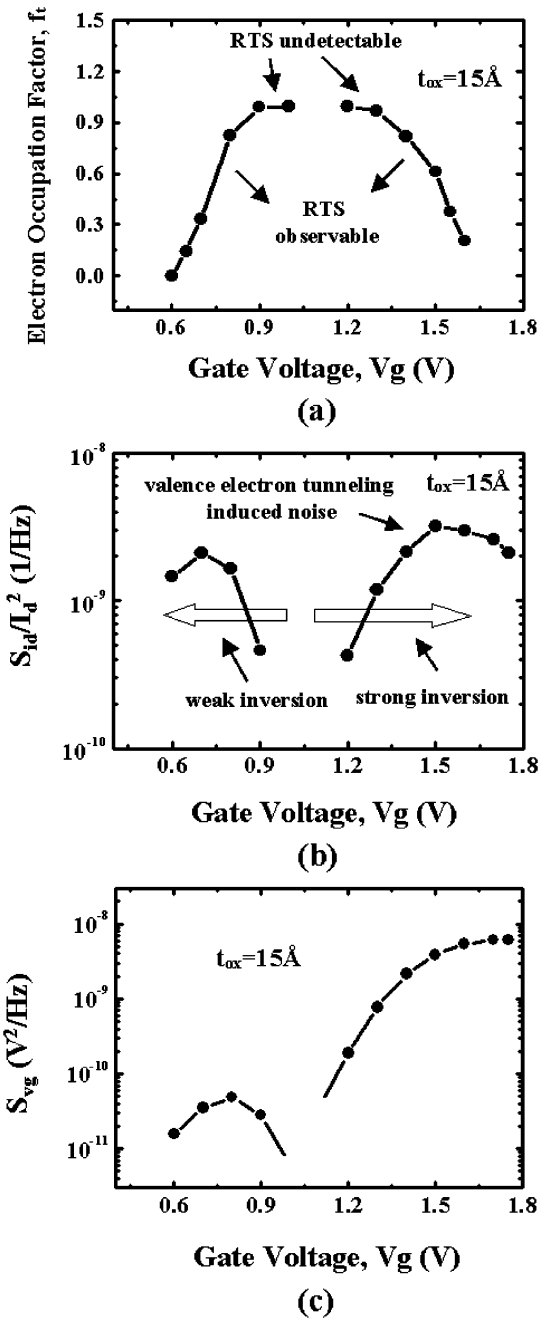

Fig. 8. (a) Electron occupation factor (f_t), (b) normalized drain current noise, and (c) gate referred voltage noise (measured at $f = 100$ Hz) versus gate voltage in a small area n-MOSFET ($W/L = 0.16\,\mu$m$/0.12\,\mu$m, $t_{ox} = 15$ Å).

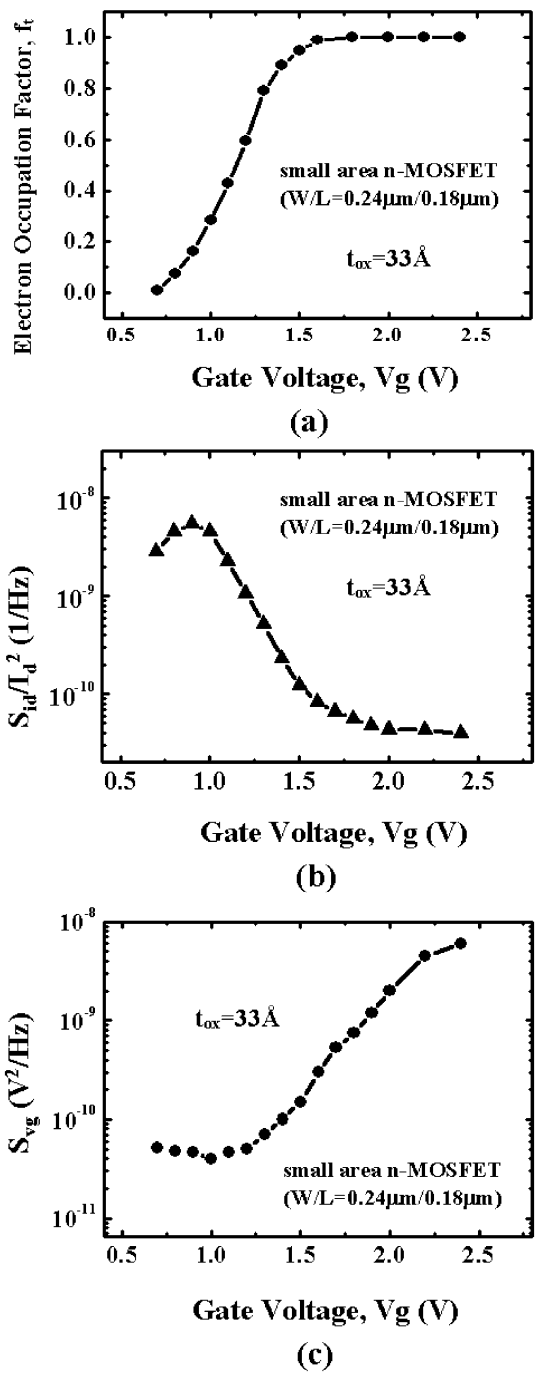

Fig. 9. (a) Electron occupation factor (f_t), (b) normalized drain current noise, and (c) gate referred voltage noise (measured at $f = 100$ Hz) versus gate voltage in a small area n-MOSFET ($W/L = 0.24/0.18\,\mu$m, and $t_{ox} = 33$ Å).

strong inversion. The readers should be reminded that according to (1) S_{id}/I_d^2 should have a peak around $f_t = 0.5$, where τ_L is equal to τ_H and thus τ reaches a maximum. In Fig. 8(a), f_t is 0.5 around $V_g = 0.75$ V (weak inversion) and 1.5 V (strong inversion). Thus, S_{id}/I_d^2 in Fig. 8(b) exhibits two peaks at the above two V_g. Fig. 8(c) shows the measured $S_{\rm vg}$ as well. Again, the double hump feature is noticed.

The possible explanation for the abnormal noise behavior in strong inversion is illustrated in Fig. 5(b). In strong inversion regime, a large V_g causes strong valence electron tunneling and leaves generated holes behind in the channel. The channel is thus in nonequilibrium. τ_H and τ_L then correspond to electron capture time and hole capture time respectively, as illustrated in Fig. 5(b). Because of the increased channel hole concentration at a larger V_g, τ_L is smaller. The nonequilibrium carrier distribution also results in the splitting of electron and hole quasi-Fermi-levels. An interface trap (E_{t2}) between the two quasi- Fermi levels can serve as the recombination center of electrons and holes. As a result, the local electron concentration in the vicinity of the trap is reduced and τ_H increases. The increase of τ_H and the decrease of τ_L lead to a reduced f_t. The second peak of S_{id}/I_d^2 in strong inversion condition $(V_g > 1\,\text{V})$ in Fig. 8(b) therefore can be well explained. The authors also would like to remark that the Si substrate trap density in bulk

MOSFETs is around 10^{14} cm^{-3} [18], or 10^{8} cm^{-2} by assuming a substrate depletion region width of 10 nm. Although we cannot completely exclude the possibility that the traps stay in the silicon depletion region, the probability that the traps are in the depletion region is very small, as compared to a typical interface trap density of 10^{10} cm^{-2}.

For comparison, the f_t and the noise power density versus V_g in a thicker gate oxide (33 Å) n-MOSFET are also characterized. The result is shown in Fig. 9. The f_t stays at unity in strong inversion. Neither RTS nor the double hump feature in noise power density is observed in strong inversion since valence-bane tunneling is insignificant in such thick gate oxide devices.

III. Conclusion

We identified two low-frequency noise sources in ultrathin oxide (15-Å) n-MOSFETs. In weak inversion, the noise arose from electron capture and emission at a shallower interface trap. In strong inversion, we observed an abnormal increase in low-frequency noise. This abnormal noise behavior is not observed in a thicker gate oxide (33 Å) device, where valence-band tunneling is insignificant. The traditional flicker noise model based on oxide charge tunnel trapping/detrapping cannot account for this excess low-frequency noise. The analysis of RTS patterns and trap occupation factor reveals that the channel is in nonequilibrium at a large gate voltage due to valence-band tunneling. The increased channel hole concentration and a Fermi-level splitting caused by valence-band electron tunneling should be responsible for the excess low-frequency noise.

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References

[1] A. van der Ziel, *Noise in Solid State Devices and Circuits*. New York: Wiley, 1986.

[2] A. Hajimiri and T. H. Lee, "A general theory of phase noise in electrical oscillators," *IEEE J. Solid-State Circuits*, vol. 33, no. 2, pp. 179–194, Mar. 1998.

[3] K. K. Hung, P. K. Ko, C. Hu, and Y. C. Cheng, "A unified model for the flicker noise in metal–oxide–semiconductor field-effect transistors," *IEEE Trans. Electron Devices*, vol. 37, no. 5, pp. 654–665, May 1990.

[4] ——, "A physics-based MOSFET noise model for circuit simulators," *IEEE Trans. Electron Devices*, vol. 37, no. 10, pp. 1323–1333, Oct. 1990.

[5] M. H. Tsai and T. P. Ma, "$1/f$ noise in hot-carrier damaged MOSFETs: Effects of oxide charge and interface traps," *IEEE Electron Device Lett.*, vol. 14, no. 4, pp. 256–258, Apr. 1993.

[6] M. J. Knitel, P. H. Woerlee, A. J. Scholten, and A. T. A. Zegers-Van Duijnhoven, "Impact of process scaling on $1/f$ noise in advanced CMOS technologies," in *IEDM Tech. Dig.*, 2000, pp. 463–466.

[7] H. S. Momose, H. Kimijima, S.-I. Ishizuka, Y. Miyahara, T. Ohguro, T. Yoshitomi, E. Morifuji, S.-I. Nakamura, T. Morimoto, Y. Katsumata, and H. Iwai, "A study of flicker noise in n- and p-MOSFETs with ultrathin gate oxide in the direct-tunneling regime," in *IEDM Tech. Dig.*, 1998, pp. 923–926.

[8] A. Mercha, J. M. Rafí, E. Simoen, E. Augendre, and C. Claeys, "'Linear kink effect' induced by electron valence-band tunneling in ultrathin gate oxide bulk and SOI MOSFETs," *IEEE Trans. Electron Devices*, vol. 50, no. 11, pp. 1675–1682, Nov. 2003.

[9] J. W. Wu, J. W. You, H. C. Ma, C. C. Cheng, C. S. Chang, G. W. Huang, and T. Wang, "Valence-band tunneling induced low-frequency noise in ultrathin oxide (15-Å) n-type metal–oxide–semiconductor field effect transistors," *Appl. Phys. Lett.*, vol. 85, pp. 5076–5077, 2004.

[10] J. W. Wu, H. C. Ma, C. C. Cheng, G. W. Huang, C. S. Chang, and T. Wang, "Low frequency noise degradation in ultrathin oxide (15-Å) analog nMOSFETs resulting from valence-band tunneling," in *Proc. Int. Reliab. Phys. Symp.*, 2005, pp. 260–264.

[11] K. Kandiah, M. O. Deighton, and F. B. Whiting, "A physical model for random telegraph signal currents in semiconductor devices," *J. Appl. Phys.*, vol. 66, pp. 937–948, 1989.

[12] N. V. Amarasinghe and Z. Çelik-Butler, "Complex random telegraph signals in 0.06 μm^2 MDD n-MOSFETs," *Solid State Electron.*, vol. 44, pp. 1013–1019, 2000.

[13] Z. Çelik-Butler and F. Wang, "Effects of quantization on random telegraph signals observed in deep-submicron MOSFETs," *Microelectron. Reliab.*, vol. 40, pp. 1823–1831, 2000.

[14] G. Ghibaudo and T. Boutchacha, "Electrical noise and RTS fluctuations in advanced CMOS devices," *Microelectron. Reliab.*, vol. 42, pp. 573–582, 2002.

[15] E. Simoen and C. Claeys, "Random telegraph signal: A local probe for single point defect studies in solid-state devices," *Mater. Sci. Eng.*, vol. B91-92, pp. 136–143, 2002.

[16] C. W. Tsai, S. H. Gu, L. P. Chiang, and T. Wang, "Valence-band tunneling enhanced hot carrier degradation in ultrathin oxide nMOSFETs," in *IEDM Tech. Dig.*, 2000, pp. 139–142.

[17] S. T. Martin, G. P. Li, E. Worley, and J. White, "The gate bias and geometry dependence of random telegraph signal amplitudes," *IEEE Trans. Electron Devices*, vol. 18, no. 3, pp. 444–446, Mar. 1997.

[18] D. S. Ang, Z. Lun, and C. H. Ling, "Generation-recombination noise in the near fully depleted SIMOX SOI nMOSFETs—Physical characteristics and modeling," *IEEE Trans. Electron Devices*, vol. 50, no. 12, pp. 2490–2498, Dec. 2003.

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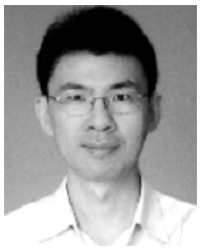

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