Native-NMOS-Triggered SCR With Faster Turn-On Speed for Effective ESD Protection in a 0.13-μm CMOS Process

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***Abstract*—In order to quickly discharge the electrostatic discharge (ESD) energy and to efficiently protect the ultrathin gate oxide, a novel native-negative-channel metal oxide semiconductor (NMOS)-triggered silicon-controlled rectifier (NANSCR) is proposed for on-chip ESD protection in a 0.13-μm complementary metal oxide semiconductor (CMOS) process with a voltage supply of 1.2 V. The proposed NANSCR can be designed for the input, output, and power-rail ESD protection circuits without latchup danger. A new whole-chip ESD protection scheme realized with the proposed NANSCR devices is also demonstrated with the consideration of pin-to-pin ESD stress. From the experimental results, the trigger voltage, holding voltage, turn-on resistance, turn-on speed, and charged-device-model (CDM) ESD level of NANSCR can be greatly improved, as compared with the traditional low-voltage-triggering SCR (LVTSCR). Under transmission line pulsing (TLP) stress, the gate leakage current of the gate monitor device protected by the proposed NANSCR is monitored after each TLP pulse, whereas the gate leakage current is not obviously increased. Therefore, the ultrathin gate oxide of the input stage can be safely protected by the new proposed NANSCR against ESD stress in the nanoscale CMOS technology.**

***Index Terms*—Charged device model (CDM), electrostatic discharge (ESD), native NMOS, silicon-controlled rectifier (SCR).**

I. Introduction

ELECTROSTATIC discharge (ESD) is a transient process of high energy transformation from the external to the internal integrated circuit (IC) when the IC is floated. Total discharge process of a human-body-model (HBM) [1] ESD event takes only about 100 ns. Several hundred volts, or even several thousand volts, are transferred during ESD stress. Such high energy transformation will rupture the gate oxide of the input stage and further cause the malfunctions of internal circuits. For complementary metal oxide semiconductor (CMOS) IC applications with maximum supply voltage of 1.2 V, the silicon-controlled rectifier (SCR) can be a great candidate for on-chip ESD protection due to its highest ESD robustness, smallest layout area, and free to latchup issue, as compared with other ESD protection devices [such as the diode, metal oxide semiconductor (MOS), bipolar junction transistor (BJT), or field-oxide device]. However, the SCR still has a higher trigger voltage of $\sim$ 18 V in a 0.13-μm CMOS process, which is generally greater than the gate-oxide breakdown voltage of the input stages. Furthermore, the gate-oxide thickness has been scaled down to only $\sim$ 25 Å, and its time-to-breakdown (t_{BD}) or charge-to-breakdown (Q_{BD}) will also be decreased in the same CMOS process. Hence, it is imperative to reduce the trigger voltage of SCR and to enhance the turn-on speed of SCR for efficiently protecting the ultrathin gate oxide from latent damage or rupture [2], especially against the fast charged-device-model (CDM) [3] ESD events. To provide a more effective on-chip ESD protection, the modified lateral SCR (MLSCR) [4] and the low-voltage-triggering SCR (LVTSCR) [5], [6] were invented to reduce the trigger voltage of the SCR device. Moreover, some advanced circuit techniques had also been reported to further reduce the trigger voltage and enhance the turn-on speed of the SCR device, such as the gate-coupled technique [7], the substrate-triggered technique [8], [9], and the gate-grounded NMOS (GGNMOS)-triggered technique [10].

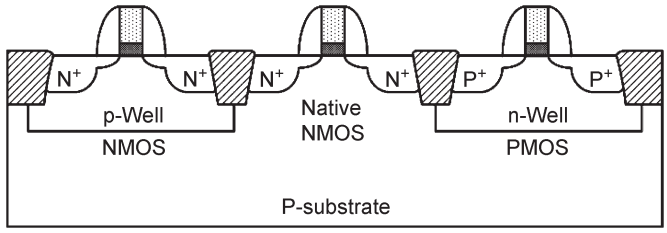

Fig. 1. Device cross-sectional views of the NMOS, PMOS, and native NMOS in a P-substrate twin-well CMOS technology.

In this paper, based on the substrate-triggered technique [8], a native NMOS with almost zero threshold voltage, which is an optional device in a 0.13-μm CMOS process without adding extra mask, is first used to trigger on the SCR device during ESD events. The novel native-NMOS-triggered SCR (NANSCR) has the lower trigger voltage, smaller turn-on resistance, lower holding voltage, faster turn-on speed, and higher CDM ESD level than those of a traditional LVTSCR; therefore, it is more suitable to protect the ultrathin gate oxide. The NANSCR can be used in the input, output, power-rail, and whole-chip ESD protection circuits without latchup danger in CMOS IC applications with a voltage supply of 1.2 V.

II. Device Characteristics of NANSCR

The native NMOS is directly built in a lightly doped p-type substrate, whereas the normal NMOS [positive-channel MOS

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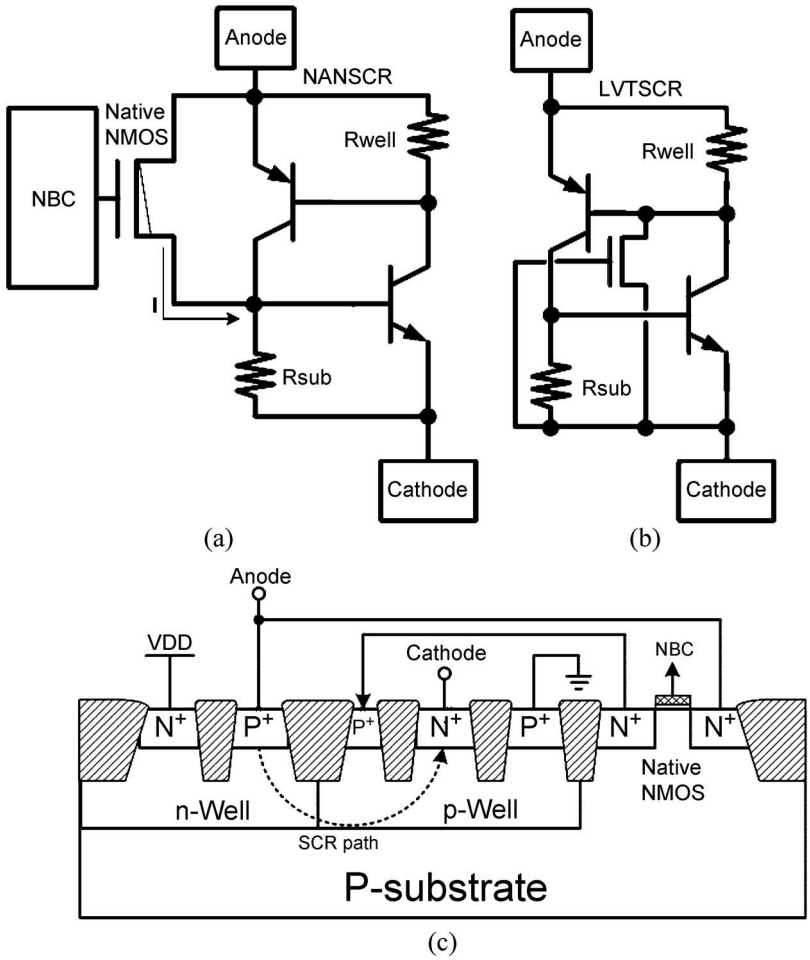

Fig. 2. Circuit schematics of (a) the proposed NANSCR and (b) the traditional LVTSCR. (c) Device cross-sectional view of NANSCR.

(PMOS)] is in a heavily doped p-well (n-well) in a P-substrate twin-well CMOS technology, as shown in Fig. 1. The native NMOS is fully compatible with the standard CMOS process without adding extra mask. The threshold voltage of native NMOS is almost zero ($\sim$ 0.1 V); however, that of normal NMOS is about 0.34 V in a 0.13-μm CMOS process. The native NMOS and lateral SCR are merged together to be a novel ESD protection device (NANSCR), which is first proposed in the literature. The circuit schematics of NANSCR and LVTSCR are shown in Fig. 2(a) and (b), respectively. The drain of native NMOS in NANSCR is directly coupled to the pad of the anode, but the drain of NMOS in LVTSCR is located across the n-well/P-substrate junction of the SCR device. The gate of native NMOS is connected to a negative bias circuit (NBC) [11] to turn off the NANSCR, but the gate of NMOS in LVTSCR is connected to VSS to ensure that LVTSCR is off, under normal circuit operating conditions. Fig. 2(c) shows the cross-sectional view of the NANSCR device. The spacing between the P+-anode edge and the n-well edge and the spacing between the n-well edge and the N+-cathode edge are 1 μm (i.e., the spacing between anode and cathode is 2 μm). The spacing between the N+ cathode and the P+ guardring is 3 μm. A P+ diffusion is inserted between the n-well edge and the N+ cathode as the trigger node, which is connected to the source terminal of the native NMOS.

The NBC is formed with a clock generator, capacitors, and diodes. The clock generator is used to provide the charge-pump source. The output negative voltage of the NBC is dependent on the voltage amplitude of the clock generator and the cut-in voltages of diodes, which can be tuned to fulfill various applications [11]. For avoiding the large power-on transient leakage current from VDD through the native NMOS to VSS, the rise time of VDD, the clock generator, and the capacitance should be properly designed. In addition, a decoupling capacitor or a shielding guardring can be added to reduce the noise interference into the NBC circuit.

Under an ESD event, the NBC is initially floating, so the native NMOS is an already-on device that draws some ESD current from the pad of the anode to bias the SCR device. When a trigger current through the native NMOS is applied into the base (P-substrate) of the NPN in Fig. 2(a), the base voltage of the NPN will be raised up due to the substrate resistor (Rsub). As long as the base voltage of the NPN is greater than 0.7 V, the NPN bipolar transistor in the SCR structure is active. The collector current of the NPN is generated to bias the PNP bipolar transistor. If the voltage drop across the well resistor (Rwell) is greater than 0.7 V, the PNP bipolar transistor in the SCR structure is also active. When the PNP transistor is turned on, the collector current of the PNP is, in turn, generated to further bias the NPN transistor. The positive feedback regeneration

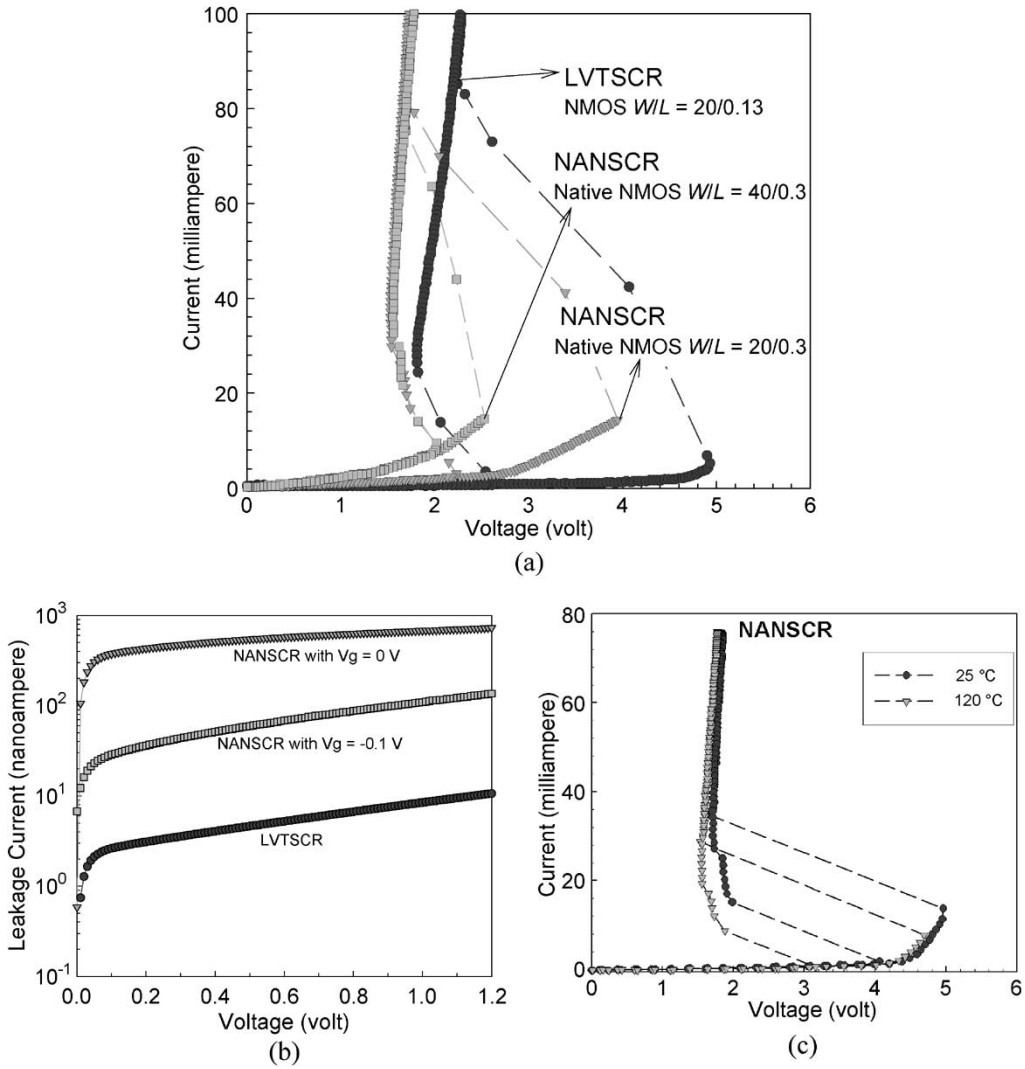

Fig. 3. (a) DC $I-V$ curves and (b) leakage currents of the NANSCR and LVTSCR. (c) DC $I-V$ curves of NANSCR under different temperatures.

mechanism of the SCR latching process [12], [13] is initiated by the trigger current of the already-on native NMOS in the NANSCR structure. Finally, the NANSCR will be successfully triggered on into its latching state to discharge the ESD current.

The new proposed NANSCR device and the traditional LVTSCR device have been fabricated in a 0.13-μm silicided CMOS process. Both of them are fully silicided devices without the extra silicide-blocking mask. In the experimental test chip, the active area (without including the guard rings) of SCR in the NANSCR is drawn as 20×8 μm^2. The active area of LVTSCR is drawn as 20×7.5 μm^2, and the W/L of NMOS within the LVTSCR is 20 μm/0.13 μm. The comparison of DC $I-V$ curves between the NANSCR and LVTSCR is shown in Fig. 3(a) at room temperature. The native NMOS in the NANSCR structure has two different device dimensions of 20 μm/0.3 μm and 40 μm/0.3 μm for comparison. With the substrate-triggered technique [8], the trigger voltage of the NANSCR with the native NMOS of the 20-μm channel width is about $\sim$ 4 V, which is smaller than that of the LVTSCR ($\sim$ 5 V). Hence, the NANSCR can be triggered on faster than the LVTSCR. Moreover, if the channel width of the native NMOS in the NANSCR is increased from 20 to 40 μm, the trigger voltage of the NANSCR with the native NMOS of the 40-μm channel width can be further reduced to only $\sim$ 2.5 V. The NANSCR with lower trigger voltage can clamp ESD overstress voltage more quickly. The turn-on resistance and holding voltage of the NANSCR are also smaller than those of the LVTSCR in Fig. 3(a). Therefore, the voltage on the pad clamped by the NANSCR device will be lower than that clamped by the LVTSCR device under the same ESD stress. Fig. 3(b) shows the leakage currents of the LVTSCR and the NANSCR under different gate biases at room temperature. The W/L of the native NMOS in the NANSCR is 20 μm/0.3 μm in Fig. 3(b). The leakage current of the NANSCR can be reduced under normal circuit operating conditions, when the gate of the native NMOS is biased at -0.1 V. The measured $I-V$ curves of the NANSCR under different temperatures are shown in Fig. 3(c). When the temperature is increased from 25 to 120 °C, the holding voltage of the NANSCR is reduced from $\sim$ 1.6 to $\sim$ 1.5 V, which is still greater than the VDD + 10%. Therefore, the NANSCR still has high enough latchup immunity in a 0.13-μm CMOS process with a supply voltage of 1.2 V.

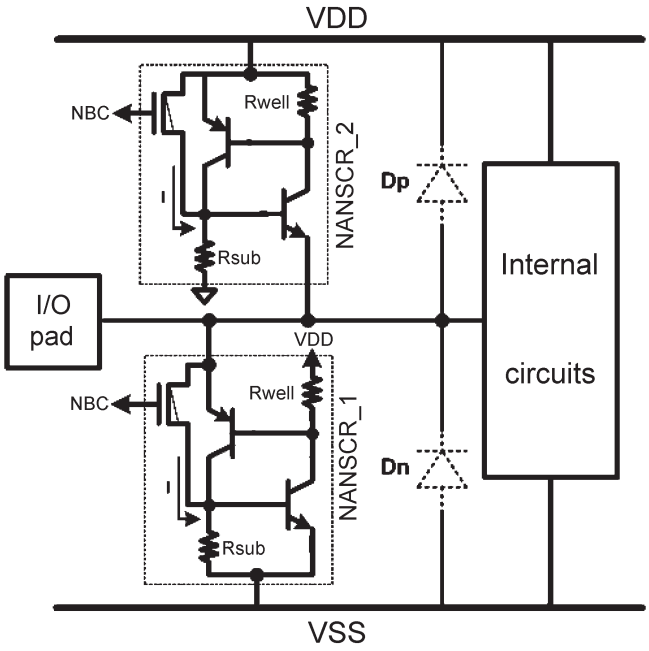

Fig. 4. Design of ESD protection circuit for the input or output pads with the proposed NANSCR devices.

III. On-Chip ESD Protection Design With NANSCR

A. ESD Protection Circuit for Input/Output (I/O) Pads

The ESD protection circuit for input or output pads, which is realized with NANSCR devices, is shown in Fig. 4. The NANSCR devices are placed between the I/O pad and VDD/VSS power lines. The n-well in the NANSCR_1 is connected to VDD but not connected to the I/O pad. The gates of the native NMOS in the NANSCR_1 and NANSCR_2 are connected to the same NBC. The parasitic diode Dp is the p+-to-n-well (VDD) diode in the NANSCR_1 structure. The parasitic diode Dn is the n-well-to-P-substrate (VSS) diode in the NANSCR_2 structure.

Under normal circuit operating conditions, the gates of the native NMOS in all NANSCR devices are biased by the same NBC to turn off the NANSCR devices. Therefore, the NANSCR devices (NANSCR_1 and NANSCR_2) will not interfere with the functions of I/O circuits, whenever the I/O signals are logic high (VDD) or logic low (VSS). Because the holding voltage of NANSCR ($\sim$ 1.6 V) is greater than the maximum voltage level (1.2 V) of the I/O signals, the transient-induced latchup issue in such NANSCR devices is vanished.

Under the positive-to-VSS (PS) ESD-zapping condition (with grounded VSS but floating VDD), the gate of the native NMOS in the NANSCR_1 is floating. The NANSCR_1 is triggered on quickly by the substrate-triggering current generated from the native NMOS. Therefore, the positive ESD current can be effectively discharged from the I/O pad through the NANSCR_1 to the grounded VSS line. Under the negative-to-VDD (ND) ESD-zapping condition (with grounded VDD but floating VSS), the gate of the native NMOS in the NANSCR_2 is floating but with an initial voltage level of 0 V. The negative ESD voltage at the I/O pad will pull down the source voltage of the native NMOS through the base–emitter junction of the NPN in the NANSCR_2 device. Therefore, the native NMOS in NANSCR_2 will be turned on first, resulting in the NANSCR_2 being triggered on quickly. The negative ESD current will be discharged from the I/O pad through the NANSCR_2 to the grounded VDD line. For the negative-to-VSS (NS) [positive-to-VDD (PD)] ESD-zapping condition, the parasitic diode Dn (Dp) is forward biased to discharge the negative (positive) ESD current. Thus, the four modes (PS, NS, PD, and ND) of ESD stresses on the I/O pad can be clamped to a very low voltage level by the NANSCR_1, Dn, Dp, and NANSCR_2, respectively. The ultrathin gate oxide of internal circuits can be fully protected by this design with the new proposed NANSCR devices.

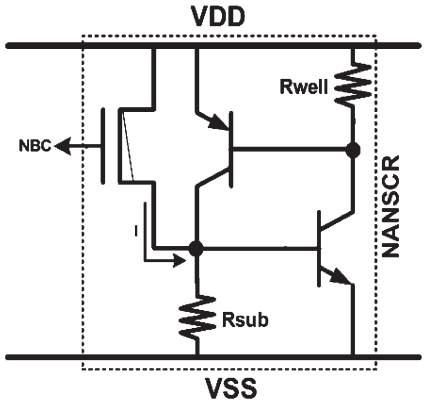

Fig. 5. VDD-to-VSS ESD clamp circuit realized with the NANSCR device.

B. ESD Clamp Circuit Between Power Rails

The VDD-to-VSS ESD clamp circuit realized with the NANSCR device is shown in Fig. 5. Under normal circuit operating conditions, the NBC is active to turn off the NANSCR device. Hence, the NANSCR device between the power lines will neither degrade the VDD power-on condition nor interfere with the functions of the internal circuit. Under ESD stress conditions, the NBC is inactive. No negative bias is applied to the gate of the native NMOS in the NANSCR. When a positive ESD pulse is applied on the VDD line with the grounded VSS line, the NANSCR device will be quickly triggered on by the already-on native NMOS to discharge the positive ESD current to the grounded VSS line. If a negative ESD pulse is applied on the VDD line with the grounded VSS line, the parasitic diode (P-substrate/n-well junction) in the NANSCR structure will be forward biased to discharge the negative ESD current. With the power-rail ESD clamp circuit, the positive ESD current on the I/O pad in Fig. 4 can be partially discharged by another current path, which is from the I/O pad, forward-biased diode (Dp), through the power-rail ESD clamp circuit, to the grounded VSS line under the PS ESD-zapping condition. For the ND ESD-zapping condition, the negative ESD current on the I/O pad can also be partially discharged through the current path, which is from the I/O pad, forward-biased diode (Dn), the power-rail ESD clamp circuit, to the grounded VDD line. The ESD robustness can be greatly improved, and the layout area of

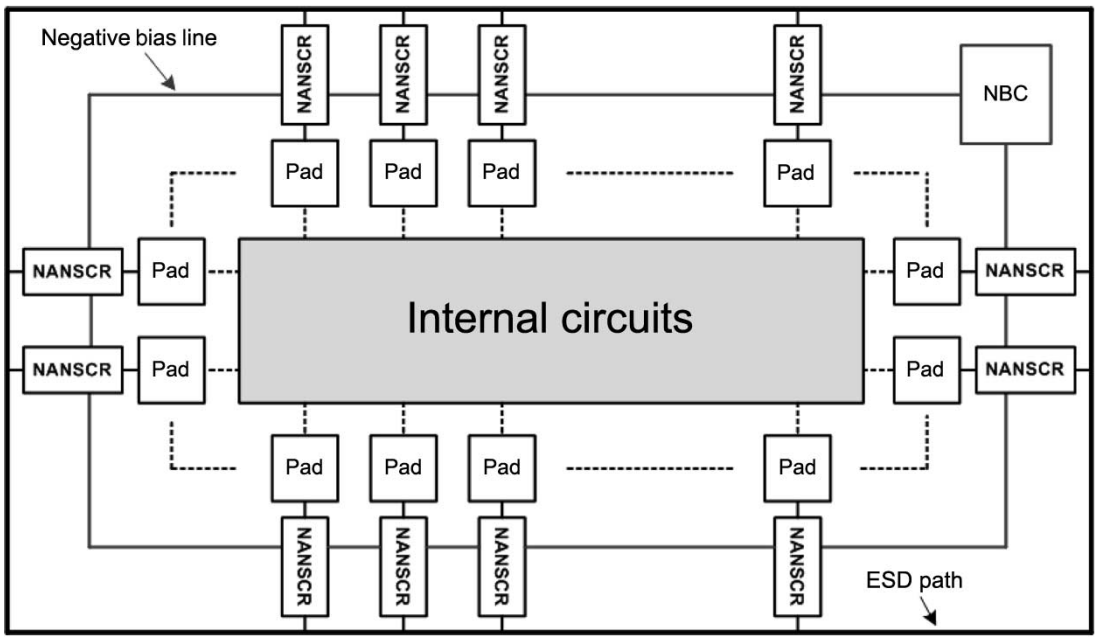

Fig. 6. New whole-chip ESD protection scheme realized with the NANSCR devices.

the NANSCR devices used in the I/O stages can be further reduced, while the power-rail ESD clamp circuit is added.

C. Whole-Chip ESD Protection Scheme

A new whole-chip ESD protection scheme with the proposed NANSCR devices is shown in Fig. 6. The anode terminals of the NANSCR devices are all connected to the pads (including I/O, VDD, and VSS pads), and their cathode terminals are all connected to the ESD path. The ESD path indicated by the bold line in Fig. 6 can be realized with the wide and top metal line in the chip to efficiently discharge the ESD current of several amperes during ESD events. To further save layout area in the chip, such ESD path can be merged with the seal ring of the chip. The gates of the native NMOS in the NANSCR devices are biased by an on-chip NBC [11] to fully turn off all NANSCR devices under normal circuit operating conditions. During the ESD-zapping condition, the NANSCR devices without negative bias in the whole-chip ESD protection scheme can be triggered on more quickly to effectively protect the internal circuits. Except for the four modes of ESD stresses on the I/O pads with VDD or VSS grounded, all pin-to-pin ESD-zapping conditions [such as input-to-input, output-to-output, input-to-output, or VDD (VSS)-to-VDD (VSS)] can be fully protected by this whole-chip ESD protection scheme. For example, when an ESD pulse is zapping on an input pad (In_1) and another input pad (In_2) is relatively grounded, the ESD current will be conducted from the In_1 pad to the common ESD path through the NANSCR device. As long as the voltage level of the ESD path is raised up, the parasitic diode (P-substrate/n-well junction) in another NANSCR structure connected to In_2 will be forward biased. Hence, the ESD current on the In_1 can be discharged from the In_1 through the NANSCR to the common ESD path and the parasitic diode

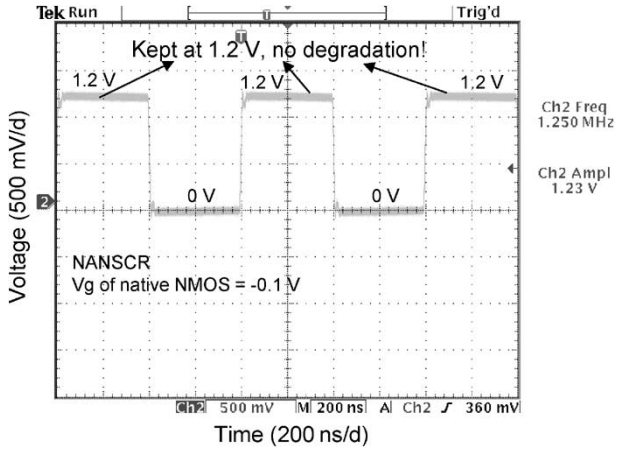

Fig. 7. Measured voltage waveform of input signal on the pad with the NANSCR device under normal circuit operating conditions when a 1.2-V voltage signal is applied to the pad.

in another NANSCR to the grounded In_2. By using this new whole-chip ESD protection scheme, the pin-to-pin ESD stress can be discharged through only a NANSCR, the ESD path, and a parasitic diode between the zapping pin and the grounded pin. For ultra-large-scale CMOS ICs with multiple power pins, this new proposed whole-chip ESD protection scheme with the NANSCR devices and common ESD path is an overall solution to discharge all modes of ESD stresses quickly and efficiently.

IV. Experimental Results

A. Turn-On Verification

The measured voltage waveform of the input signal on the pad with the NANSCR as an ESD protection device under normal circuit operating condition is shown in Fig. 7. The

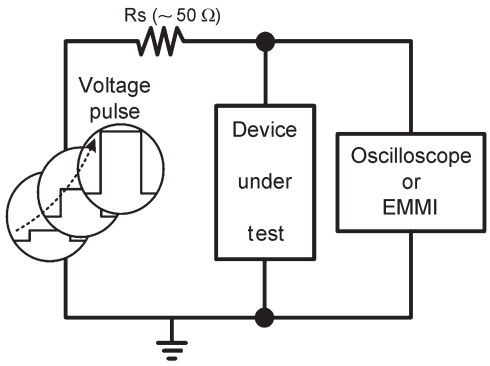

Fig. 8. Experimental setup to measure the turn-on speed or EMMI photograph of turn-on behavior among ESD devices.

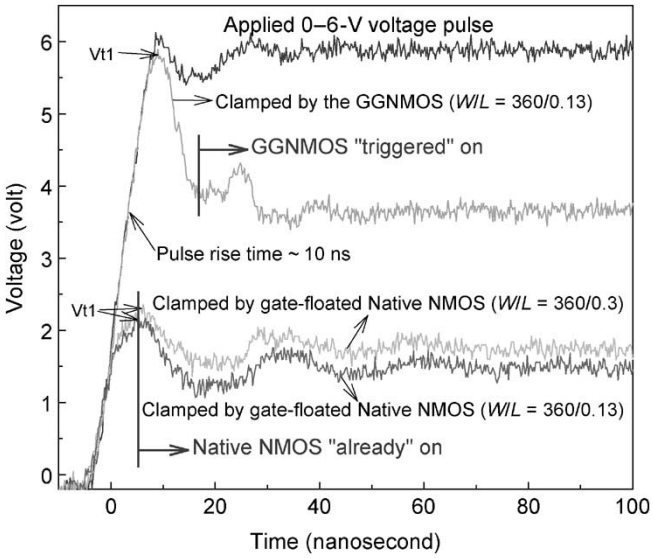

Fig. 9. Comparison of turn-on speeds between the GGNMOS and the gate-floated native NMOS under different channel lengths.

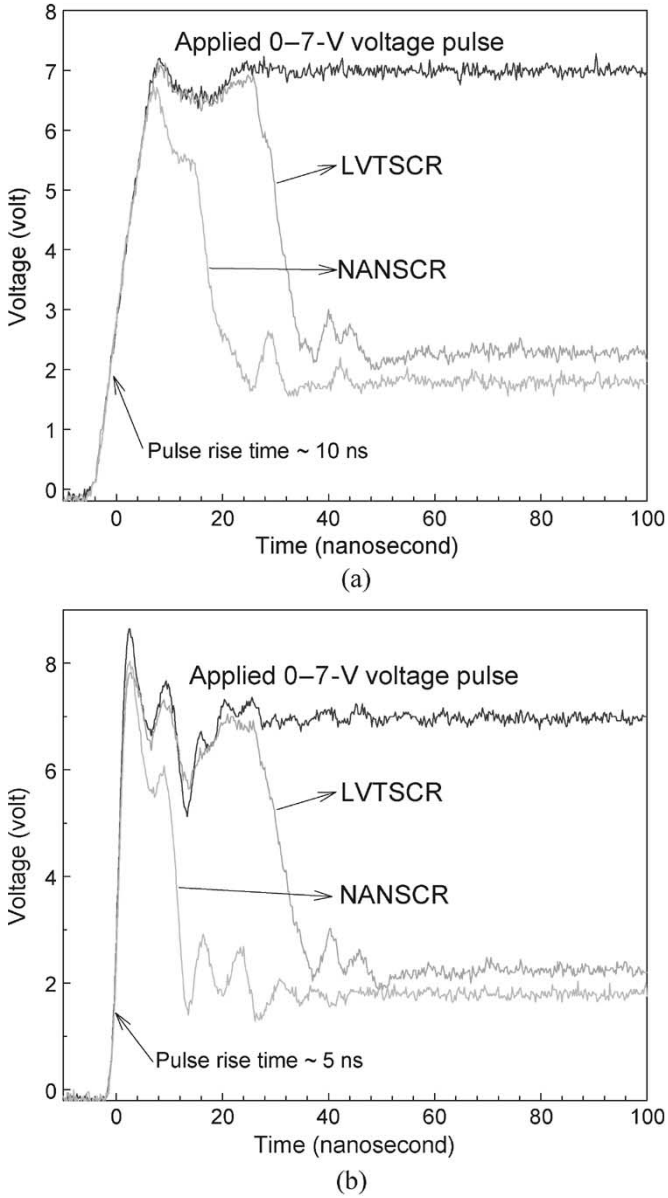

Fig. 10. Comparison of turn-on speeds between the NANSCR and the LVTSCR under the 0–7-V voltage pulse with (a) a 10-ns rise time and (b) a 5-ns rise time.

voltage waveform has no degradation when a 1.2-V voltage signal is applied to the pad, and the gate of the native NMOS in the NANSCR is biased at -0.1 V. Hence, the proposed NANSCR device does not interfere with the functions of I/O circuits or degrade the voltage level of input signals under normal circuit operating conditions. Another experimental setup to measure the turn-on speed or the emission microscope (EMMI) photograph of turn-on behavior among ESD devices under ESD-like transient conditions is shown in Fig. 8, where the Rs (50 Ω) is the output impedance of the pulse generator. By changing the amplitude or rise time of voltage pulse, the turn-on behaviors of ESD devices under ESD events can be observed. The turn-on speeds between the GGNMOS and the gate-floated native NMOS under a channel width of 360 μm, but different channel lengths are compared in Fig. 9. Because the native NMOS is an already-on device under ESD events, the trigger voltage Vt1 ($\sim$ 2 V) of the gate-floated native NMOS is lower than that ($\sim$ 6 V) of the normal GGNMOS under the same device dimension when a 0–6-V voltage pulse is applied. Even if the channel length of the gate-floated native NMOS is drawn as 0.3 μm, its trigger voltage is still lower than that of the normal GGNMOS with a channel length of 0.13 μm. Hence, the turn-on speed of the gate-floated native NMOS is significantly faster than that of the normal GGNMOS. Moreover, whether the channel length of the gate-floated native NMOS is 0.13 or 0.3 μm, both of the gate-floated native NMOS devices have a lower clamping voltage ($\sim$ 2 V) than that ($\sim$ 3.5 V) of the normal GGNMOS with a channel length of 0.13 μm. The trigger voltage and clamping voltage of the gate-floated native NMOS can be reduced with the shrinkage of channel length.

The comparisons of turn-on speeds between the NANSCR and the LVTSCR under 0–7-V voltage pulse with the pulse rise times of 10 and 5 ns are measured and shown in Fig. 10(a) and (b), respectively. The W/L of the native NMOS in the

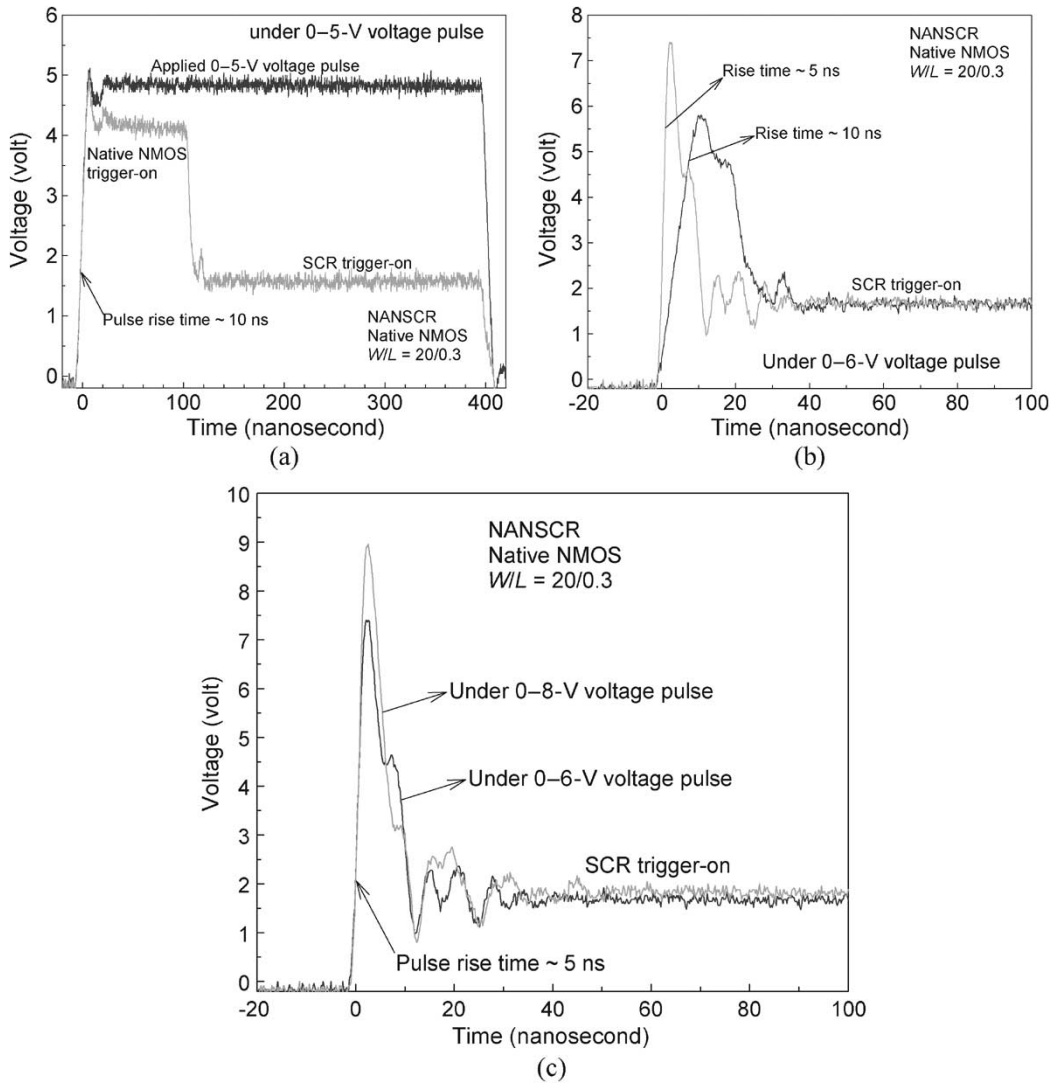

Fig. 11. (a) Turn-on waveform of the NANSCR under the 5-V voltage pulse with a rise time of 10 ns. Comparison of turn-on speeds of the NANSCR (b) under the 6-V voltage pulse with different rise times and (c) under different pulse voltages with the same rise time of 5 ns.

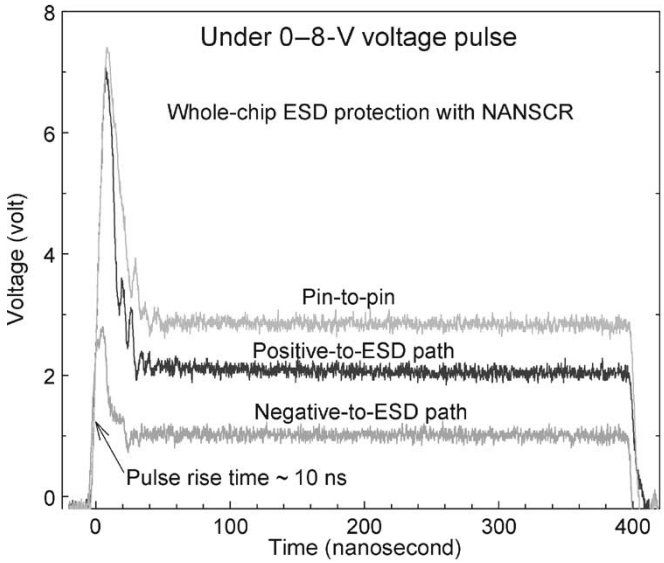

Fig. 12. Clamped voltage waveforms of the whole-chip ESD protection scheme with NANSCR under positive-to-ESD path, negative-to-ESD path, and pin-to-pin ESD-zapping conditions.

NANSCR under this test is 20 μm/0.3 μm. In Fig. 10(a), the turn-on speed ($\sim$ 24 ns) of the NANSCR is faster than that ($\sim$ 38 ns) of the LVTSCR under the 7-V voltage pulse with a 10-ns rise time. Furthermore, the turn-on speed of the NANSCR can be improved with the reduction of pulse rise time but not for the LVTSCR. In Fig. 10(b), the turn-on speed ($\sim$ 12 ns) of the NANSCR is almost three times faster than that ($\sim$ 36 ns) of the LVTSCR when the rise time of the 7-V voltage pulse is reduced from $\sim$ 10 to $\sim$ 5 ns. In addition, the NANSCR can clamp the ESD-like voltage pulse to a lower voltage level than that of the LVTSCR. From the experimental results, the NANSCR is more suitable than the LVTSCR to quickly discharge ESD energy and to efficiently protect the ultrathin gate oxide.

The dependence of turn-on speeds of the NANSCR under different pulse rise times and pulse voltages are shown in Fig. 11(a)–(c). When a 0–5-V voltage pulse is applied to the pad with the NANSCR, the voltage waveform on the pad is clamped to a low voltage level, as shown in Fig. 11(a). The gate-floated native NMOS in the NANSCR will first be turned on to clamp the ESD-like voltage pulse. Because the native

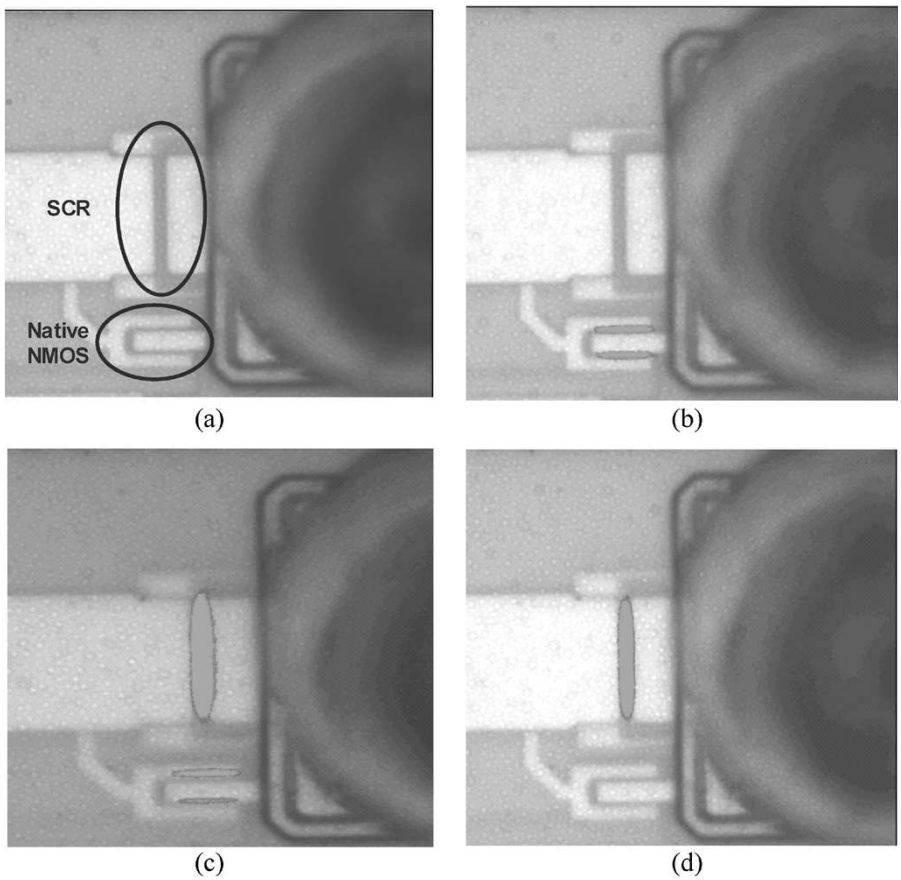

Fig. 13. Measured EMMI photographs on the turn-on behavior of the NANSCR device under the pulsed voltage stresses of (a) 0, (b) 5, (c) 5.8, and (d) 6 V.

NMOS is already on, it will conduct some ESD current to trigger on the SCR device, and then, the SCR clamps the voltage pulse to 1.6 V. Because of the output impedance of the pulse generator and the turn-on resistance of the native NMOS, the clamping voltage ($\sim$ 4 V) of the native NMOS with a channel width of 20 μm in Fig. 11(a) is greater than that of the native NMOS with a channel width of 360 μm in Fig. 9 ($\sim$ 2 V). If the pulse voltage is increased to 6 V and the pulse rise time is kept at $\sim$ 10 ns in Fig. 11(b), the NANSCR can be triggered into a latching state more quickly due to the substrate-triggered technique. Moreover, the turn-on time of the NANSCR is significantly reduced from $\sim$ 30 to only $\sim$ 10 ns when the rise time of the 6-V voltage pulse is reduced from $\sim$ 10 to $\sim$ 5 ns in Fig. 11(b). However, the turn-on speeds of the NANSCR are the same in Fig. 11(c), when the 6- or 8-V voltage pulse with a fixed 5-ns rise time is applied. Fig. 11(c) shows that the dominated factor on the turn-on speed of the proposed NANSCR is the pulse rise time, but not the overshoot transient voltage, if the high-enough voltage pulse is applied. The turn-on time of the NANSCR will trace the rise time of the ESD event (even the CDM stress) to efficiently protect the ultrathin gate oxide if the high-enough voltage pulse has been applied to the NANSCR device.

Fig. 12 verifies the turn-on waveforms of the whole-chip ESD protection scheme with the NANSCR in Fig. 6 under the positive-to-ESD path, negative-to-ESD path, and pin-to-pin ESD-zapping conditions. When a 0–8-V voltage pulse is applied to a pad and the ESD path is relatively grounded, the voltage waveform on the pad is clamped to $\sim$ 2 V by the turned-on NANSCR device. Under the negative-to-ESD path ESD-zapping condition, the amplitude of the clamped voltage waveform on the zapping pad is clamped to $\sim$ 1 V by the forward-biased diode in the NANSCR device between the pad and the ESD path. During pin-to-pin ESD zapping, if the 0–8-V voltage pulse is applied to a pad_1 and a pad_2 is connected to ground, the turn-on waveform on the pad_1 can be quickly clamped to $\sim$ 3 V by the turned-on NANSCR device and the forward-biased diode between the pad_1 and pad_2. The turn-on speed of the NANSCR and the forward-biased diode under the pin-to-pin ESD-zapping condition is almost the same as that of the standalone NANSCR under positive-to-ESD path ESD zapping. Hence, the new whole-chip ESD protection scheme in Fig. 6 can successfully protect the ultrathin gate oxide of the internal circuits against various ESD-zapping tests.

B. EMMI Photographs

The measured EMMI photographs on the turn-on behavior of NANSCR under different voltage pulses are shown in

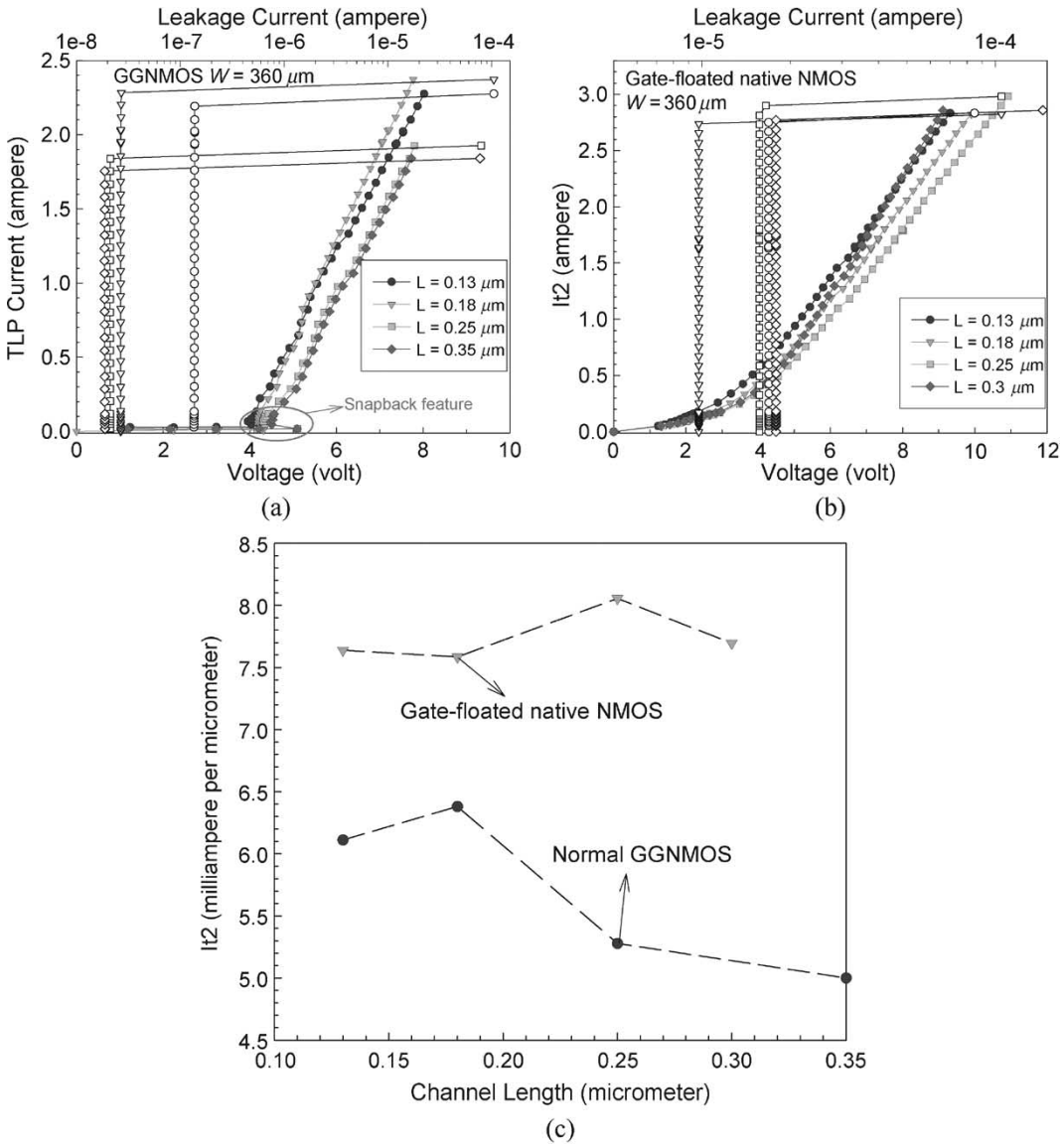

Fig. 14. TLP-measured $I-V$ curves of (a) the normal GGNMOS and (b) the gate-floated native NMOS under a channel width of 360 μm and different channel lengths. (c) Comparison of It2 per micron between the normal GGNMOS and the gate-floated native NMOS under different channel lengths.

Fig. 13(a)–(d). Fig. 13(a) shows the initial EMMI photograph of the NANSCR under the voltage pulse of 0 V, where there is no hot spot in the NANSCR structure. When the pulse voltage is increased to 5 V, the hot spots are shown to be located at the native NMOS in Fig. 13(b), which indicates the turn-on behavior of the native NMOS. When a 5.8-V voltage pulse is applied to the pad, the hot spots are located at both the native NMOS and the SCR device in Fig. 13(c), which means that SCR has been triggered on. Moreover, the intensity of hot spots on the native NMOS will become weaker in Fig. 13(c). If the pulse voltage is further increased to 6 V, all hot spots will be located at the SCR device, and the hot spot in the native NMOS will vanish in Fig. 13(d). The turn-on behaviors of the NANSCR observed by these EMMI photographs are consistent with the results of Fig. 11 observed by the voltage waveforms in the time domain. With the increase of pulse voltage, the ESD current path, as shown by the hot spots, is initially discharged from the native NMOS to trigger SCR into the latching state and then fully discharged through the SCR device, as shown in Fig. 13(b)–(d).

C. Transmission Line Pulsing (TLP) Measurement

By using the TLP measurement [14], [15], the secondary breakdown current (It2) of the ESD protection device can be found. It2 is another index for the HBM ESD robustness, which is indicated by the sudden increase of the leakage current at the voltage bias of 1.2 V in this paper. The relation between secondary breakdown current (It2) and HBM ESD level $(V_{\rm ESD})$ can be approximated as $V_{\rm ESD} \cong {\rm It2} \times 1.5\ {\rm k}\Omega$, where 1.5 k$\Omega$ is the equivalent resistance of the human body. The TLP-measured $I-V$ curves of the normal GGNMOS and the gate-floated native NMOS devices with a silicide-blocking mask under a channel width of 360 μm but different channel lengths are shown in Fig. 14(a) and (b), respectively. Because of the involvement of the avalanche breakdown mechanism [16], [17],

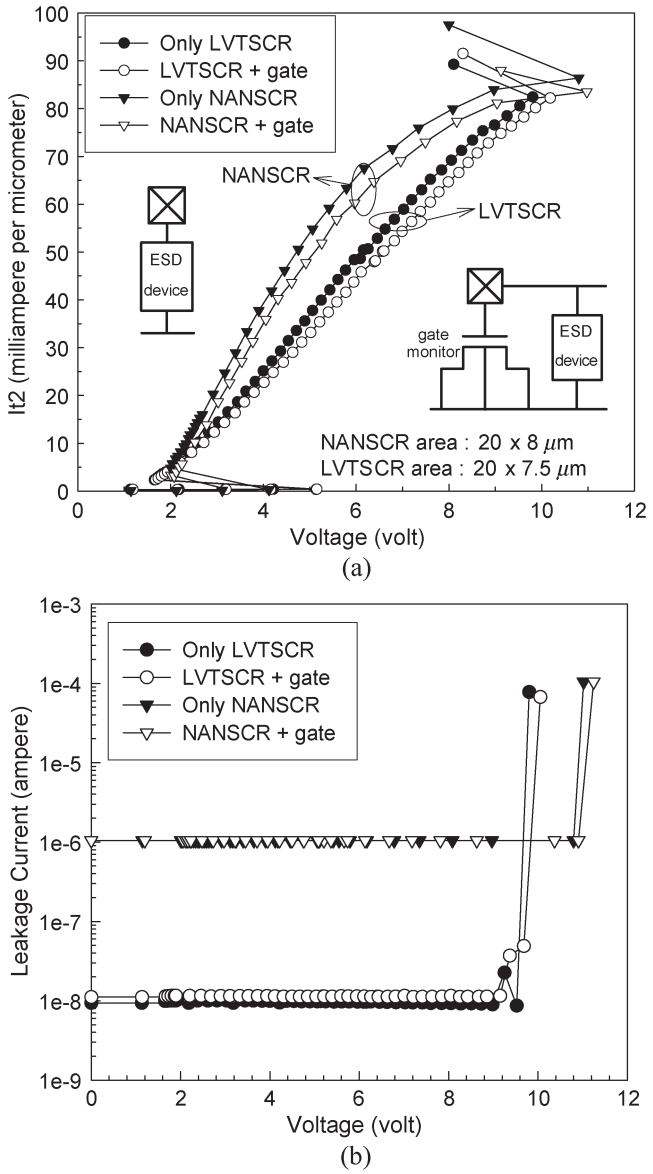

Fig. 15. (a) TLP-measured $I-V$ curves and (b) their corresponding leakage current of NANSCR and LVTSCR under conditions with or without the gate monitor device.

a significant snapback feature will exist in the normal GGNMOS in Fig. 14(a), but it cannot be found in the gate-floated native NMOS in Fig. 14(b). The gate-floated native NMOS is an already-on device under the ESD-zapping condition, so the required substrate current to trigger on the NPN bipolar transistor can be provided by the on current of the native NMOS without involving the avalanche breakdown mechanism. Hence, the trigger voltage of the gate-floated native NMOS in Fig. 14(b) is smaller than that of the normal GGNMOS ($\sim$ 5 V) in Fig. 14(a). The comparison of It2 between the normal GGNMOS and the gate-floated native NMOS under different channel lengths is summarized in Fig. 14(c). The It2 per channel width (in microns) of the gate-floated native NMOS under different channel lengths are all greater than 7.5 $\mathrm{mA}/\mu\mathrm{m}$; however, those of GGNMOS under different channel lengths are all smaller than 6.5 $\mathrm{mA}/\mu\mathrm{m}$. The gate-floated native NMOS can sustain more ESD current than that of the normal GGNMOS under the same layout size.

TABLE I
COMPARISON ON THE ESD ROBUSTNESS BETWEEN NANSCR AND LVTSCR

ESD Device	ESD Stress (volt per square micrometer)			
	HBM ($V/\mu m^2$)	MM ($V/\mu m^2$)	CDM (+) ($V/\mu m^2$)	CDM (-) ($V/\mu m^2$)
NANSCR	16.1	1.3	5	-3.75
LVTSCR	15.9	1.1	2.33	-2

Active area: NANSCR = 20×8 μm^2, LVTSCR = 20×7.5 μm^2.

The It2 of the fully silicided NANSCR and LVTSCR devices under the conditions with or without the gate monitor device and the corresponding measurement setups are shown in Fig. 15(a). The gate monitor device is an NMOS capacitor that verifies the effectiveness of the ESD protective device. The It2 of the NANSCR is almost the same as that of LVTSCR, but the turn-on resistance of the NANSCR ($\sim 3\ \Omega$) is smaller than that of the LVTSCR ($\sim 5.1\ \Omega$) under the TLP-measured conditions, which corresponds to the DC-measured result in Fig. 3(a). Under the breakdown limitation of the ultrathin gate oxide of the input stage, the NANSCR with smaller turn-on resistance can sustain more ESD current than that of the LVTSCR with larger turn-on resistance. In other words, the layout area of the NANSCR can be reduced to sustain the same ESD current as the LVTSCR with the larger layout area. The NANSCR devices have the same It2 per micron of $\sim 80\ \mathrm{mA}/\mu\mathrm{m}$ under the measured conditions with or without the gate monitor device. The corresponding leakage currents of the NANSCR and LVTSCR under the conditions with or without the gate monitor device are shown in Fig. 15(b). The leakage current of the NANSCR with the gate monitor device is almost the same as that of the standalone NANSCR device before the secondary breakdown of the NANSCR device. Therefore, the ultrathin gate oxide of the input stage can be safely protected by the newly proposed NANSCR against ESD stress. Such It2 per micron of the NANSCR with silicide is ten times larger than that of the normal GGNMOS without silicide shown in Fig. 14(c). This has verified that the NANSCR has the highest ESD robustness in the smallest layout area than that of other ESD protection devices.

D. ESD Robustness

ESD stresses have been conventionally divided into three types: the HBM [1], machine-model (MM) [18], and CDM [3] ESD tests. An IC product must sustain such ESD specifications. These three ESD tests are used to verify the ESD levels of the NANSCR and LVTSCR devices. The comparison on the ESD robustness per layout area between the NANSCR and the LVTSCR is summarized in Table I. In this ESD verification, the failure criterion is defined as the measured voltage when the current level of 1 μA is shifted 30% after ESD zapping. The HBM (MM) ESD levels per layout area of the NANSCR and the LVTSCR are almost the

same and equal to ~ 16 (~ 1) V/μm^2. This is because the the NANSCR and the LVTSCR can be triggered on in time. Once the NANSCR and LVTSCR are turned on, the HBM and MM-ESD-stressed energies are discharged through the lateral SCR inherent in the NANSCR and LVTSCR. Therefore, the HBM and MM ESD level of the NANSCR and the LVTSCR are almost the same. However, under the socket-mode CDM ESD testing, the CDM ESD level of the NANSCR is larger than that of the LVTSCR. The die area of the test chip is 1500×1500 μm^2, and its package type is DIP 40. The NANSCR with the gate monitor device can sustain the positive (negative) CDM ESD level per layout area of 5 (-3.75) V/μm^2, but the LVTSCR with the gate monitor device can only sustain that of 2.33 (-2) V/μm^2 in the same 0.13-μm CMOS process. The gate monitor device is also used as an NMOS capacitor in these measurements. The gate of the NMOS capacitor is connected to a pad and protected by the NANSCR or the LVTSCR. The leakage currents of the gate monitor device are the same before and after the ESD-zapping measurements. From the CDM-zapping results, the NANSCR can be indeed triggered on faster to protect the ultrathin gate oxide of the input stage and to sustain the higher CDM ESD robustness, as compared with the LVTSCR.

In addition, the CDM ESD level is an IC's specification related to the ESD protection device, die area, package type, testing environment, and so on [19], [20]. The device-level CDM ESD robustness of the test chip is not always the same as the chip-level CDM ESD robustness of an IC product, but it is a useful and important indication for the ESD protection device to determine which one will be the better solution in the practical field applications.

V. Conclusion

The novel native-negative-channel metal oxide semiconductor (NMOS)-triggered SCR (NANSCR) has been successfully investigated in a 0.13-μm complementary metal oxide semiconductor (CMOS) process with a 1.2-V voltage supply. The NANSCR with a holding voltage of 1.6 V can be designed free of latchup issues for 1.2-V CMOS integrated circuit (IC) applications. As compared with the traditional low-voltage-triggering SCR (LVTSCR), the NANSCR has the lower trigger voltage, smaller turn-on resistance (~ 3 Ω), lower clamping voltage, faster turn-on speed, and higher charged-device-model (CDM) electrostatic discharge (ESD) level to protect the ultrathin gate oxide against ESD stresses. From the experimental results, the turn-on speed of NANSCR ($\sim$ 20 ns) has been improved to two times faster than that of a traditional LVTSCR ($\sim$ 40 ns) under a 7-V voltage pulse with a 10-ns rise time. Moreover, the turn-on time of the NANSCR is further reduced to only $\sim$ 10 ns when the pulse rise time is reduced from 10 to 5 ns under a 6-V voltage pulse. The NANSCR can sustain the positive (negative) CDM ESD level per layout area of 5 (-3.75) V/μm^2, but the LVTSCR can only sustain that of 2.33 (-2) V/μm^2 in the same 0.13-μm CMOS process. For ultra-large-scale CMOS ICs with multiple power pins, the proposed whole-chip ESD protection scheme with the NANSCR and the ESD path is an overall solution to quickly discharge all kinds of ESD stresses and to provide efficient protection for the internal circuits.

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