Investigation of Electrical Characteristics on Surrounding-Gate and Omega-Shaped-Gate Nanowire FinFETs

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***Abstract*—In this paper, electrical characteristics of small nanowire fin field-effect transistor (FinFET) are investigated by using a three-dimensional quantum correction simulation. Taking several important electrical characteristics as evaluation criteria, two different nanowire FinFETs, the surrounding-gate and omega-shaped-gate devices, are examined and compared with respect to different ratios of the gate coverage. By calculating the ratio of the on/off current, the turn-on resistance, subthreshold swing, drain-induced channel barrier height lowing, and gate capacitance, it is found that the difference of the electrical characteristics between the surrounding-gate (i.e., the omega-shaped-gate device with 100% coverage) and the omega-shaped-gate nanowire FinFET with 70% coverage is insignificant. The examination presented here is useful in the fabrication of small omega-shaped-gate nanowire FinFETs. It clarifies the main difference between the surrounding-gate and omega-shaped-gate nanowire FinFETs and exhibits a valuable result that the omega-shaped-gate device with 70% coverage plays an optimal candidate of the nanodevice structure when we consider both the device performance and manufacturability.**

***Index Terms*—Coverage ratio, device structure, fabrication, fin field-effect transistor (FinFET), gate capacitance, nanodevice, nanowire, omega-shaped-gate, on/off ratio, process technique, quantum correction model, semiconductor devices, subthreshold swing (SS), surrounding gate, three-dimensional (3-D) simulation, turn-on resistance.**

I. Introduction

SILICON-ON-INSULATOR (SOI) devices have recently been of great interest and relatively present better scaling-down properties than that of conventional bulk metal–oxide–semiconductor field-effect transistors (MOSFETs) [1]–[4]. Double-gate SOI devices have been proposed and found more attractive electrical characteristics than that of single-gate SOI devices [5]–[21]. They inherently have good suppression of short-channel effects (SCEs), high transconductance, and ideal subthreshold swing (SS). In order to further reduce the SCEs, promising device structures, such as the fin field-effect transistor (FinFET), multiple-gate FinFETs, and surrounding-gate nanowire FinFETs have been proposed, fabricated, and demonstrated their fascinating device characteristics [5]–[21]. However, these structures cannot be directly fabricated with advanced fabrication processes and have inherently encountered several difficulties [7], [8], [11]. Considering issues of the mass production, omega-shaped-gate nanowire FinFET structures [5], [6], [9], [20] have been proposed to make a compromise between the device performance and manufacturability. Device simulation with different physical aspects and computational models has been widely proposed and used in studying diverse semiconductor nanodevices [14], [18], [19], [21]–[58]. However, theoretical calculation and comparison of the surrounding-gate and omega-shaped-gate nanowire FinFETs using a unified simulation model have never been well drawn. In addition, a quantitative evaluation of the difference on these devices' performance is still unclear. We believe that any theoretical examinations on the surrounding-gate and omega-shaped-gate nanowire FinFETs will provide interesting information for designing any novel structures and benefits the fabrication of integrated circuits with using these advanced nanodevices.

In this paper, electrical characteristics of ultrasmall nanowire FinFETs are numerically explored using a developed quantum correction simulation. Based on a multidimensional device simulation [41]–[54], the ratio of the on/off current, turn-on resistance ($R_{\rm out}$), SS, drain induced barrier lowering (DIBL), and gate capacitance C_G [59], [60] are calculated and compared for a 5-nm nanowire FinFET with the surrounding-gate and omega-shaped-gate structures, respectively. Device with the surrounding-gate structure means it has 100% ratio of the gate coverage. The coverage changing from 70% to 80% for the device with the omega-shaped-gate structure is comprehensively explored in this study. The diameter of the 5-nm nanowire field-effect transistor (FET) is set to be 10 nm and the thickness of the gate oxide is with 1 nm. According to our calculation, it is found that the characteristic difference between the surrounding-gate and omega-shaped-gate FinFETs with 70% coverage is insignificant. However, the first structure possesses slightly better DIBL effect than that the latter one with different coverage ratios. Taking the thickness of the silicon film into consideration, the omega-shaped-gate device with 70% gate coverage provides an attractive alternative in considering both the device performance and manufacturability. Overall, the omega-shaped-gate FinFET with a coverage that

Manuscript received August 15, 2004; revised January 10, 2005. This work was supported in part by the National Science Council of Taiwan under Contract NSC-93-2215-E-429-008 and Contract NSC-94-2752-E-009-003-PAE, by the Ministry of Economic Affairs, Taiwan, R.O.C., under Contract 93-EC-17-A-07-S1-0011, and by the Taiwan Semiconductor Manufacturing Company under a 2004–2005 grant. An earlier version of this paper was presented at the 2004 IEEE Conference on Nanotechnology.

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Digital Object Identifier 10.1109/TNANO.2005.851410

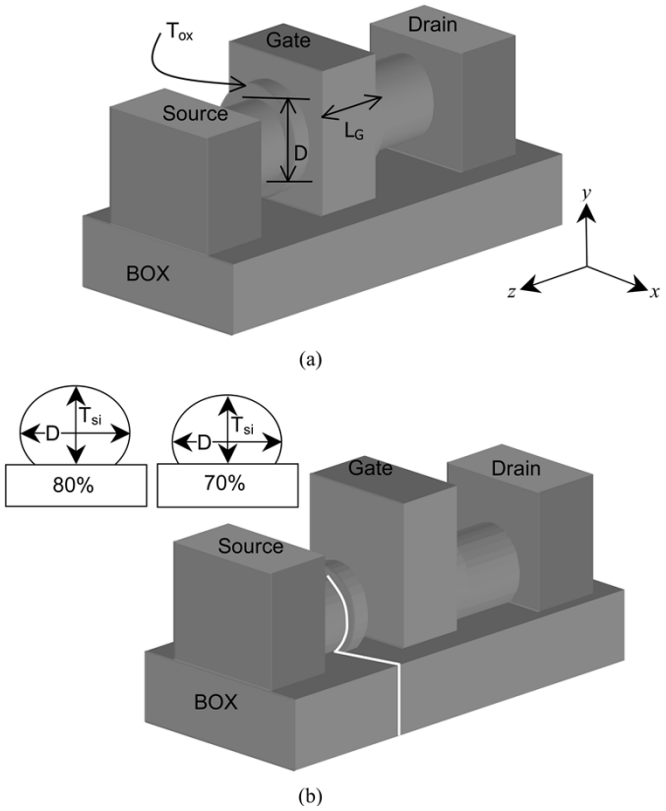

Fig. 1. Illustrations of the cylindrical nanowire FinFET with: (a) the surrounding-gate structure and (b) the omega-shaped-gate structure. L_G is the channel length, $T_{\rm ox}$ is the thickness of oxide, and D is the diameter of the nanowire FinFET. The two insets, cutting along the white line in (b), show the cross sections of the structure with 70% and 80%, respectively, where $T_{\rm si}$ is the thickness of the channel film.

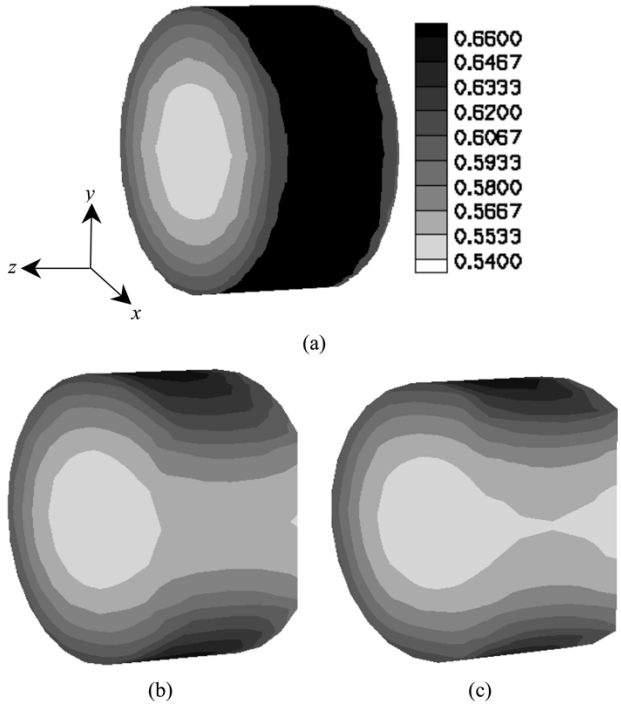

Fig. 2. Electrostatic potential on the channel region of the 5-nm nanowire FinFET with: (a) the surrounding-gate structure (b) the 80% omega-shaped-gate structure, and (c) the 70% omega-shaped-gate structure, respectively. The bias condition is $V_G = 0.8$ V and $V_D = 0.05$ V.

is larger than 70% may demonstrate a similar performance to the surrounding-gate FinFET. Our examination presented here clarifies the geometric effects on the characteristic difference between the surrounding-gate and omega-shaped-gate FinFETs. It is useful to develop new fabrication techniques for ultrasmall omega-shaped-gate nanowire FinFETs.

This paper is organized as follow. In Section II, we state the investigated device structure and simulation. In Section III, we calculate several important electrical characteristics of the studied device structures. Comparison and discussion between the different device structures with various coverage ratios are included in this section. Section IV draws conclusions and suggests future works.

II. Device Structure and Computational Model

Computationally experimental structures are shown in Fig. 1. These two devices are the surrounding-gate and omega-shaped-gate nanowire FinFETs, respectively. An omega-shaped-gate nanowire FinFET with 100% gate coverage is automatically equivalent to the surrounding-gate nanowire FinFET. To simplify the investigated problem and clarify the main effect of the geometric variation on the electrical characteristics for the small nanowire FinFET, the simulated FinFETs are with the same diameter $D = 10$ nm, the gate length $L_G = 5$ nm, the channel is with an uniform doping 10^{18}cm^{-3}, the source/drain doping is with 5×10^{19}cm^{-3} uniformly, the oxide thickness $T_{\rm ox} = 1$ nm, and the midgap material, such as TiN, is chosen as the gate material. Today, the channel length of semiconductor devices is in the nanoscale regime; it becomes necessary to include quantum mechanical effects when modeling any FET's terminal property [14], [18], [19], [21]–[55], [58]. There have been several approaches to the modeling of quantum mechanical effects, such as quantum mechanical methodologies and quantum corrections to the classical transport models [18], [19], [21]–[55], [58]. A full quantum mechanical model physically provides one of the most accurate ways to simulate nanodevices, but it is costly in the technology computer-aided design (TCAD) simulation of multidimensional deep submicrometer and nanoscale devices [22].

To focus on exploring the fluctuation problem of the electrical characteristics for optimal nanodevice structures, phenomenological quantum correction model, a density-gradient equation [41]–[54] together with the classical three-dimensional (3-D) drift–diffusion model [56], [57] is adopted and solved numerically in this study. A carefully calibrated density-gradient model [43]–[47] has attracted more and more attention and successfully demonstrates its validity for efficient modeling of the quantum mechanical effects in a TCAD simulator using first-order quantum corrections [41]–[54]. This simulation quantitatively predicts the main tendency of electrical and physical properties for the examined device structures. Full quantum mechanical methodologies definitely will input more accurate estimation on the characteristics, but it is believed that our simulation will not be significantly altered. The density-gradient modeling approach is computationally effective for incorporating the quantum mechanical effect in a multidimensional nanodevice TCAD simulation [22], [49], [51], [52].

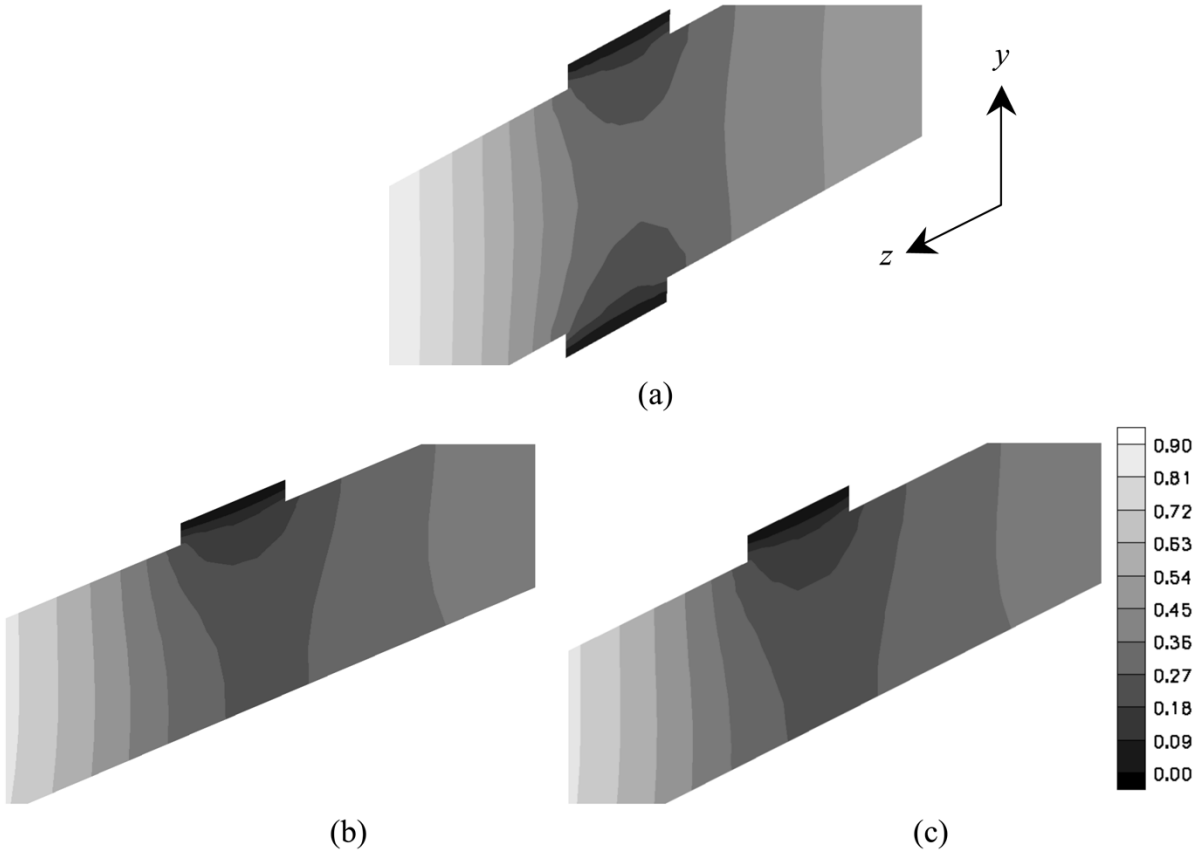

Fig. 3. Electrostatic potential on channel regions from the source to drain for the 5-nm nanowire FinFET with: (a) the surrounding-gate structure, (b) the 80% omega-shaped-gate structure, and (c) the 70% omega-shaped-gate structure, respectively. The bias condition is $V_G = 0.0$ V and $V_D = 0.8$ V.

To calculate the numerical solution of the multidimensional density-gradient model [41]–[52] for the studied device structures, shown in Fig. 1, a robust two-dimensional (2-D)/3-D device simulation program is developed. Developing this computational prototype is mainly based on our recent work on nanodevice simulations [53]–[57]. Firstly, we decouple the coupled partial differential equations (PDEs); each decoupled PDE is approximated with the finite volume method over nonuniform mesh [51]–[57]. The corresponding system of the nonlinear algebraic equations is then solved with the mixed monotone iteration and Newton's iteration methods [57]. Iterations will be terminated and postprocesses will be performed when the specified stopping criteria for inner and outer iteration loops are satisfied, respectively.

III. Results and Discussion

Figs. 2(a)–(c) and 3(a)–(c) are the computed electrostatic potential for the simulated nanowire FinFET with the surrounding gate, omega-shaped gate with a coverage ratio of 80%, and (c) omega-shaped gate with a coverage ratio of 70%, respectively. The difference of the on state is observed in the channel region when $V_G = 0.8$ V and $V_D = 0.05$ V is shown in Fig. 2(a)–(c). Moreover, for $V_G = 0.0$ V and $V_D = 0.8$ V, the contours of the off-state potential are shown in Fig. 3(a)–(c). It is found from those figures that gate electrodes of the omega-shaped-gate devices have a good controllability at the undercut region. Owing to the good controlling of the undercut regime, the on-current degradation of the omega-shaped-gate device does not follow

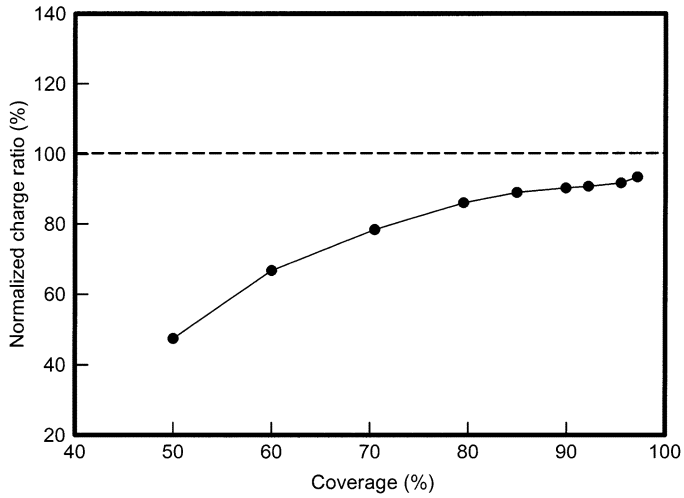

Fig. 4. Normalized ratio of the inversion charge versus the gate coverage. The coverage ratio varies from 50% to 97%. The normalization is with respect to the charge of the surrounding-gate nanowire FinFET under $V_D = 0.05$ V and $V_G = 0.8$ V.

the reduction of the gate coverage ratio. That is a reduction on the coverage ratio of the omega-shaped-gate nanowire FinFETs, which can only slightly influence the electrical characteristics of devices. As shown in Fig. 4, the plot of the charge ratio versus the coverage of the gate confirms the calculation results, as shown in Figs. 2 and 3. The devices are with $V_D = 0.0$ V and $V_G = 0.8$ V, where the calculated total charge is normalized with respect to the total charge of the surrounding-gate nanowire

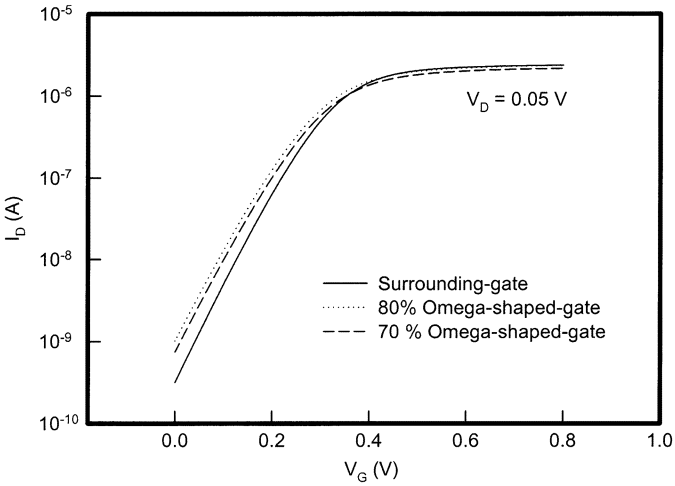

Fig. 5. $I_D - V_G$ curves of the simulated 5-nm nanowire FinFET with the surrounding-gate and the omega-shaped-gate structures. The solid line is the result of the surrounding-gate device and the dotted and dashed lines are the results of the omega-shaped-gate device with 80% and 70% coverage ratios, respectively.

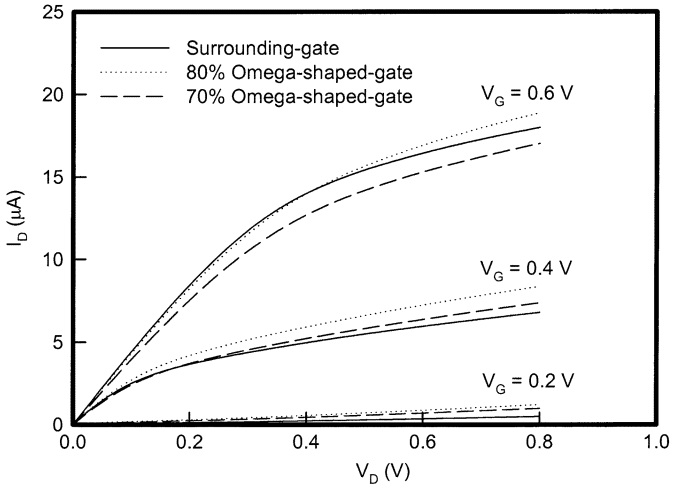

Fig. 6. $I_D - V_D$ curves of the simulated 5-nm nanowire FinFET with the surrounding-gate and the omega-shaped-gate structures.

FinFET. It is found when the gate coverage varies from 50% to 70% that the slope of the normalized charge ratio is approximately 2 times larger than that of the gate coverage varying from 70% to 97%.

The potential distributions explain the $I_D - V_G$ and $I_D - V_D$ characteristics for both the surrounding-gate and the omega-shaped-gate nanowire FinFETs, shown in Figs. 5 and 6, respectively. The $I_D - V_G$ characteristics for the structures with different coverage ratios are shown in Fig. 5. Although the surrounding-gate nanowire FinFET has better characteristics over the off-state and the subthreshold condition, the on-state current for all the simulated structures are almost similar with respect to different coverage ratios. Moreover, the difference on the $I_D - V_G$ and $I_D - V_D$ characteristics between the surrounding-gate and omega-shaped-gate devices are quite small, e.g., the largest variation of the $I_D - V_D$ characteristics at $V_G = 0.6$ V and $V_D = 0.8$ is approximately 10%, as shown in Fig. 6. The fluctuation of the drain current is acceptable when we take the difficulty of the fabrication into consideration. The ratio of the on/off current calculated from the transfer curves is summarized in Table I. The calculation is done by dividing the on-current level (i.e., I_D at $V_G = 0.8$ V and $V_D = 0.05$ V) to the off current level (i.e., I_D at $V_G = 0.0$ V and $V_D = 0.8$ V). The ratio of the on/off current is a major concerned factor in modern gigascale integrated-circuit design. The on current is strongly related to the switching speed and the off current is directly corresponding to the power consumption. Therefore, a higher ratio of the on/off current is preferred for improving the circuitry performance. According to the summarized data shown in Table I, it is found that the surrounding-gate nanowire FinFET has a slightly higher ratio of the on/off current than that of the omega-shaped-gate structures. Similarly, this can be explained due to the channel controllability for these structures, as shown in Figs. 2 and 3.

Based on numerical simulation, the SS property is also extracted and shown in Table I. The SS is defined as the gate voltage that has to be increased for enlarging a decade of subthreshold current [56], [57]. This property is highly correlated with the switching speed and the noise margin of the designed circuit. It has been found that the SS of the surrounding-gate device is insignificantly lower than that of the others. That is, without considering the fabrication stability, the surrounding-gate structure merely contributes a slight improvement on designing the digital circuit. The SS of the bulk devices traditionally is around 100 mV/decade. However, the SS of all explored devices shown here is much less than that of the bulk devices. The significant improvement will be mainly contributed to the fully depleted effects. We note that the SS is not simply proportional to the coverage ratio of the omega-shaped-gate structure. It is also affected by the thickness of the channel film. For device with a smaller coverage, it implies a thinner channel film thickness. For example, for an omega-shaped-gate structure with 80% coverage, its channel film thickness is equal to 9 nm. For the 70% coverage, it is 8 nm. Therefore, according to the argument of the channel film thickness, the omega-shaped-gate structure with 70% coverage has a smaller SS than that of the structure with 80% coverage. Furthermore, owing to the fully depleted effect, the threshold voltage of the nanowire FinFET devices is hardly to be adjusted by changing the channel doping concentration. Altering the work function will be one of the efficient ways for the modification of the threshold voltage. The midgap material will be the candidate for gate formation.

Output characteristics of the simulated structures with different coverage ratios could be explored from the results shown in Figs. 6 and 7, respectively. It can be found that the difference between the simulated structures with different coverage rations is very limited. Moreover, in comparing both the on current and output resistance, it will be concluded that the higher gate coverage ratio will result in better device characteristics. To make it more clear, the omega-shaped-gate device with a coverage ratio of 80% has a higher on-state current, but a lower output resistance than that of the 70% one. The on-state current discussed above is directly related to the operation speed of the digital circuit. On the other hand, the output resistance is an important element in designing the analog circuit, i.e., the higher the output resistance, the better the analog performance. Accordingly, we can summarize that the omega-shaped-gate devices with a different coverage ratio will be a promising approach to a different application category and should be subject

TABLE I
COMPARISON OF THE CALCULATED ELECTRICAL CHARACTERISTICS FOR THE SIMULATED 5-nm NANOWIRE FinFET WITH TWO DIFFERENT GATE STRUCTURES. DIBL IS CALCULATED AS THE SHIFT OF V_t, WHERE V_t IS THE THRESHOLD VOLTAGE. C_G IS CALCULATED WHEN $V_G = 0.8$ V

	Device with the surrounding-gate structure	Device with the omega-shaped-gate structure	
Gate coverage ratio	100%	80%	70%
SS	87 mV	97 mV	93 mV
DIBL	0.09 V	0.115 V	0.10 V
Log (Ratio of the on/off current)	2.96	2.21	2.32
C_G	$4.28\text{x}10^{-18}$ F	$3.8\text{x}10^{-18}$ F	$3.68\text{x}10^{-18}$ F

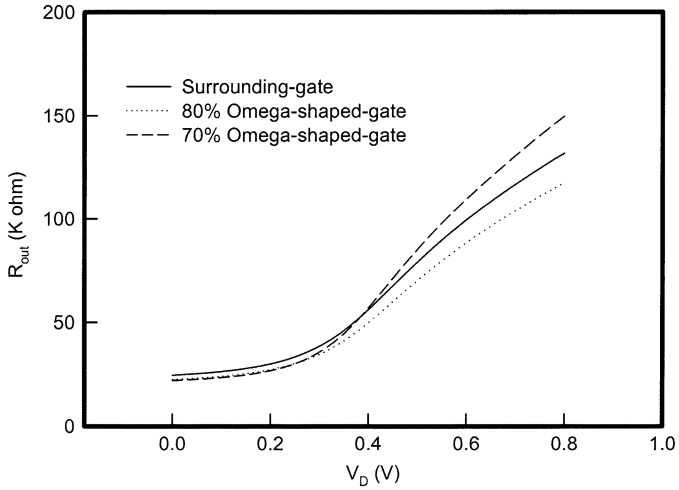

Fig. 7. Calculated characteristics of R_{out} for the simulated 5-nm nanowire FinFET with the surrounding-gate and the omega-shaped-gate structures where $V_G = 0.6$ V.

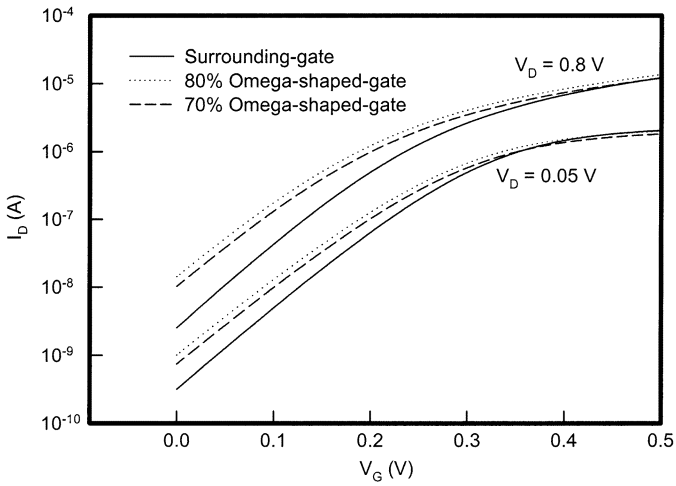

Fig. 8. DIBL effects for the simulated 5-nm nanowire FinFET with the surrounding-gate and omega-shaped-gate structures.

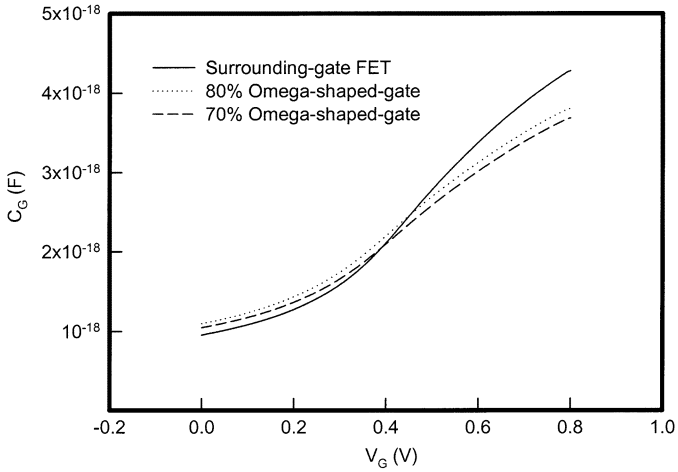

Fig. 9. Plot of C_G versus V_G for the simulated 5-nm nanowire FinFET with the surrounding-gate and the omega-shaped-gate structures where the $V_D = 0.05$ V.

to further optimization for the nanodevice fabrication. The effect of the drain induced channel barrier height lowering in the simulated structures with different coverage ratios are shown in Fig. 8 and also summarized in Table I. It is known that the DIBL effect will make the devices harder to be turned off at high drain biased situations. Additionally, this effect will also suffer the development of the corresponding equivalent-circuit compact model for integrated-circuit simulation and degrades the performance of analog integrated circuits. We are found that the surrounding-gate device has a better ability in suppressing the DIBL effect. Nevertheless, the improvement is still unpronounced in comparison with the difficulty coming from the manufacturability point-of-view.

The plot of the $C_G - V_G$ curve for the simulated structures is reported in Fig. 9 and the corresponding extracted output is listed in Table I. The simulation of $C_G - V_G$ confirms the preliminary consistence of the electrical and physical properties of the surrounding-gate and omega-shaped-gate nanowire FinFETs. Based on a rough estimation form the CV calculation shown in Fig. 9 and Table I, the capacitance reduction ratio is

only a half of the decrement on the gate coverage ratio. Those results also can be verified from the results shown in Fig. 4. It confirms that our previous simulations on the difference of electrical characteristics between the surrounding-gate and omega-shaped-gate nanowire FinFETs are very subtle. It could be summarized that the degradation of the electrical characteristics on the omega-shaped-gate nanowire FinFETs is far less than the reduction of the coverage ratio. Consequently, in order to obtain both device performance and manufacturability of the nanowire devices, the omega-shaped-gate devices with 70% coverage will be an attractive candidate.

IV. Conclusion

In this paper, we have preliminarily explored the difference of the electrical characteristics between the surrounding-gate and omega-shaped-gate (with different coverage ratios) nanowire FinFETs. Different simulation has been performed on a 5-nm nanowire FinFET with the developed simulation program, which is mainly based on a calibrated density-gradient equation together with the 3-D drift–diffusion model. According to our theoretical investigation, it has been found that the gate coverage ratio only contributes a small reduction on the output device performance. A higher gate coverage ratio does not necessarily promise better output characteristics. We believe that the work presented here is useful in the fabrication of the omega-shaped-gate nanowire FinFETs [7], [8], [61]. It exhibits a valuable result, which is that the omega-shaped-gate FinFET with 70% coverage is an optimal candidate of the nanodevice structure when we consider both device performance and manufacturability.

However, the physical model considered in the developed device simulation prototype can be improved and extended by using full quantum mechanical techniques. It is believed that full quantum mechanical modeling and simulation [58] will quantitatively provide more accurate estimation. We are currently developing a multidimensional full quantum mechanical simulation and also calibrating the developed 3-D quantum correction simulation with the fabricated 5- and 10-nm nanowire CMOS devices. Optimization of the geometric ratio of the strained omega-shaped-gate nanowire FinFETs with respect to the device's diameter and channel length is under investigation.

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Hung-Mu Chou, photograph and biography not available at time of publication.

Jam-Wem Lee, photograph and biography not available at time of publication.