A Comparative Study of Electrical Characteristic on Sub-10-nm Double-Gate MOSFETs

Yiming Li and Hong-Mu Chou

Abstract—We explore the structure effect on electrical characteristics of sub-10-nm double-gate metal–oxide–semiconductor field-effect transistors (DG MOSFETs). To quantitatively assess the nanoscale DG MOSFETs' characteristics, the on/off current ratio, subthreshold swing, threshold voltage ($V_{\rm th}$), and drain-induced barrier-height lowering are numerically calculated for the device with different channel length (L) and the thickness of silicon film ($T_{\rm si}$). Based on our two-dimensional density gradient simulation, it is found that, to maintain optimal device characteristics and suppress short channel effects (SCEs) for nanoscale DG MOSFETs, $T_{\rm si}$ should be simultaneously scaled down with respect to L. From a practical fabrication point-of-view, a DG MOSFET with ultrathin $T_{\rm si}$ will suppress the SCE, but suffers the fabrication process and on-state current issues. Simulation results suggest that $L/T_{\rm si} \geq 1$ may provide a good alternative in eliminating SCEs of double-gate-based nanodevices.

Index Terms—Adaptive computation, channel length, density gradient drift-diffusion model, double-gate MOSFET, drain-induced barrier height lowering, numerical simulation, on/off current ratio, quantum correction transport model, sub 10 nm, subthreshold swing, system-on-a-chip (SOC), thickness of silicon film, threshold voltage, very large scale integration (VLSI).

Fig. 1.   Schematic diagram of the simulated DG MOSFET.

DOUBLE-GATE silicon-on-insulator (DG SOI) devices have recently been of great interest, particularly for the investigation of sub-10-nm field-effect transistors [1]–[5]. These structures suppress short channel effects (SCEs), have high transconductance, and produce ideal subthreshold swing (SS). Compared with conventional single-gate metal–oxide–semiconductor field-effect transistor (MOSFETs) [1]–[3], they have superior channel-control properties so drain-induced barrier-height lowering (DIBL), $V_{\rm th}$ rolloff, and off-state leakage can be greatly suppressed [1]–[11]. The on/off current ratio is directly related to the high-frequency performance and power consumption. Circuits with a higher on/off current ratio have a better high-frequency performance versus power consumption tradeoff. SS reflects the switch speed of the devices; a lower SS sustains a digital circuit with a high switching speed and high noise margin. $V_{\rm th}$ rolloff and DIBL effects will direct
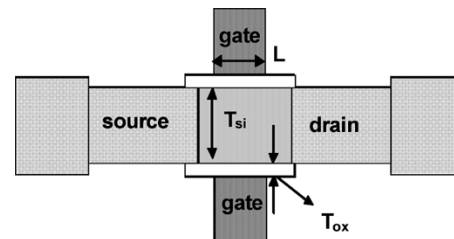
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influence the uniformity of designed circuit. A large $V_{\rm th}$ results in a significant variation of the designed circuit, which downgrades the circuit performance. Under specified conditions, the structure of nanoscale DG SOI devices can be subject to further optimization for sustaining more physical and electrical benefit.

By considering: 1) the on/off current ratio; 2) the SS; 3) the threshold voltage; and 4) and the DIBL, we theoretically investigate the electrical characteristics of sub-10-nm double-gate MOSFETs (DG MOSFETs) with respect to different L and $T_{\rm si}$. To have optimal device structure and corresponding electrical characteristic, the aforementioned four characteristics are calculated and quantitatively compared utilizing two-dimensional (2-D) density gradient simulation [9]–[12]. There have been several approaches to the modeling of quantum mechanical (QM) effects in nanoscale devices such as full QM and quantum correction models [6]–[13]. To focus on the problem of structure optimization, a set of 2-D density gradient drift–diffusion equations is adopted in the simulation of nanoscale DG MOSFETs [9], [11], [13]. To validate the density gradient model, we have referred to the simulation reported in [6], and [9]–[12] to calibrate the model in both the confinement and source/drain tunneling by using different effective masses along the normal and parallel directions with respect to the device channel [9]–[12]. This approach is computationally efficient for incorporating quantum corrections in 2-D/three-dimensional (3-D) technology computer-aided design (TCAD) simulation of the device. To solve the 2-D density gradient drift–diffusion model, we use the adaptive computational technique [13].

Shown in Fig. 1, $T_{\rm ox}$ is equal to 1 nm for the symmetric DG MOSFET. The source (and drain) overlapping the gate is 0.5 nm and the gate edge to the source/drain contact edge is 150 nm. This setting is referring to as the realistic device structure for having a better result in calibration. The source/drain doping used in our simulation is an n$^+$ Gaussian profile with is peak value of 5×10^{19} cm^{-3}. The channel is with a 10^{18} cm^{-3} constant doping. The channel length L is defined in a physical
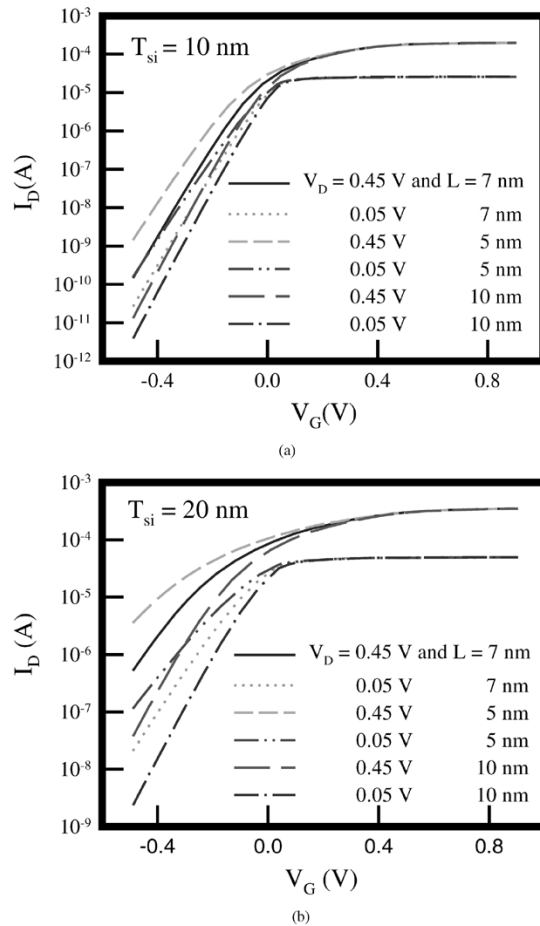
(a)

(b)

Fig. 2. Comparison of the I_D–V_G characteristics for the DG MOSFETs with L where: (a) $T_{si} = 10$ nm (b) and $T_{si} = 20$ nm, respectively.

Fig. 3. I_D–V_D characteristics simulated from the DG MOSFETs with different L where $T_{si} = 10$ nm is fixed.

TABLE I
EFFECT OF CHANNEL DOPING CONCENTRATION ON THE THRESHOLD VOLTAGE FOR THE SIMULATED DG MOSFET WITH $T_{si} = L = 10$ nm

Doping level (cm^{-3})		10^{15}	10^{16}	10^{17}	10^{18}
V_D	0.05 V	-0.00561 V	-0.05675 V	-0.04052 V	-0.06352 V
	0.45 V	-0.03809 V	-0.08739 V	-0.09059 V	-0.09083 V

meaning; it means that it is taken as the real length of the gate pattern. The gate material is with an n+ polysilicon gate, where the doping level is 10^{20} cm^{-3} and its thickness is 30 nm. Considering the fabrication accessibility and process fluctuation [2], [3], a thinnest thickness of silicon film is taken as 10 nm in this study.

Fig. 2(a) shows that the gate length reduction will cause a worse DIBL characteristic; moreover, the SS is simultaneously becoming large for the short gate-length devices. These characteristics, from the fabrication engineering point-of-view, will be important issues for the scaling down of devices. Without considering the poor SCEs for short channel devices, it could be concluded that the length of gate does not significantly modulate the on-state current of double-gate devices. This should be caused from the fact that the parasitic resistance is relatively high; therefore, it limits the on-state current of these thin device's film. The I_D–V_G transfer curves of the 10-nm thicken silicon film devices slightly shows DIBL effects, but the DG MOSFETs with $T_{si} = 20$ nm present significant DIBL effects, as shown in Fig. 2(b). Moreover, the off-state current level of the devices with the thicker silicon film is much higher than those with the thinner one. Those drawbacks are mainly caused from the fact that the device with a thicker silicon film weakens the controllability of gate electrodes. Owing to such poor gate controllability, devices with a thicker silicon film have a lower
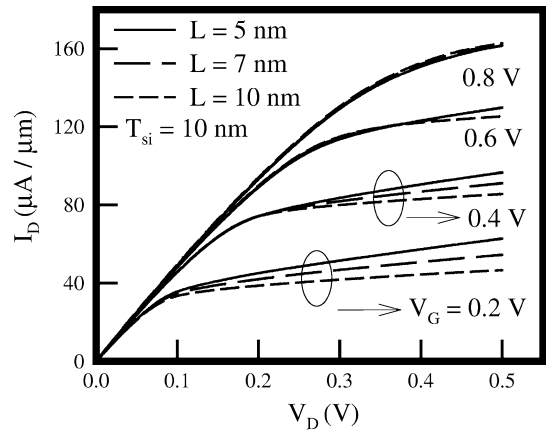
channel barrier height, encounter a higher leakage current level, and get a worse result for DIBL effects.

Besides, the on-state current is another important factor for evaluating the operation of novel devices; for example, a large on-state current will result in a high operation frequency. Fig. 3 shows the I_D–V_D characteristics of the simulated DG MOSFETs with $T_{si} = 10$ nm. The short channel devices do slightly enhance the on-state current. However, owing to a very poor performance in the threshold voltage and the off-state current, the benefit of the on-state current relatively becomes minor in the optimization of DG MOSFETs. The higher on-state current level is caused from the DIBL effect that the drain voltage modulates the current for the shorter gate-length devices. Nevertheless, the current modulation will cause a drawback for the analog circuit applications, such as a small output resistance will greatly degrade the gain of the device.

Due to the full depletion of the channel region, the threshold voltage of the thin body devices is relatively low and hardly needs to be adjusted by increasing the channel doping. It is clearly found from Table I that a four-orders increase of channel doping could only make approximately a 0.1-V shift of V_{th}. Consequently, it is becoming a more important course in fine tuning the work function of the metal semiconductor. For the simulated DG MOSFET with $T_{si} = L = 10$ nm, Table I exhibits the effects of channel-doping concentration on the threshold voltage. Channel doping is often considered a parameter for the threshold voltage adjustment in the bulk devices, but it does not work well for double-gate devices. Therefore, directly tuning the work function of the gate metal provides an alternative to obtain a required threshold voltage. According to our studies, a midgap metal may provide suitable material for the design
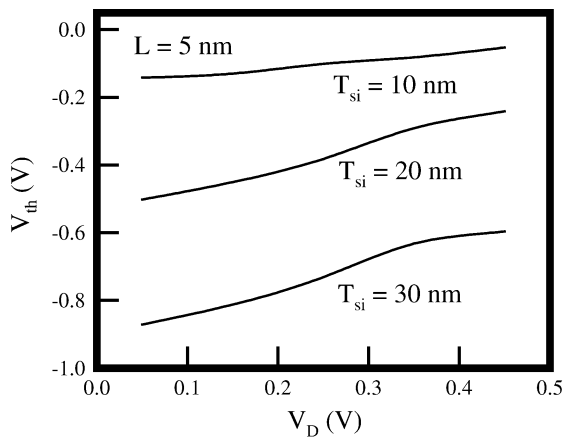
Fig. 4. V_{th} versus the drain bias with respect to different T_{si} where $L = 5$ nm and T_{si} varies from 10 to 30 nm.

and fabrication of double-gate nanodevices. For a more accurate estimation, effects of the random doping fluctuation should also be included [10], [12]. The V_{th} rolloff characteristic is an important issue for modern very large scale integration (VLSI) circuit design including system-on-a-chip (SOC) application; a significant V_{th} rolloff will greatly increase the difficulty in both the VLSI circuit design and SOC manufacturing. The thickness of silicon film correlated threshold voltage rolloff properties are calculated and shown in Fig. 4. It is found that the devices with the thinner silicon films will sustain a good rolloff behavior. Additionally, a thinner silicon film will result in a larger threshold voltage. These good characteristics improve the scalability of nanoscale DG MOSFETs.

In conclusion, by solving a unified 2-D density gradient model, we have simulated sub-10-nm DG MOSFETs and found that DG MOSFETs with thinner silicon films greatly suppress the SCE, but the on-state current issue suffers. A compromise between silicon film thickness and gate channel length should be maintained at the same time so that an optimal device characteristic could be obtained. It is known that $L/T_{\text{si}} > 1$ (i.e., 1.5 or 2) has been reported for double-gate devices. However, according to our investigations, $L/T_{\text{si}} = 1$ may provide a good compromise between the elimination of SCEs and uniformity of fabrication in double-gate-based nanodevices. This investigation is useful for the fabrication of nanodevice and SOC application.

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