Optimizing the Match in Weakly Inverted MOSFET's by Gated Lateral Bipolar Action

Ming-Jer Chen, *Member, IEEE*, Jih-Shin Ho, and Dang-Yang Chang

***Abstract*—The on-chip n-type MOSFET current mirror circuit with different drawn gate widths and lengths has been fabricated, and has been characterized across the wafer with back gate slightly forward biased. The weakly inverted MOSFET device with a small back-gate forward bias represents equivalently the high-gain gated lateral bipolar transistor in low-level injection. Experimental results have exhibited a substantial improvement in the match of the drain current in weak inversion due to action of the gated lateral bipolar transistor, especially for the small size devices. The extensively measured mismatch of the weak inversion drain current has been successfully reproduced by an analytic statistical model with back-gate forward bias and device size both as input parameters. The experimentally extracted variations in process parameters such as the flat-band voltage and the body effect coefficient each have been found to follow the inverse square root of the device area. The mismatch model thus can serve as a quantitative design tool, and has been used to optimize the trade-off between the device area and the match with the forward back-gate bias as a parameter.**

I. INTRODUCTION

THERE are many advantages for operating MOSFET's in subthreshold or weak inversion region: extremely low power dissipation, low-voltage swing, and exponential dependence of drain current on gate-to-source voltage. The latter provides a very useful property for many applications such as analog computation [1], [2]. One of the major disadvantages associated with weakly inverted MOSFET's is the current mismatch between identically drawn devices [1]. Owing to exponential dependencies on the process variations, devices in subthreshold usually exhibit a dramatically large mismatch in current as compared with that in above-threshold [1]. This poor control over the current match in weak inversion can cause a number of unwanted effects in the circuit level. This situation would be made worse if the device area is further reduced for higher density requirement. On the other hand, there indeed exist nonzero back-gate or substrate (or bulk)-to-source biases in the present subthreshold CMOS circuits [1], [2] and thus the dependence of current mismatch in weakly inverted MOSFET's on the back-gate bias must be taken into account. With respect to the well-documented work concerning the mismatch analysis in above-threshold [3]–[5], the study of mismatch in weak inversion is still limited [6]–[8]. In [6], the measured weak inversion current mismatch was observed to be proportional to the inverse square root of device area; however, the effect of back-gate bias on the mismatch was not simultaneously addressed. In [7] and [8], the back-gate reverse bias was judged to be responsible for significant degradation in match. In [8], it was also demonstrated that 1) the current match can be substantially improved by a small back-gate forward bias or equivalently the action of the high-gain gated lateral bipolar transistor in low-level injection [9]–[11]; and 2) the measured dependencies of the mismatch on the back-gate bias can be reproduced by a new statistical model. However, in [8] only a device of 2 μm $\times$ 2 μm was characterized and the dependence of the mismatch on the device area was not reported experimentally or theoretically.

In our work [8], a gated lateral bipolar action in low-level injection has been suggested as a new method of improving the transistor matching in weak inversion. To highlight this method in a more practical way, here we will establish a quantitative design tool that analytically expresses the weak inversion current mismatch as a function of both the device area and back-gate forward bias. First, experimental mismatch data from different drawn gate widths and lengths each measured at different back-gate forward biases will be given in detail. Then an analytic statistical model will be completely derived and employed to simultaneously reproduce a large amount of the mismatch data extensively measured across the wafer. Finally, from the mismatch model the work of optimizing the trade-off between the device area and the match with back-gate forward bias as a parameter will be reported.

II. EXPERIMENT & RESULTS

The measurement of current mismatch in this study was achieved through the n-type MOSFET current mirror circuit as schematically shown in the inset of Fig. 1. The transistors M_1 and M_2 with identical drawn gate size were placed in parallel and close to each other. The on-chip current mirror circuit with four different gate width to length ratios of 1.5 μm/1.5 μm, 3 μm/3 μm, 6 μm/6 μm, and 10 μm/10 μm was fabricated by a 0.8-μm CMOS process. Fig. 2 shows the photograph of the test chip. First in the measurement, the back-gate or substrate-to-source forward bias V_{BS} was fixed when sweeping V_{GS} and V_{DS} simultaneously from 0 V to 2 V in the same steps of 20 mV. This procedure was repeated for each V_{BS} varying from 0.4 V down to 0 V in steps of -100 mV. The choice for the maximum forward bias V_{BS} of 0.4 V ensures the

Manuscript received September 25, 1995; revised December 11, 1995. The review of this paper was arranged by Editor K. Shenai. This work was supported by the National Science Council under Contract NSC 84-2215-E-009-043.

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Publisher Item Identifier S 0018-9383(96)03376-X.

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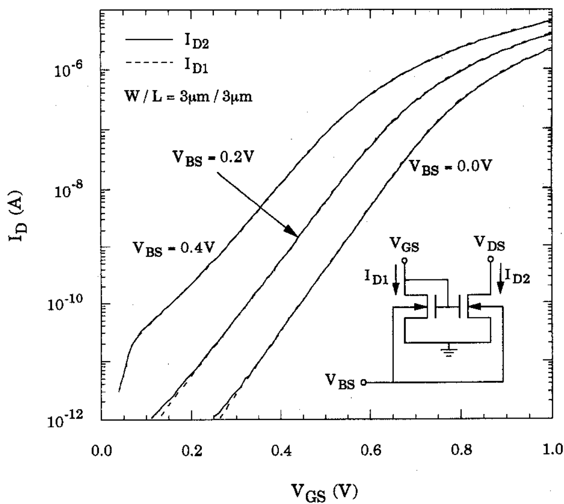


Fig. 1. The drain currents versus gate-to-source voltage characteristics measured from one current mirror circuit with back-gate forward bias as parameter.

action of only the gated lateral bipolar transistor in low-level injection, as explained later. The total measurement of one current mirror circuit for these full ranges consumed about 13 min. Fig. 1 depicts typically the I-V characteristics with $V_{\rm BS}$ as parameter measured from one single current mirror. In Fig. 1 the operating regime of interest in this study, i.e., the weak inversion, is around $V_{\rm GS} > 0$ and I_{D1} (or I_{D2}) < 10 nA. From Fig. 1 we can observe a slight difference between the two drain current versus gate-to-source voltage curves for each given $V_{\rm BS}$.

A total of 50 current mirror circuits for each gate width to length ratio have been measured across the same wafer. Fig. 3 shows in detail the histogram of the measured drain current mismatch measured with $V_{\rm BS}$ as parameter for a specified reference current of 10^{-9} A. Here, the current mismatch δ_I is defined as

$$\delta_I = \frac{I_{D1} - I_{D2}}{I_{D1}} \tag{1}$$

where I_{D1} is regarded as the reference drain current and I_{D2} is the mirrored drain current. The strategy of calculating the δ_I properly from the measured I-V data is described here. First, given a value of I_{D1}, the $V_{\rm GS}$ can be obtained from the I_{D1} versus $V_{\rm GS}$ data using Lagrange interpolation; and then the corresponding I_{D2} can be found from the I_{D2} versus $V_{\rm GS}$ data accordingly. We can confidently calculate δ_I at any specific current without any further measurement. From Fig. 3 we can observe that the mismatch distribution significantly broadens as either the device area is reduced or the $V_{\rm BS}$ increases negatively from 0.4 V to 0 V. We have also found that for given $V_{\rm BS}$ the mismatch distributions measured from the same gate width to length ratio are comparable for other different reference currents in weak inversion. An important statistical parameter for another quantitative evaluation of the current mismatch, σ_{δ_I}, i.e., the standard deviation of δ_I, is defined as

$$\sigma_{\delta_I}^2 = \frac{m\sum_{i=1}^{m}\delta_{I_i}^2 - \left(\sum_{i=1}^{m}\delta_{I_i}\right)^2}{m(m-1)} \tag{2}$$

where m is the sample number. Fig. 4 shows the σ_{δ_I} versus the reference current I_{D1} from each gate width to length ratio measured at five different back-gate forward biases. From Fig. 4 we can observe that for each $V_{\rm BS}$, in the weak inversion region the mismatch is essentially independent of the current while as the current increases and enters into the transition and further above-threshold regions, the mismatch significantly rolls off. The mechanism for transition and then above-threshold regions is that the surface drift component begins to appear and gradually dominate, and simultaneously the dependency of the drain current variation on the threshold voltage variation due to process variation is transferred from exponential to polynomial. Physically speaking, the amount of the inverted carriers increases, thus increasing the ability of shielding the interface states. The data in Fig. 4 suggest two methods for improving the matching in weak inversion: increasing positively the back-gate forward bias and increasing the device area. To highlight these two methods, the measured mismatch data in terms of the standard deviation of the difference in the weak inversion drain current versus the bias $V_{\rm BS}$ for four different gate width to length ratios is plotted in Fig. 5. From Fig. 5 we can observe that the current match for the small size devices can be substantially improved by increasing the back-gate forward bias, while for large devices it tends to be insensitive to the back-gate bias.

III. Mismatch Model

According to [12], the variance or standard deviation $\sigma_{g(x,y)}$ of a function $g(x,y)$ with two random variables x and y can be expressed as

$$\sigma_{g(x,y)}^2 \cong \left(\frac{\partial g}{\partial x}\right)^2 \sigma_x^2 + \left(\frac{\partial g}{\partial y}\right)^2 \sigma_y^2 + 2\left(\frac{\partial g}{\partial x}\right)\left(\frac{\partial g}{\partial y}\right) C_{ov}(x,y) \tag{3}$$

where σ_x and σ_y are the variances of x and y, respectively; and $C_{ov}(x,y)$ is the correlation coefficient between x and y. Thus the variance of the difference in the drain current I_D can be written as function of the variances in the associated process parameters

$$\sigma_{\delta_I}^2 \cong \left(\frac{\partial I_D}{\partial \gamma}\right)^2 \left(\frac{\gamma}{I_D}\right)^2 \sigma_{\delta_\gamma}^2 + \left(\frac{\partial I_D}{\partial V_{\rm FB}}\right)^2 \left(\frac{V_{\rm FB}}{I_D}\right)^2 \sigma_{\delta_{V_{\rm FB}}}^2 \tag{4}$$

where σ_{δ_I}, σ_{δ_γ}, and $\sigma_{\delta_{V_{\rm FB}}}$ are the standard deviation of the difference in the I_D, the body effect coefficient γ, and the flat-band voltage $V_{\rm FB}$, respectively. To facilitate the analysis, we assume $C_{ov}(V_{\rm FB}, \gamma) = 0$. This is a basic assumption in the field [3]–[5] since the process variations are independent of each other in nature. Note that the variations in the gate oxide thickness $t_{\rm ox}$ and channel effective doping concentration N_A are simultaneously reflected in the single parameter γ since γ includes both $t_{\rm ox}$ and N_A, i.e., $\gamma = t_{\rm ox}\sqrt{2q\epsilon_{\rm si}N_A}/\epsilon_{\rm ox}$ where $\epsilon_{\rm si}$ and $\epsilon_{\rm ox}$ are the silicon and oxide permittivities, respectively. The following weak inversion current expression is considered

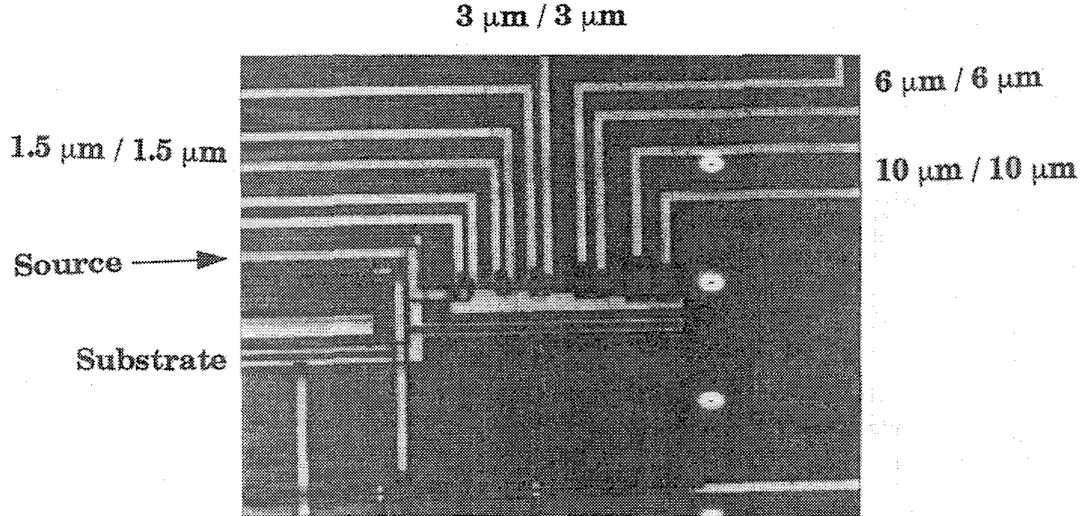


Fig. 2. The photograph of the test chip.

for derivation of the model [13]:

$$I_D = I_0 e^{\frac{q(V_{GS}-V_{th})}{nkT}}$$
$$I_0 \propto \frac{\gamma}{2\sqrt{1.5\phi_f - V_{BS}}} e^{-\frac{q\phi_f}{2kT}} \tag{5}$$

where the critical voltage $V_{th} = V_{FB} + 1.5\phi_f + \gamma\sqrt{1.5\phi_f - V_{BS}}$; the Fermi level $\phi_f = (kT/q)\ln(N_A/n_i)$; the slope $n = 1 + \gamma/2\sqrt{1.5\phi_f - V_{BS}}$; and n_i is the intrinsic concentration. From (5) the derivatives in (4) can easily be derived

$$\frac{\gamma}{I_D}\frac{\partial I_D}{\partial \gamma} = 1 - \frac{q\gamma\sqrt{1.5\phi_f - V_{BS}}}{nkT} - \frac{q\gamma(V_{GS} - V_{th})}{2n^2kT\sqrt{1.5\phi_f - V_{BS}}} \tag{6}$$

and

$$\frac{V_{FB}}{I_D}\frac{\partial I_D}{\partial V_{FB}} = -\frac{qV_{FB}}{nkT}. \tag{7}$$

We have found that the first and third terms of the right-hand side of (6) can be neglected with respect to the second term, implying that the variation in V_{th} contributes predominantly to the variation in I_D. Thus, we obtain a compact model

$$\sigma_{\delta_I} \cong \sqrt{\left(\frac{q\gamma}{nkT}\right)^2 (1.5\phi_f - V_{BS})\sigma_{\delta_\gamma}^2 + \left(\frac{qV_{FB}}{nkT}\right)^2 \sigma_{\delta_{V_{FB}}}^2}. \tag{8}$$

Apparently, (8) analytically expresses the current mismatch in weak inversion as function of the standard deviation of the difference in V_{FB} and γ. Note that (8) does not contain the reference current I_D, indicating that the weak inversion mismatch is independent of the current, as observed experimentally above.

The process parameters available from the foundry are: $t_{ox} = 190$ Å, $V_{FB} = -0.76$ V, and $N_A = 5.6 \times 10^{16}$ cm^{-3}. By substituting these parameter values into (8), the data from four different gate width to length ratios in Fig. 5 have been successfully reproduced over the back-gate forward bias range illustrated. The corresponding extracted variations in process parameters V_{FB} and γ versus the inverse square root of the device area are plotted in Fig. 6. From Fig. 6 we can observe that the standard deviations of the difference in V_{FB} and γ each effectively follow the inverse square root of the device area, in agreement with [3], [4]. Thus, empirically we have

$$\sigma_{\delta_\gamma} = \frac{A_\gamma}{\sqrt{WL}} \quad \text{and} \quad \sigma_{\delta_{V_{FB}}} = \frac{A_{V_{FB}}}{\sqrt{WL}} \tag{9}$$

where A_γ and $A_{V_{FB}}$ are the size proportionality constants for σ_{δ_γ} and $\sigma_{\delta_{V_{FB}}}$, respectively. The extracted values of $A_\gamma = 0.032\,93$ μm and $A_{V_{FB}} = 0.013\,32$ μm lead to good agreement with experimental data as shown in Fig. 6. Further we add the data from the same foundry as cited in [8] to Fig. 6; surprisingly, these two data points each are close to the line of (9). Therefore, a combination of (8) and (9) can serve as an analytic design tool for properly calculating the mismatch with back-gate forward bias and device size both as input parameters.

IV. Optimizing the Match

Here we demonstrate how to apply the above mismatch model in the work of optimizing the trade-off between the device size and the match with back-gate forward bias as design parameter. By means of (8) and (9) along with the above known and extracted parameter values, the calculation results in terms of gate length versus gate width with one specified mismatch value of $\sigma_{\delta_I} = 10\%$ are plotted in Fig. 7 for three different back-gate biases of 0 V, 0.2 V, and 0.4 V. The area under each curve in Fig. 7 for a given V_{BS} yields the mismatch value larger than the specification. From Fig. 7 we can observe that this area or equivalently the device size significantly decreases as the back-gate forward bias is increased. Apparently, the mismatch model can serve as

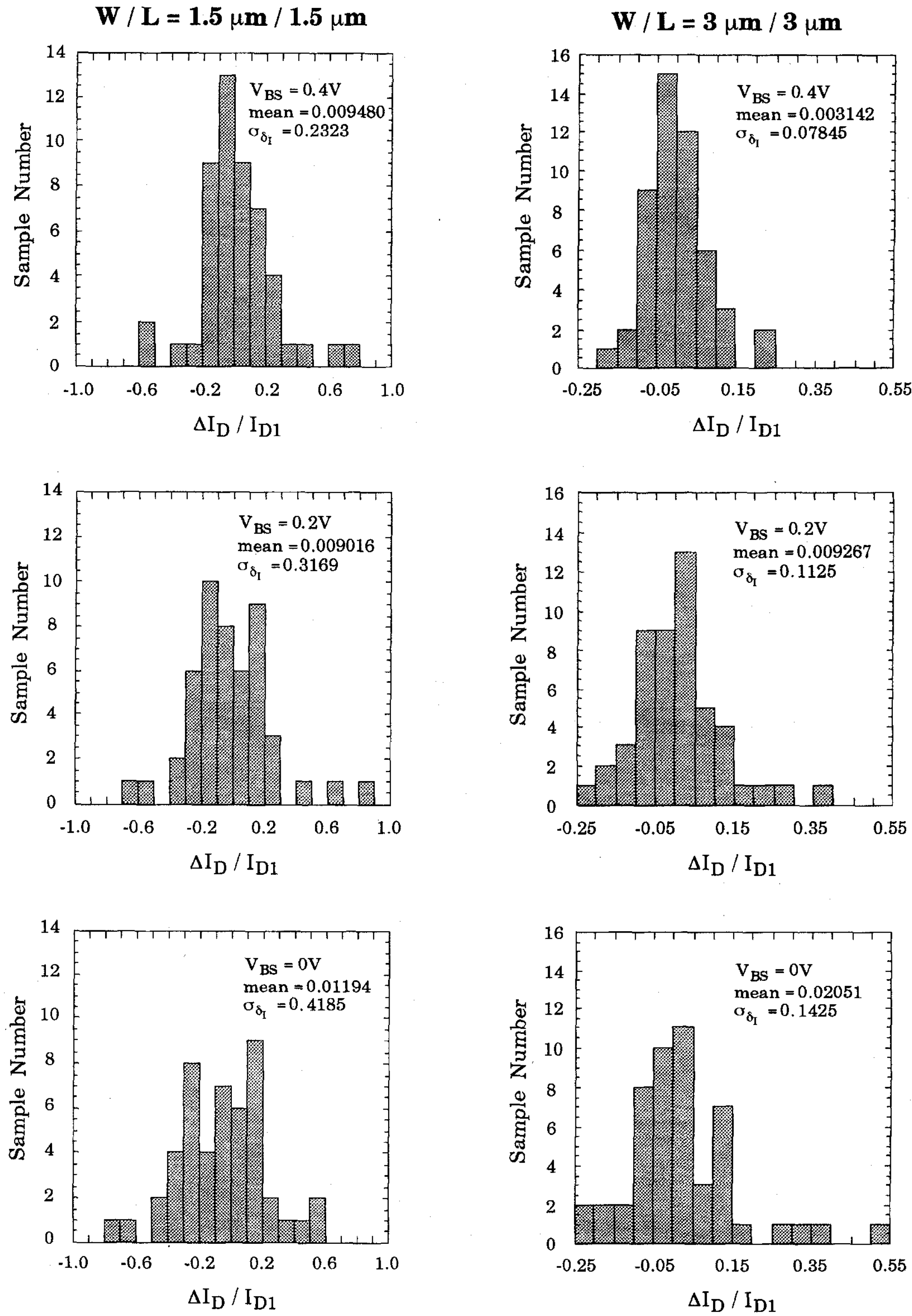


Fig. 3. The histogram of the drain current difference percentage with respect to the reference current of 10^{-9} A measured from the drawn gate width to length ratio W/L of (a) 1.5 μm/1.5 μm and 3 μm/3 μm; and (b) 6 μm/6 μm and 10 μm/10 μm.

a design tool, i.e., the drawn gate width or length can be quantitatively minimized for a specified mismatch. In Fig. 7, for example, to maintain the same accuracy the minimum gate area of 9.5 μm^2 at $V_{\mathrm{BS}} = 0.4$ V is needed to be increased to a large value of about 31 μm^2 for a conventional zero back-gate bias.

Again applying (8) and (9), the calculation results in terms of the back-gate forward bias versus the gate width or length for two different specified mismatch values of σ_{δ_I} =5% and 10% are plotted in Fig. 8. In this figure, the gate width is made equal to the gate length. From Fig. 8 we can observe that the minimum gate width or length can be significantly

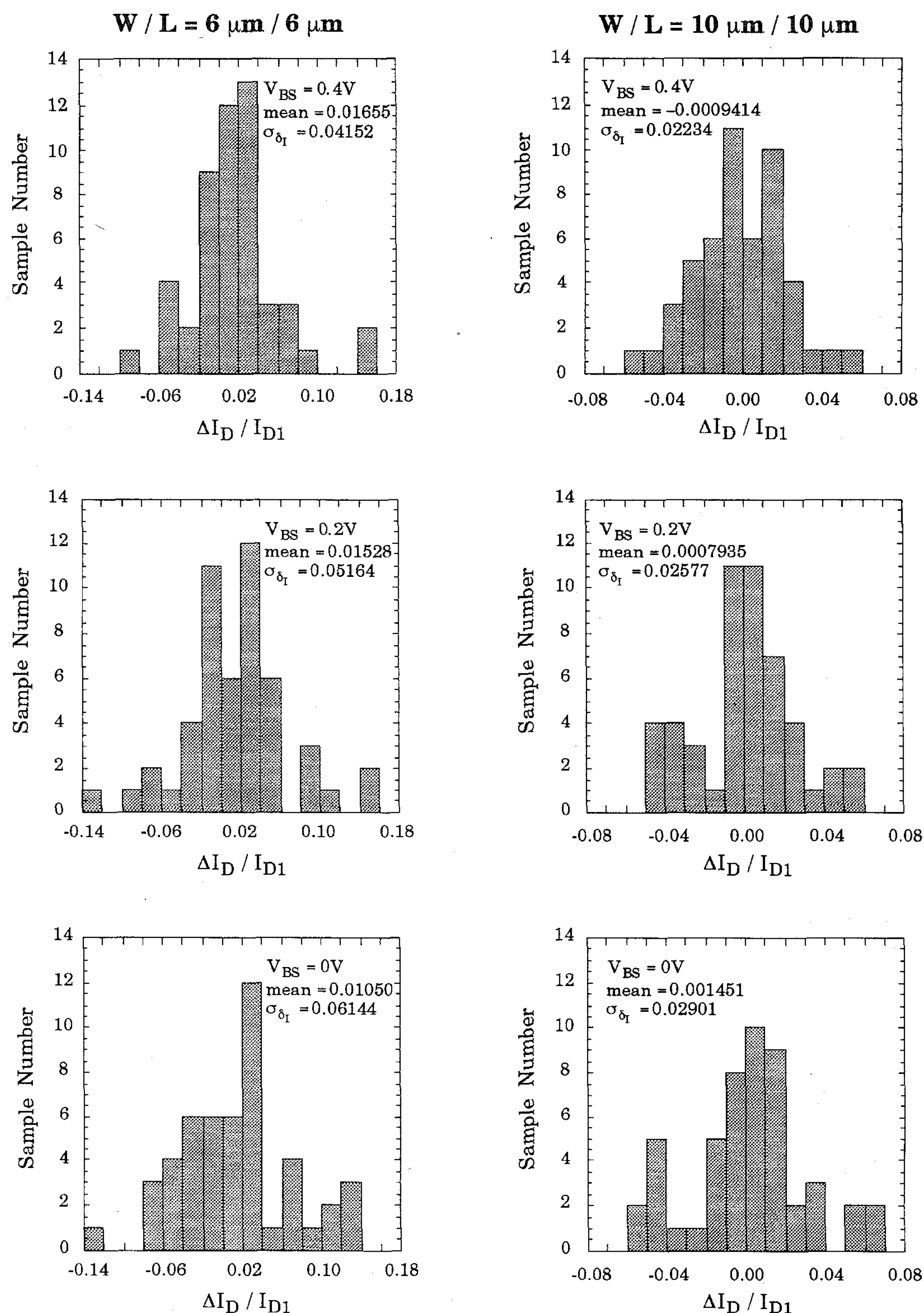


Fig. 3. (*Continued.*)

scaled down by increasing the back-gate forward bias from 0 V, i.e., an about 3.3 and 3.1 times reduction of gate area is obtained at $V_{\mathrm{BS}} = 0.4$ V for $\sigma_{\delta_I} = 5\%$ and 10%, respectively. One guideline for circuit design can be drawn from Fig. 8: if the specification of σ_{δ_I} is strictly decreased from 10% to 5%, the original size of 5.6 μm $\times$ 5.6 μm at $V_{\mathrm{BS}} = 0$ V must be significantly raised to a large value of 11.3 μm $\times$ 11.3 μm while if the $V_{\mathrm{BS}} = 0.4$ V is imposed this value can be suppressed to a comparable magnitude of 6.2 μm $\times$ 6.2 μm. We have also additionally measured the match improvement for the V_{BS} over 0.4 V; however, under such higher forward biases the parasitic bipolar far away the surface, which is primarily responsible for further improvement in the matching, is becoming activated, and may cause the undesirable effects

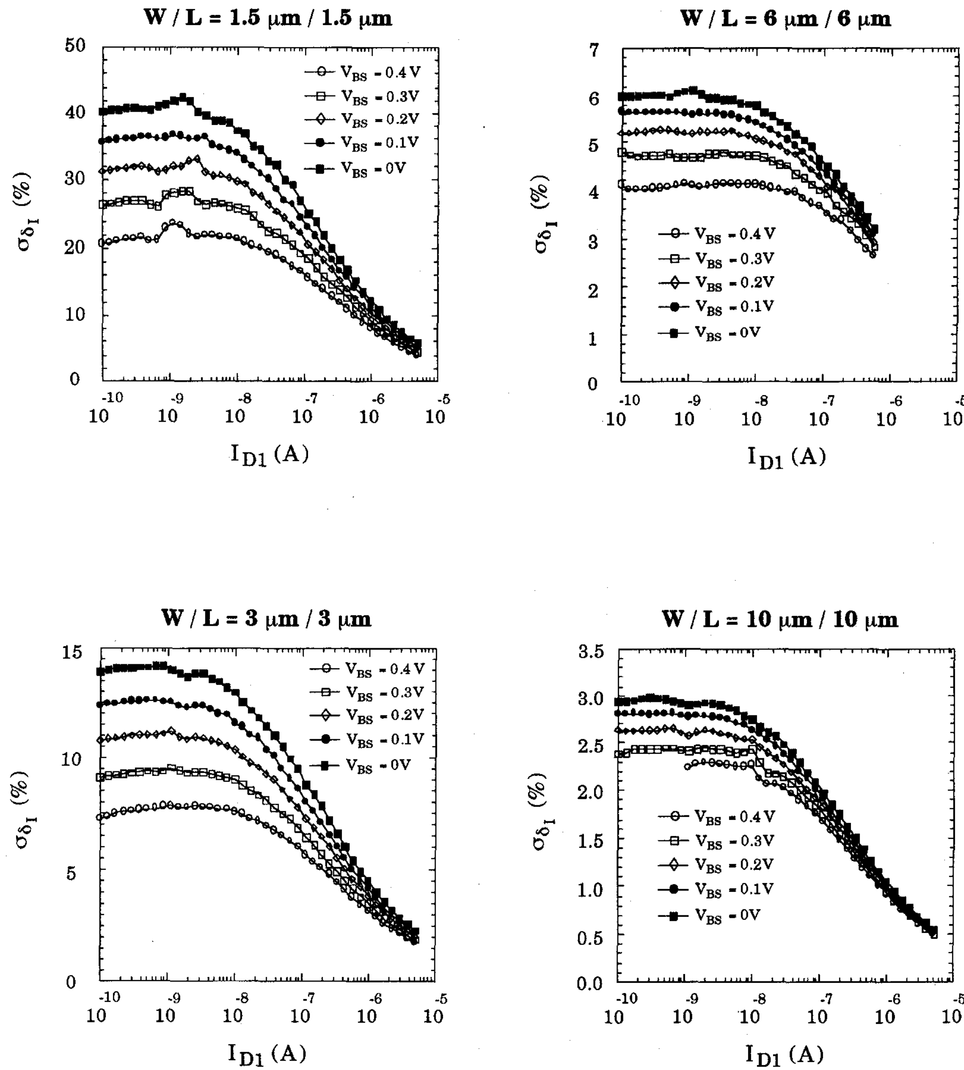


Fig. 4. The standard deviation versus the reference current measured from four different drawn gate width to length ratios with back-gate forward bias as parameter.

such as disturbing the nearby circuitry in the present bulk CMOS process. Thus in this study we limit the maximum V_{BS} to 0.4 V. Under this situation, the MOSFET with back gate slightly forward biased plays equivalently a role of a high-gain gated lateral bipolar transistor in low-level injection [9]–[11], i.e., the base or substrate current is considerably small or the parasitic bipolar action is almost suppressed. The back-gate forward bias can be provided externally or generated on chip. The design of the on-chip back-gate forward bias generation circuit can be made easily by appropriate determination of the V_{BS} value. For example, if the V_{BS} is fixed at 0.3 V, the base or substrate current has been found to have an extremely low value at the order of pA or less [11]; thus the simple bandgap voltage references without the complicated regulator circuitry are enough since in this situation the load current sourcing capability becomes of less concern. It is worthy to note that even at a small V_{BS} = 0.3 V, the gate area at σ_{δ_I} =5% or 10% can be reduced by a considerable factor of about 2.2 with respect to zero back-gate bias.

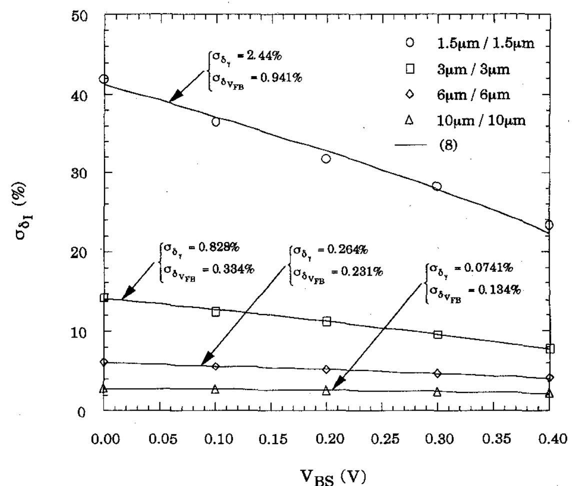
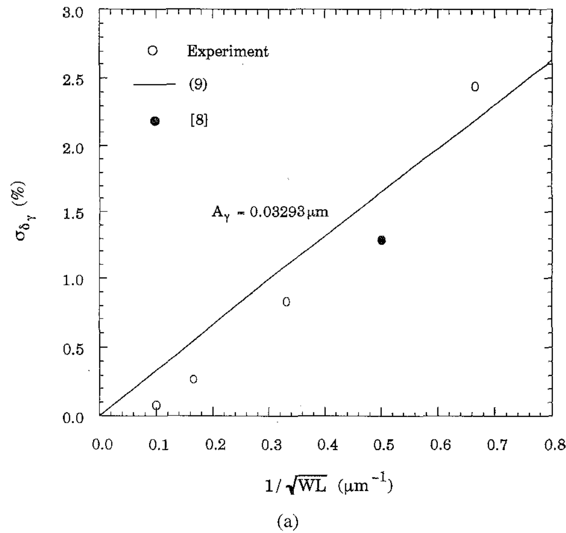
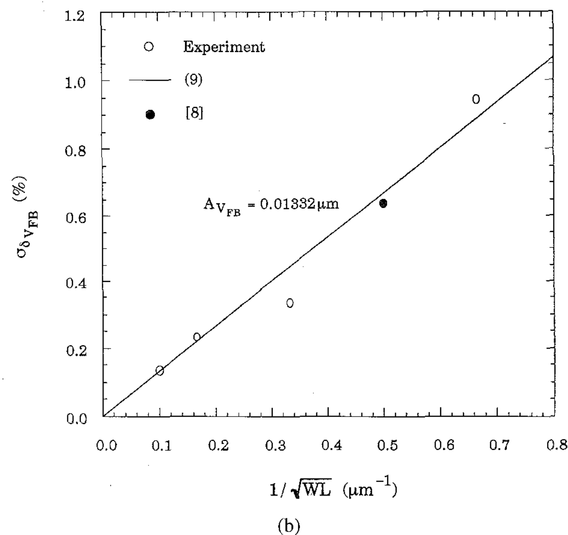


Fig. 5. The measured and calculated standard deviation of the difference in the drain current in weak inversion versus back-gate forward biases.



(a)



(b)

Fig. 6. (a) The measured and calculated standard deviation of the difference in the body effect coefficient γ versus the inverse square root of the device area; and (b) the measured and calculated standard deviation of the difference in the flat-band voltage V_{FB} versus the inverse square root of the device area. The data from [8] are also plotted together.

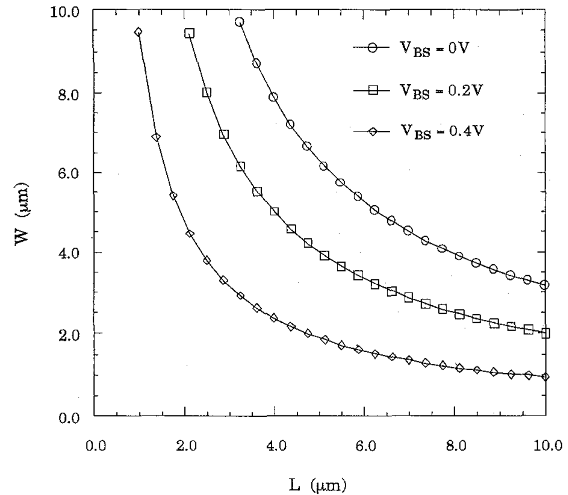


Fig. 7. The calculated gate width versus gate length with back-gate forward bias as parameter for the specification of $\sigma_{\delta_I} = 10\%$.

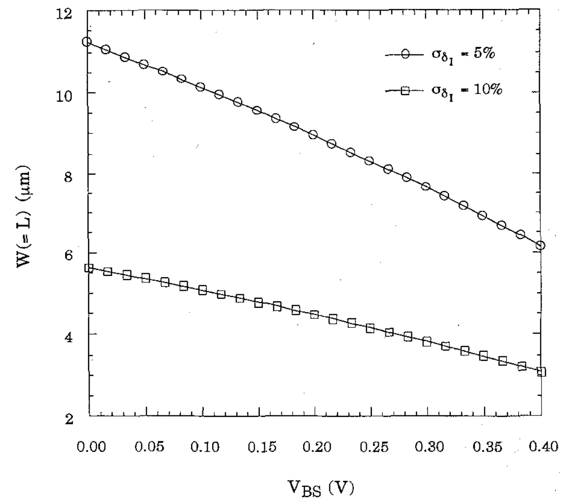


Fig. 8. The calculated back-gate forward bias versus gate width for two specified σ_{δ_I} of 5 and 10%. Here the gate width is made equal to the gate length.

Note that the pure lateral bipolar action in a MOS transistor with substrate-to-source junction forward biased has been well documented in [14], [15] for improving the transistor matching. However, our operating condition and the mechanism responsible both are completely different from those in [14], [15]; that is, in our work the maximum V_{BS} for gated lateral bipolar action is limited to 0.4 V such that the parasitic bipolar far away from the surface is essentially inactive [9]–[11], implying a high current gain feature. Note that for V_{BS} exceeding 0.5 V the gate loses its control over the current, that is, the pure lateral bipolar collector current dominates in the weak inversion and transition regimes [10], [11]. Accurate comparisons can be presented in the following: 1) in [14], [15] the polarity of the V_{GS} is negative (i.e., the MOSFET is completely turned off) while in our work it is positive; and 2) in [14] and [15] the pure lateral bipolar action occurs at $V_{BS} > 0.3$–0.4 V while in our work the gated lateral bipolar action appears in low-level regime of $0 \text{ V} < V_{BS} < 0.4$ V.

V. Conclusion

The on-chip n-type MOSFET current mirror circuits having four different drawn gate width to length ratios each with a large sample number of 50 have been extensively measured over a small back-gate forward bias range. The MOS transistor with substrate-to-source junction slightly forward biased acts as a high-gain gated lateral bipolar transistor in low-level injection. Experiment has exhibited that the drain current match in weak inversion can be substantially improved by action of the gated lateral bipolar in low-level injection, especially for the small size devices. An analytic mismatch

model has been developed and has successfully reproduced the extensively measured data. The extracted variations in the associated process parameters have been found to follow the inverse square root of the device area. The work of optimizing the trade-off between the match and the device size with back-gate forward bias as design parameter has been demonstrated based on the model.

Acknowledgment

The authors would like to thank the Chip Implementation Center, National Science Council, for wafer fabrication and technology support.

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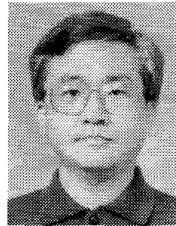

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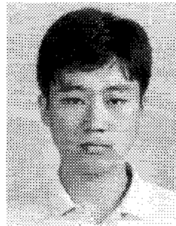

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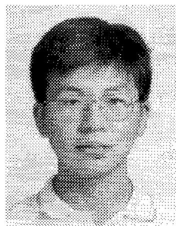

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