Reduction of Leakage Current in Metal-Induced Lateral Crystallization Polysilicon TFTs With Dual-Gate and Multiple Nanowire Channels

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***Abstract*—This letter addresses the leakage current in nickel (Ni) metal-induced lateral crystallization (Ni-MILC) polysilicon thin-film transistors (poly-Si TFTs) with multiple nanowire channels and dual-gate. Experimental results reveal that applying multiple nanowire channels improves the Ni-MILC poly-Si TFT performance. However, the leakage current of both single-gate with single-channel and multiple nanowire channels remains high ($>10^{-8}$ A), because of the field emission of carriers through the poly-Si grain traps and the defects caused by Ni contamination. Applying the dual-gate structure can suppress the electrical filed in the drain depletion region, significantly reducing the leakage current of the Ni-MILC poly-Si TFT, increasing the ON/OFF ratio.**

***Index Terms*—Dual-gate, metal-induced lateral crystallization (MILC), nanowire, thin-film transistor (TFT).**

I. Introduction

HIGH-PERFORMANCE thin-film transistors (TFTs) fabricated on a polysilicon film formed by metal-induced lateral crystallization (MILC) using Ni have attracted much interest because of their potential use in three-dimensional circuit technology [1], liquid-crystal display (LCD) drivers and system-on-panel (SOP) applications [2]. It is a low-cost batch process that yields superior poly-Si films. However, the applications of Ni-MILC poly-Si TFTs remain limited, because the grain boundaries of poly-Si in the channel region substantially degrade performance. The electrical characteristics of the TFTs can be improved by reducing the number of defects in the poly-Si grain boundaries in the channel, and poly-Si TFTs with several multichannels have been reported to effectively reduce grain boundary defects [3], [4]. The Ni-MILC poly-Si TFT suffers from higher leakage current because of Ni contamination during MILC annealing [2], [5], [6] than those by solid phase crystallization and laser crystallization. The Ni impurity atomic percentage in MILC region was determined of 0.08% by secondary ion mass spectroscope (SIMS) analysis [5]. This Ni defects induced leakage current is directly related to the lateral electrical field in the drain depletion region in the off-state [7]. This is another major limitation on Ni-MILC poly-Si TFT applications. According to previous report, the poly-Si TFTs adopted multigate can effectively reduce leakage current, addressing this leakage issue [8].

This work develops a single-gate with a single-channel, a single-gate with multiple nanowire channels, and a dual-gate with multiple nanowire channels in the Ni-MILC poly-Si TFT to study their leakage current and performance. The experimental results reveal that a dual-gate with multiple nanowire channels structure can significantly reduce the leakage current, while maintaining the high performance of the Ni-MILC TFT.

Manuscript received May 27, 2005; revised June 27, 2005. The review of this letter was arranged by Editor J. Sin.

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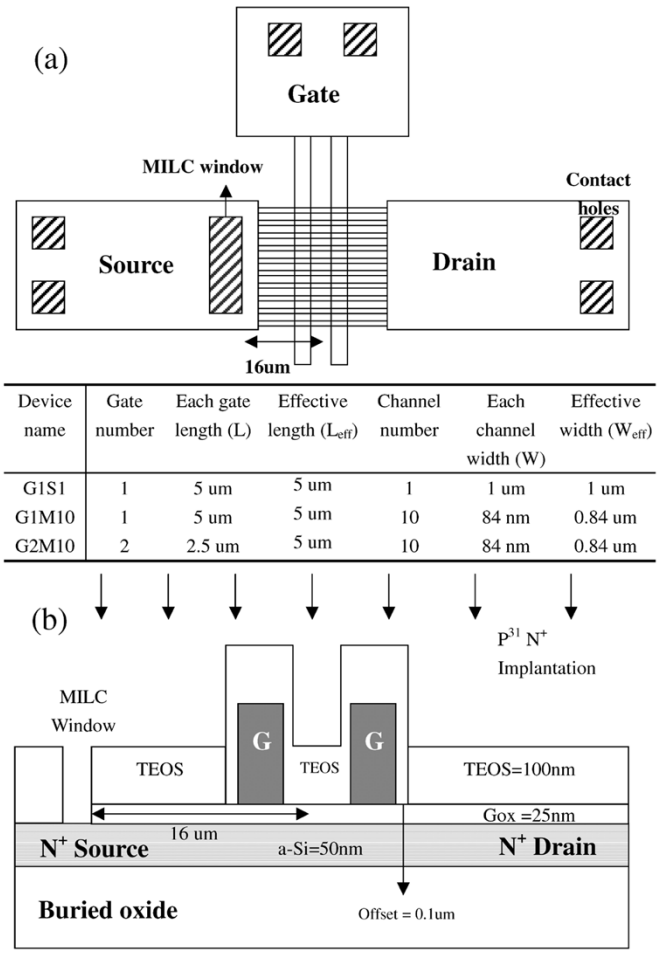
Digital Object Identifier 10.1109/LED.2005.854382

II. Device Sturcture, Simulation, and Fabrication

In this letter, three Ni-MILC poly-Si TFTs, one with a single-gate length of 5 μm and a single-channel width of 1 μm (G1S1), one with a single-gate length of 5 uμm and ten strips of 84-nm wire channels (G1M10), and one dual-gate, each gate with a length of 2.5 μm and ten strips of 84-nm wire channels (G2M10) were fabricated. Fig. 1(a) presents the top view of G2M10 Ni-MILC poly-Si TFT with source, drain, nanowire channels, a Ni-MILC seeding window and a dual-gate. The inset table lists all device dimensions. Fig. 1(b) presents the cross-sectional view of Ni-MILC poly-Si TFT, with a conventional top dual-gate, self-aligned offset MOSFET structure. As the anomalous off-current (leakage current) in the poly-Si TFTs is related to the lateral electrical field in the channel. Fig. 2 presents the simulation results obtained using an ISE TCAD 2-D device simulator of the lateral electrical field of the single-gate (G1) and dual-gate (G2) TFTs with the same bias condition. The peak lateral electrical field (E_m) of the dual-gate TFT is lower than that of the single-gate TFT, indicating that the dual-gate (G2) structure effectively reduces the leakage current of poly-Si TFTs. The inset picture shows scanning electron microscopy (SEM) photography of active pattern with the source, the drain, ten nanowire channels and dual-gate. The each dual-gate length is 2.5 μm, and the each channel width is 84 nm.

The 6-in p-type single crystal silicon wafers were coated 400-nm-thick SiO_2 as the starting materials. Undoped 50-nm-thick amorphous-Si (a-Si) layer were deposited by low-pressure chemical vapor deposition (LPCVD) at 550 °C. Then the active islands, including source, drain, and ten nanowire channels were patterned by Electron Beam lithography (EBL) and transferred



Device name	Gate number	Each gate length (L)	Effective length (L_{eff})	Channel number	Each channel width (W)	Effective width (W_{eff})
G1S1	1	5 um	5 um	1	1 um	1 um
G1M10	1	5 um	5 um	10	84 nm	0.84 um
G2M10	2	2.5 um	5 um	10	84 nm	0.84 um

Fig. 1. (a) Topview plot of G2M10 Ni-MILC poly-Si TFT with source, drain, nanowire channels, Ni-MILC seeding window, and dual-gate. Device dimensions of all proposed Ni-PDMILC poly-Si TFTs are listed in inset table. (b) Cross-sectional view of Ni-MILC poly-Si TFT, which was a conventional top-gate, self-aligned offset MOSFET structure. All devices have the same active channel thickness of 50 nm and a gate TEOS-oxide thickness of 25 nm.

by reactive ion etching (RIE). After defining the active region, the 25-nm-thick tetra-ethyl-ortho-silicate oxide (TEOS-SiO_2) was deposited by LPCVD as gate insulator. Then, 150-nm-thick undoped poly-Si films were deposited immediately on the gate oxide by LPCVD. The poly-Si layers were patterned by EBL and transferred by RIE to define the gate electrode. After gate formation, a 100-nm-thick TEOS-SiO_2 layer as passivation layer was deposited by LPCVD. The poly-Si gate sidewall TEOS-SiO_2 was formed self-aligned offset spacer with the width of 0.1 μm, as shown in Fig. 1(b). Then, the MILC seeding window and contact holes were patterned by EBL and transferred by RIE in the same mask process. Then, a thin 10-nm-thick nickel (Ni) layer was deposited by physical vapor deposition (PVD). The MILC crystallization was carried out at 550 °C for 48 h in an N_2 ambient. The MILC crystallization length of 30 μm, which is longer than 16 μm [Fig. 1(a)] to promise the whole active channel was crystallized by MILC process. After annealing, the unreacted nickel on passivative TEOS-SiO_2 were removed by H_2SO_4 solution at 120 °C with 10 min. Phosphorus ions at a dose of 5×10^{15} cm^{-2} were implanted through the passivative TEOS-SiO_2 to form the n+ gate, source/drain regions, and the self-aligned offset region

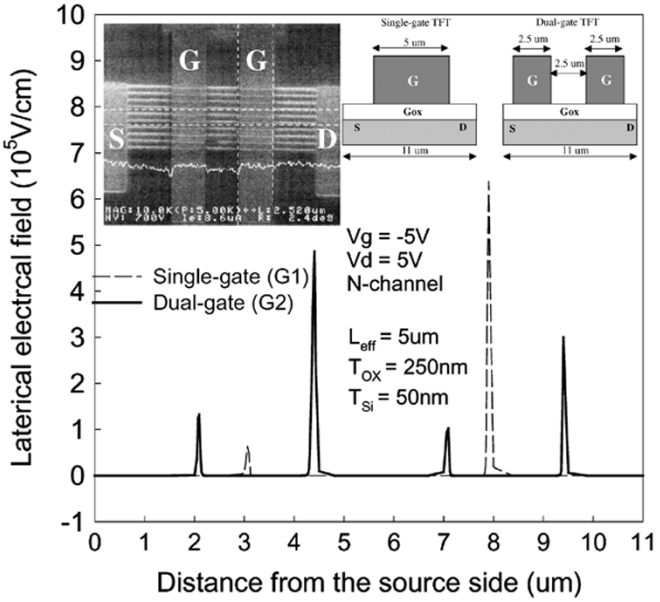
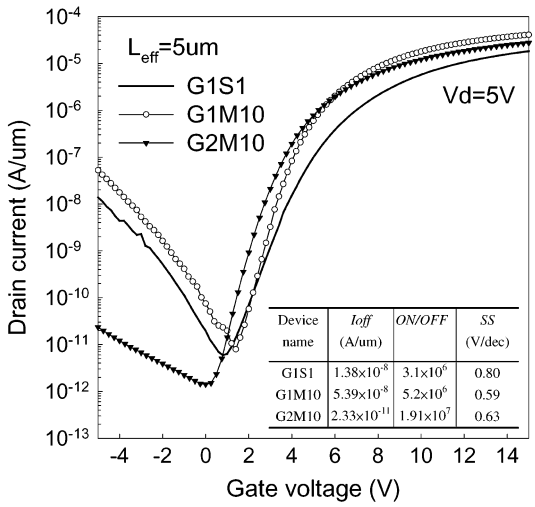


Fig. 2. Off-state lateral electrical field simulation results of single-gate and dual-gates poly-Si TFT by ISE TCAD versus 7 (a 2-D device simulator). The inset scanning electron microscopy (SEM) photography shows the active pattern with the source, drain, ten nanowire channels, and dual-gate.



Device name	*Ioff* (A/um)	*ON/OFF*	*SS* (V/dec)
G1S1	1.38×10^{-8}	3.1×10^{6}	0.80
G1M10	5.39×10^{-8}	5.2×10^{6}	0.59
G2M10	2.33×10^{-11}	1.91×10^{7}	0.63

Fig. 3. Comparison of I_d–V_g transfer characteristics of G1S1, G1M10, and G2M10 Ni-MILC poly-Si TFT with the same device effective length (L_{eff}) of 5 μm. The inset table presents the leakage current (I_{OFF}), maximum ON/OFF ratio and SS.

were formation in the same process step, as shown in Fig. 1(b). Then, the dopants were activated by rapid thermal annealing (RTA) at 850 °C with 30 s. The 300-nm-thick aluminum (Al) layer was deposited by physical vapor deposition (PVD) and patterned for source, drain and gate metal pads. In this letter, no other H or NH_3 plasma passivation was performed. This allowed the intrinsic behavior of the devices to be compared and studied.

III. Results and Discussion

The inset table of Fig. 3 lists all poly-Si TFT parameters, including leakage current (I_{OFF}), ON/OFF ratio and subthreshold swing (SS). The I_{OFF} is defined as the drain current at $V_d = 5$ V

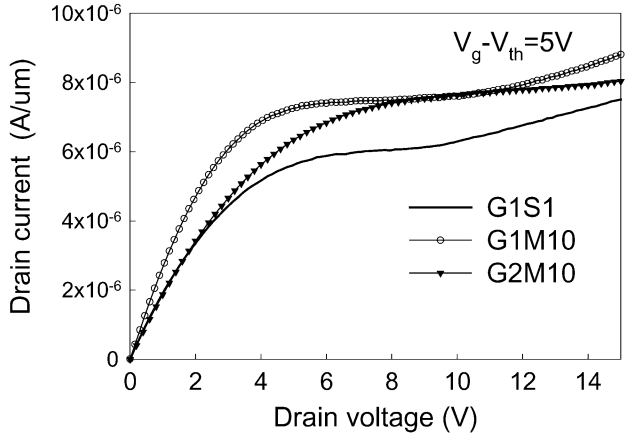


Fig. 4. Comparison of I_d–V_d output characteristics of G1S1, G1M10, and G2M10 Ni-MILC poly-Si TFT with the same device effective length ($L_{\rm eff}$) of 5 μm.

and $V_g = -5$ V, and the ON/OFF ratio is defined as the maximum value of $I_{\rm ON}/I_{\rm OFF}$ at $V_d = 5$ V. By compassion of the single-gate with the single-channel (G1S1) and the ten nanowire channels (G1M10) TFTs in Fig. 3, the G1M10 has a higher ON current, a higher ON/OFF ratio and a steeper SS than the G1S1. These results reveal that the multiple nanowire channels have fewer defects at grain boundaries. However, both G1S1 and G1M10 exhibit severe leakage current ($>10^{-8}$ A). The large leakage current is generated from the poly-Si grain boundary defects and Ni contamination defects via carrier thermionic field emission and tunneling [7]. Notably, the leakage current of G1M10 of 5.39×10^{-8} A is larger than that of G1S1 of 1.38×10^{-8} A. This result can be explained that the G1M10 suffered from a higher lateral field because its gate control was more robust than that of the G1S1 [9], [10] Ni-MILC poly-Si TFT. By comparison of the single-gate (G1M10) and dual-gate (G2M10) with the same ten nanowire channels Ni-MILC poly-Si TFT revealed that the G2M10 leakage current of 2.33×10^{-11} A was significantly lower over three decades, whereas the ON current of G2M10 is close to that of G1M10 TFT. These findings reveal that the dual-gate structure can reduce the peak lateral electrical field in the drain depletion region. Therefore, the leakage current that arises from the field emission and tunneling of carriers through the poly-Si grain traps and the defects associated with Ni contamination was reduced. This finding is consistent with the lower simulation value of the lateral electrical field of dual-gate TFT in Fig. 2. Fig. 4 compares the output curves of G1S1, G1M10, and G2M10 Ni-MILC poly-Si TFTs with the same effective gate length, $L_{\rm eff}$ of 5 μm. The kink-effect of G2M10 is suppressed relative to those of the other TFTs. For the same reason, the dual-gate structure effectively reduces the electrical field, reducing the impaction ionization in the active channel of the Ni-MILC poly-Si TFT. The G2M10 TFT goes into saturation at higher drain bias as compared to G1M10 and G1S1 TFT. This result can be explained that the G2M10 TFT has additional parasitic resistance between two gates [Fig. 1(b)].

IV. Conclusion

Experiment results show that applying ten nanowire channels enhances the Ni-MILC poly-Si TFT performance, including a higher ON/OFF ratio and a steeper SS than that of single-channel TFT. However the leakage current of single-gate Ni-MILC poly-Si TFTs is still high. By applying dual-gate structure can significantly reduce the Ni-MILC TFT leakage current, and increase the ON/OFF ratio. Only the saturation voltage of output curve is higher than single-gate TFT. This novel multichannel and dual-gate Ni-MILC poly-Si TFTs is quite easy and involves no additional processes, thus highly suitable for high-performance MILC poly-Si TFT applications.

References

[1] H. Wang, M. Chan, S. Jagar, V. M. C. Poon, M. Qin, Y. Wang, and P. K. Ko, "Super thin-film transistor with SOI CMOS performance formed by a novel grain enhancement method," *IEEE Trans. Electron Devices*, vol. 47, no. 8, pp. 1580–1586, 2000.

[2] Z. Meng, M. Wang, and M. Wong, "High performance low temperature metal-induced unilaterally crystallized polycrystalline silicon thin film transistors for system-on-panel applications," *IEEE Trans. Electron Devices*, vol. 47, no. 2, pp. 404–409, Feb. 2000.

[3] T. Unagami and O. Kogure, "Large ON/OFF current ratio and low leakage current poly-si TFTs with multichannel structure," *IEEE Trans. Electron Devices*, vol. 35, no. 11, pp. 1986–1989, Nov. 1988.

[4] Y. C. Wu, T. C. Chang, C. Y. Chang, C. S. Chen, C. H. Tu, P. T. Liu, H. W. Zan, and Y. H. Tai, "High-performance polycrystalline silicon thin-film transistor with multiple nanowire channels and lightly doped drain structure," *Appl. Phys. Lett.*, vol. 84, pp. 3822–3824, 2004.

[5] C. F. Cheng, M. C. Poon, C. W. Kok, and M. Chan, "Modeling of metal-induced-lateral-crystallization mechanism for optimization of high performance thin-film-transistor fabrication," in *IEDM Tech. Dig.*, 2002, pp. 569–572.

[6] S. W. Lee and S. K. Joo, "Low temperature polysilicon thin-film transistor fabricated by metal-induced lateral crystallization," *IEEE Electron Device Lett.*, vol. 17, pp. 160–162, Apr. 1996.

[7] K. R. Olasupo and M. K. Hatalis, "Leakage current mechanism in submicron polysilicon thin-film transistors," *IEEE Trans. Electron Devices*, vol. 43, no. 8, pp. 1218–1223, Aug. 1996.

[8] J. H. Park and C. J. Kim, "A study on the fabrication of a multigate/multichannel polysilicon thin-film transistor," *Jpn. J. Appl. Phys.*, vol. 36, pp. 1428–1432, Mar. 1997.

[9] S. Z. R. Han, J. K. O. Sin, and M. Chan, "Reduction of off-current in self-aligned double-gate TFT with mask-free symmertic LDD," *IEEE Trans. Electron Devices*, vol. 49, no. 8, pp. 1490–1492, Aug. 2002.

[10] Y. C. Wu, C. Y. Chang, T. C. Chang, P. T. Liu, C. S. Chen, C. H. Tu, H. W. Zan, Y. H Tai, and S. M. Sze, "High performance and high reliability polysilicon thin-film transistors with multiple nano-wire channels," in *IEDM Tech. Dig.*, 2004, pp. 777–780.