Channel Backscattering Characteristics of Uniaxially Strained Nanoscale CMOSFETs

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***Abstract*—Channel backscattering characteristics of uniaxially strained nanoscale CMOSFETs are reported for the first time. Channel backscattering ratio increases and decreases under uniaxial tensile and compressive strain, respectively. It is found that in sub-100-nm devices, strain-induced modulation of carrier mean-free path for backscattering and reduction in k_BT layer thickness are responsible for the different behaviors of backscattering ratio. Nevertheless, the source-side injection velocity improves irrespective of the strain polarities. The impact of channel backscattering ratio on drive current is also analyzed in terms of ballistic efficiency and injection velocity.**

***Index Terms*—MOSFETs, scattering, uniaxial strain.**

I. Introduction

RECENTLY, various strain techniques are actively pursued to give the device performance a much-needed boost in 90-nm node and beyond [1]–[3]. Mobility enhancement induced by strain in the channel has been widely characterized, however, only half of the mobility enhancement is needed to account for the observed saturation drain current increase [4]. To reconcile with this discrepancy and to understand ballistic transport in a nanoscale transistor, carrier scattering theory has been proposed. As illustrated in the inset of Fig. 1, some of the injected carriers are backscattered near the source end of the channel region within a k_BT layer which has a potential drop of k_BT/q and a thickness of l_0. Since the transmitted carriers ultimately determine the drive current, carrier backscattering ratio r, and injection velocity $v_{\rm inj}$ at the top of source-channel barrier are both critical in determining the drive current $I_{\rm dsat}$. For a higher $I_{\rm dsat}$, reducing r and increasing $v_{\rm inj}$ are desirable [5]. It has been reported that biaxial tensile strain results in backscattering ratio reduction with $Si_{0.7}Ge_{0.3}$ virtual substrate from simulation [6]. However, the influence of uniaxial strain on backscattering ratio has not been clarified yet. In this paper, we report the impact of uniaxial process-induced tensile and compressive strains on channel backscattering ratio for the first time. In addition, the impact of channel backscattering ratio on drive current is also analyzed in terms of mean-free path (MFP), k_BT layer thickness, ballistic efficiency, and injection velocity.

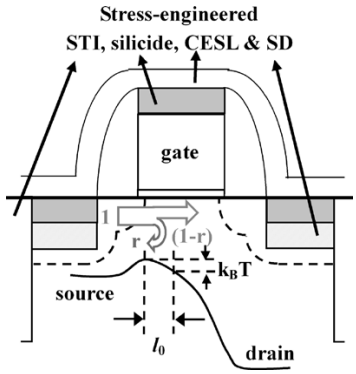

Fig. 1. Schematic structure of PSS MOSFETs. Various stress -engineered processes are employed to achieve uniaxially tensile and compressive strains for nMOSFETs and pMOSFETs, respectively. The inset illustrates that carrier in k_BT layer region is with a backscattering ratio r where the thickness of k_BT layer is l_0.

II. Experimental

Process-strained Si (PSS) MOSFETs fabricated by state-of-the-art CMOS process are studied in this letter [2]. Schematic structure with uniaxial strain engineering is illustrated in Fig. 1, where uniaxial tensile strain for nMOSFETs and uniaxial compressive strain for pMOSFETs are achieved. To minimize barrier height modulation from drain-induced barrier lowering (DIBL), PSS, and control devices with nominally identical DIBL and subthreshold swing are characterized. Drain current improvement of both PSS devices relative to control devices is shown in Fig. 2, all devices with identical inversion C–V characteristics. From scattering theory in [7], drive current in saturation region ($|V_d| = 1$ V) can be expressed as

$$I_{\rm dsat} = W v_{\rm inj} \left[\frac{1 - r_{\rm sat}}{1 + r_{\rm sat}}\right] C_{\rm eff} \left(V_g - V_{T,\rm sat}\right) \qquad (1)$$

where $v_{\rm inj}$, $r_{\rm sat}$, and $V_{T,\rm sat}$ represent injection velocity, backscattering ratio, and threshold voltage, respectively. The ratio $r_{\rm sat}$ is a function of carrier mean-free path for backscattering λ_0 and k_BT layer thickness l_0 ($r_{\rm sat} = 1/[1 + \lambda_0/l_0]$) [5]. The $V_{T,\rm sat}$ is determined by maximum transconductance ($G_{\rm m,max}$) method with DIBL consideration ($\Delta V_{\rm DIBL} = V_{T,\rm lin}@|V_d| = 10\,{\rm mV} - V_{T,\rm sat}@|V_d| = 1$ V, where V_T is defined as the gate voltage when $|I_d| = 0.1$ W/L μA), i.e., $V_{T,\rm sat} = V_{T,\rm lin}(G_{\rm m,max}@|V_d| = 10$ mV$) - \Delta V_{\rm DIBL}$.

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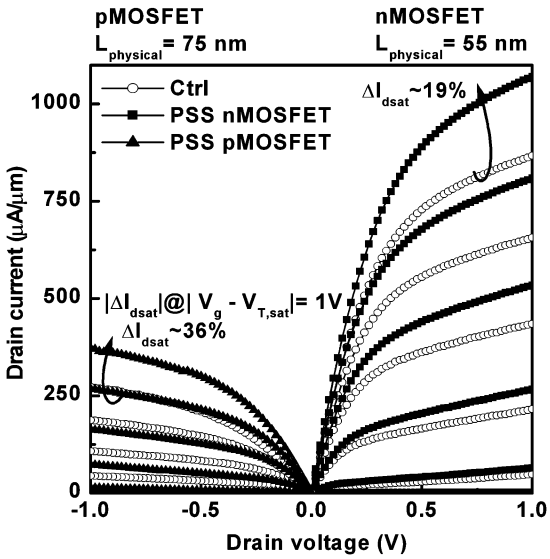

Fig. 2. I_d–V_d characteristics of control and PSS MOSFETs, where PSS nMOSFETs and pMOSFETs exhibit about 19% and 36% improvement of drive current at $|V_g{-}V_{T,\mathrm{sat}}| = |V_d| = 1$ V, respectively. The DIBLs of nMOSFETs are 161 mV/V (control) and 155 mV/V (PSS), and those of pMOSFETs are 114 mV/V (control) and 110 mV/V (PSS). The swings of nMOSFETs are 88 mV/dec (control) and 87 mV/dec (PSS), and those of pMOSFETs are 94 mV/dec (control) and 95 mV/dec (PSS).

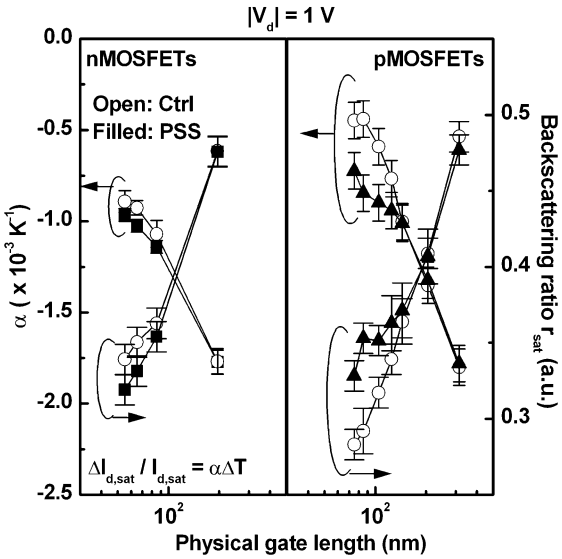

Fig. 3. Effects of uniaxial strain on temperature sensitivity of drain current α, and channel backscattering ratio r_{sat} of control devices, PSS nMOSFETs, and pMOSFETs.

Then, a temperature-dependent analytic model is employed to extract the λ_0/l_0 ratio using the following analytic expression:

$$\begin{aligned}\frac{\partial I_{\mathrm{dsat}}}{\partial T} &= I_{\mathrm{dsat}}\left[\frac{1}{v_{\mathrm{inj}}}\frac{\partial v_{\mathrm{inj}}}{\partial T}+\frac{1+r_{\mathrm{sat}}}{1-r_{\mathrm{sat}}}\frac{\partial}{\partial T}\left(\frac{1-r_{\mathrm{sat}}}{1+r_{\mathrm{sat}}}\right)\right.\\ &\qquad \left.+\frac{1}{V_g-V_{T,\mathrm{sat}}}\frac{\partial(V_g-V_{T,\mathrm{sat}})}{\partial T}\right]\\ &= I_{\mathrm{dsat}}\left[\frac{1}{2T}-\left(\frac{1}{1+r_{\mathrm{sat}}}+\frac{1}{1-r_{\mathrm{sat}}}\right)\frac{\partial r_{\mathrm{sat}}}{\partial T}\right.\\ &\qquad \left.-\frac{\eta}{V_g-V_{T,\mathrm{sat}}}\right]\\ &= I_{\mathrm{dsat}}\alpha \end{aligned} \tag{2}$$

where $\partial r_{\mathrm{sat}}/\partial T = [2r_{\mathrm{sat}}(1-r_{\mathrm{sat}})]/T$. Then α can be derived as follows:

$$\alpha = \frac{1}{T}\left[\frac{1}{2}-\frac{4}{2+\frac{\lambda_0}{l_0}}\right]-\frac{\eta}{V_g-V_{T,\mathrm{sat}}} \tag{3}$$

where α and η represent temperature sensitivity of I_{dsat} and $V_{T,\mathrm{sat}}$, i.e., $\alpha = (I_{\mathrm{dsat1}}-I_{\mathrm{dsat2}})/[I_{\mathrm{dsat2}}(T_1-T_2)]$ and $\eta = (V_{T,\mathrm{sat1}}-V_{T,\mathrm{sat2}})/(T_1-T_2)$ [8]. The measurement temperature is decreased from 298 K to 228 K at a step of 15 K. α and η are extracted from the best-fitted slopes of ΔI_{dsat} and $\Delta V_{T,\mathrm{sat}}$ at different temperatures. The λ_0/l_0 ratio can then be calculated by (3). Lastly, backscattering ratio and ballistic efficiency $B_{\mathrm{sat}}(=[1-r_{\mathrm{sat}}]/[1+r_{\mathrm{sat}}])$ can be deduced.

III. Results and Discussion

The gate length dependence of backscattering factors α and r_{sat} are shown in Fig. 3. α is the dominant factor in determining λ_0/l_0 of MOSFETs since the ratio $|\eta/(V_g-V_{T,\mathrm{sat}})|$ ($|\eta| = 0.5$ to 0.9 mV/K) is smaller than $|\alpha|$. By deducing λ_0/l_0 from α, PSS nMOSFETs demonstrate only a slight increase in λ_0/l_0, while PSS pMOSFETs show significant decrease. In the analytic model, λ_0/l_0 can be obtained directly from experimental results, unlike the method in [9] in which v_{inj} has to be calculated theoretically first before the deduction of λ_0/l_0 from (1). In the nondegenerate case, λ_0 can be written as $\lambda_0 = (2k_BT/q)\ \mu_0/v_{\mathrm{inj}}$ [4] where μ_0 is extracted by the method in [10]. In addition, l_0 is proportional to temperature. Thus, in the derivation of (2), the possible errors of r_{sat} or B_{sat} originate from the assumed temperature dependence of μ_0. In this letter, μ_0 is assumed to be proportional to $T^{-1.5}$ (i.e., theoretical value) [11]. Nonetheless, even by changing the power of temperature dependence to -1.75 (i.e., experimental value) [12], the resultant difference in $\Delta B_{\mathrm{sat}}(= [B_{\mathrm{sat,pss}} - B_{\mathrm{sat,ctrl}}]/B_{\mathrm{sat,pss}})$ is negligible, confirming the insignificance in error caused by the assumed temperature dependence. As shown in Fig. 3, compared to r_{sat} of control devices, the tensile-strained PSS nMOSFET has smaller r_{sat} while compressive-strained PSS pMOSFET has larger r_{sat}. This phenomenon indicates that injected electrons in tensile-strained nMOSFET exhibit less channel backscattering while injected holes in compressive-strained pMOSFET suffer more backscattering. The r_{sat} difference between control and PSS devices becomes more dramatic as L_{physical} is shorter than 0.1 μm. It implies that the ballistic efficiency of tensile-strained PSS nMOSFET is improved but that of compressive-strained PSS pMOSFET is degraded. Q_{inv} for characterized devices is extracted from MOSFETs with an area of 100 μm^2 under strong inversion, taking into account V_T roll-off and DIBL [13]. v_{inj} can then be calculated by $I_{\mathrm{dsat}} = Wv_{\mathrm{inj}}B_{\mathrm{sat}}Q_{\mathrm{inv}}$. As shown in Fig. 4, the injection velocity is improved in both PSS devices, which is ascribed to process-strained induced reduction in carrier effective mass [1]. In addition, ΔI_{dsat} can be related to the sum of Δv_{inj} and ΔB_{sat}. Slight underestimation of ΔI_{dsat} in nMOS is due to minor Q_{inv} difference between PSS and control devices. To further investigate the

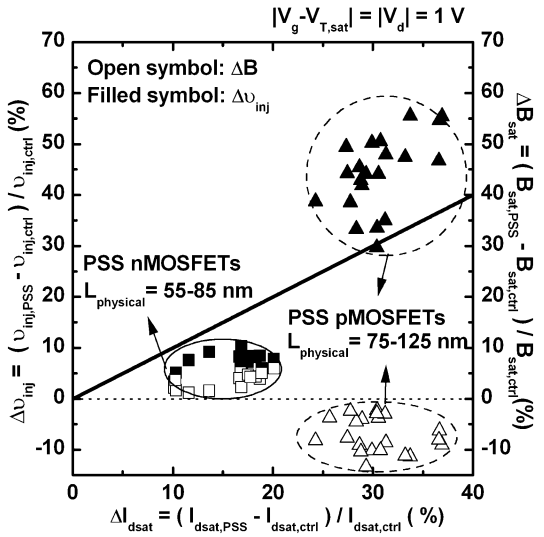

Fig. 4. $\Delta v_{\rm inj}$ and ΔB as a function of $\Delta I_{\rm dsat}$ for PSS nMOSFETs (square symbol) and pMOSFETs (triangle symbol). ΔB and $\Delta v_{\rm inj}$ are represented by open and filled symbols, respectively. The solid line indicates that $\Delta v_{\rm inj}$ (or ΔB) varies linearly with $\Delta I_{\rm dsat}$. For PSS nMOSFETs, both carrier injection velocity and ballistic efficiency are higher than control devices. While for PSS pMOSFETs, slightly lower B and much higher $v_{\rm inj}$ are obtained.

mechanism of strain-induced backscattering modulation, l_0 can be calculated from the ratio of λ_0/l_0 when λ_0 is derived. It is found that l_0 of both PSS devices is reduced to about 90% of that of control devices, and the thinning of l_0 may be due to the strain-induced bandgap shift causing sharper potential profile. In addition, λ_0 is increased in PSS nMOSFETs, which is consistent with the simulation results of [14]. Contrary to nMOSFETs, PSS pMOSFETs exhibit smaller λ_0 than that of control devices, which is probably due to the compressed lattice in the channel inducing much severe carrier scattering. Hence, it is essential to improve not only injection velocity but also ballistic efficiency in order to further enhance the performance of uniaxial-strained MOSFETs in nanoscale regime. Although $I_{\rm dsat}$ of PSS pMOSFETs is improved through the enhancement of injection velocity at the expense of ballistic efficiency loss, ultimate PSS performance boost should therefore be expected if one could conceive a clever method to enhance ballistic efficiency without sacrificing injection velocity.

IV. Conclusion

In this letter, the influence of uniaxial strain on channel backscattering ratio in nanoscale MOSFETs is investigated. Channel backscattering ratio is reduced in tensile-strained nMOSFET but increased in compressive-strained pMOSFET, notwithstanding the increased carrier injection velocity in both cases. Drive current is determined not only by backscattering ratio but also injection velocity. Strain techniques or device structures with simultaneous enhancement of channel backscattering ratio and injection velocity are therefore favorable for ultimate performance boost in mesoscopic regime.

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