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New Findings on the Drain-Induced Barrier Lowering Characteristics for Tri-Gate Germanium-on-Insulator p-MOSFETs

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ABSTRACT This paper investigates the intrinsic drain-induced barrier lowering (DIBL) characteristics for tri-gate germanium-on-insulator (GeOI) p-MOSFETs through theoretical calculation by analytical solution of 3-D Poisson's equation corroborated with TCAD numerical simulation. It is found that, relative to the silicon-on-insulator counterpart, there exists a build-in negative substrate bias in the GeOI PFET. This built-in substrate bias, stemming mainly from the large discrepancy in bandgap between Ge and Si, pulls the carriers toward the channel/BOX interface and thus degrades the DIBL of the GeOI PFET beyond what permittivity predicts. This new mechanism has to be considered when designing or benchmarking tri-gate GeOI p-MOSFETs.

INDEX TERMS Tri-gate MOSFET, multi-gate MOSFET, GeOI, SOI, DIBL.

I. INTRODUCTION

Due to its superior gate control and demonstrated feasibility, tri-gate structure (or multi-gate FinFET) has been used in sub-22nm technology nodes [1], [2]. With the tri-gate structure, Ge channel (with Si substrate) is also being actively pursued to boost the performance for especially p-MOSFETs [3]–[9]. However, one major concern for devices with Ge channel is their short channel effects (SCEs) because of the higher permittivity of Ge channel [9], [10]. In this paper, through theoretical calculation by analytical solution of 3-D Poisson's equation [8] corroborated with TCAD numerical simulation, we examine the drain-induced barrier lowering (DIBL) characteristics for tri-gate germanium-on-insulator (GeOI) p-MOSFETs. We demonstrate that the DIBL of tri-gate GeOI PFETs can be worse than what permittivity predicts, and point out a new mechanism responsible for the degraded DIBL.

II. METHODOLOGY

Fig. 1 shows a schematic sketch of the tri-gate GeOI p-MOSFET with L, W_{fin}, H_{fin}, and T_{box} denoting channel length, fin width, fin height, and the buried-oxide (BOX) thickness, respectively. The doping concentrations of source and drain are 5.5×10^{19} cm^{-3}, and the Ge channel is lightly-doped. Abrupt junction between the source/drain and channel region is assumed. The equivalent oxide thickness (EOT) of the tri-gate device is 0.8 nm.

In this work, we investigate the DIBL characteristics of the tri-gate GeOI p-MOSFET based on corroborated TCAD and analytical calculations with the model details described below. In the subthreshold regime, the semiconductor fin body is fully depleted with negligible mobile carriers. Therefore, the channel potential distribution ϕ_{ch}(x,y,z) in the subthreshold regime can be calculated by solving the following 3-D Poisson's equation:

$$\frac{\partial^2\phi_{ch}(x,y,z)}{\partial x^2}+\frac{\partial^2\phi_{ch}(x,y,z)}{\partial y^2}+\frac{\partial^2\phi_{ch}(x,y,z)}{\partial z^2}=-\frac{qN_{ch}}{\varepsilon_{ch}} \tag{1}$$

where ε_{ch} is the permittivity of the semiconductor fin, and N_{ch} denotes the channel doping concentration.

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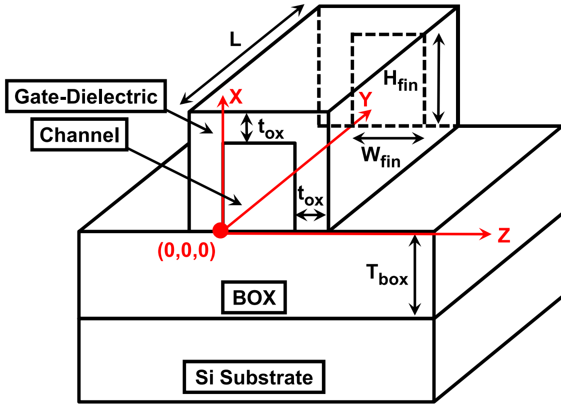


FIGURE 1. Schematic sketch of the tri-gate structure in this study. The doping concentration of the Si substrate is 1E20 cm^{-3} (n-type).

The required boundary conditions can be described as

$$\phi_{ch}(x, y, 0) = V_g - V_{fb} + t_{ox}\frac{\varepsilon_{ch}}{\varepsilon_{ox}}\frac{\partial\phi_{ch}(x, y, z)}{\partial z}\Big|_{z=0} \tag{2a}$$

$$\phi_{ch}\left(x, y, W_{fin}\right) = V_g - V_{fb} - t_{ox}\frac{\varepsilon_{ch}}{\varepsilon_{ox}}\frac{\partial\phi_{ch}(x, y, z)}{\partial z}\Big|_{z=W_{fin}} \tag{2b}$$

$$\phi_{ch}\left(H_{fin}, y, z\right) = V_g - V_{fb} - t_{ox}\frac{\varepsilon_{ch}}{\varepsilon_{ox}}\frac{\partial\phi_{ch}(x, y, z)}{\partial x}\Big|_{x=H_{fin}} \tag{2c}$$

$$\phi_{ch}(x, 0, z) = -\phi_{ms} + V_s \tag{2d}$$

$$\phi_{ch}(x, L, z) = -\phi_{ms} + V_d \tag{2e}$$

where ε_{ox} is the permittivity of gate dielectric, and t_{ox} the physical thicknesses of gate dielectric. V_g, V_s, and V_d are the voltage biases of gate, source, and drain, respectively. V_{fb} represents the flat-band voltage for the gate terminal. ϕ_{ms} is the built-in potential of the source/drain to the channel.

Additionally, the electrostatic potential in the thin BOX region $\phi_{box}(x,y,z)$ can be described by the following 3-D Laplace's equation [11]:

$$\frac{\partial^2\phi_{box}(x, y, z)}{\partial x^2} + \frac{\partial^2\phi_{box}(x, y, z)}{\partial y^2} + \frac{\partial^2\phi_{box}(x, y, z)}{\partial z^2} = 0 \tag{3}$$

The required boundary conditions can be described as

$$\phi_{box}\left(-T_{box}, y, z\right) = V_b - V_{fb2} \tag{4a}$$

$$\phi_{box}(x, 0, z) = \left(V_b - V_{fb2}\right) + \frac{\left(-\phi_{ms} + V_s\right) - \left(V_b - V_{fb2}\right)}{T_{box}}\left(x + T_{box}\right) \tag{4b}$$

$$\phi_{box}(x, L, z) = \left(V_b - V_{fb2}\right) + \frac{\left(-\phi_{ms} + V_d\right) - \left(V_b - V_{fb2}\right)}{T_{box}}\left(x + T_{box}\right) \tag{4c}$$

$$\phi_{box}\left(x, y, -t_{ib}\right) = \left(V_b - V_{fb2}\right) + \frac{\left(V_g - V_{fb}\right) - \left(V_b - V_{fb2}\right)}{T_{box}}\left(x + T_{box}\right) \tag{4d}$$

$$\phi_{box}\left(x, y, W_{fin} + t_{if}\right) = \left(V_b - V_{fb2}\right) + \frac{\left(V_g - V_{fb}\right) - \left(V_b - V_{fb2}\right)}{T_{box}}\left(x + T_{box}\right) \tag{4e}$$

where V_b and V_{fb2} represent the potential and flat-band voltage for the substrate terminal. Furthermore, the potential solutions in (1) and (3) satisfy the following boundary conditions:

$$\varepsilon_{ch}\cdot\frac{\partial\phi_{ch}(x, y, z)}{\partial x}\Big|_{x=0} = \varepsilon_{box}\cdot\frac{\partial\phi_{box}(x, y, z)}{\partial x}\Big|_{x=0} \tag{5}$$

$$\frac{\partial\phi_{ch}(x, y, z)}{\partial y}\Big|_{x=0} = \frac{\partial\phi_{box}(x, y, z)}{\partial y}\Big|_{x=0} \tag{6}$$

where ε_{box} is the permittivity of BOX.

To solve the potential solution in (1) using the above boundary conditions, the 3-D boundary value problems can be divided into three sub-problems, including 1-D Poisson's equation, 2-D and 3-D Laplace's equations. Using the superposition principle, the 3-D Poisson's equation can be solved. The complete channel potential solution is $\phi_{ch} = \phi_{ch,1} + \phi_{ch,2} + \phi_{ch,3}$ where $\phi_{ch,1}$, $\phi_{ch,2}$, and $\phi_{ch,3}$ are solutions of the 1-D, 2-D, and 3-D sub-problems in the channel, respectively. The 1-D solution can be expressed as

$$\phi_{ch,1}(x) = -\frac{qN_{ch}}{2\varepsilon_{ch}}x^2 + Ax + B \tag{7a}$$

The 2-D and 3-D solutions can be obtained using the method of separation of variables:

$$\phi_{ch,2}(x, y) = \sum_{n=1}^{\infty}\left\{\left[\begin{array}{l} B_n\sinh\left(\frac{n\pi}{H_{eff}}y\right) \\ +E_n\sinh\left(\frac{n\pi}{H_{eff}}(L-y)\right)\end{array}\right]\cdot\sin\left(\frac{n\pi}{H_{eff}}x\right)\right\} \tag{8a}$$

$$\begin{aligned}\phi_{ch,3}(x, y, z) &= \sum_{n=1}^{\infty}\sum_{m=1}^{\infty}\left\{\begin{array}{l}\sinh\left[\sqrt{\left(\frac{n\pi}{H_{eff}}\right)^2 + \left(\frac{m\pi}{L}\right)^2}\cdot z\right] \\ +\sinh\left[\sqrt{\left(\frac{n\pi}{H_{eff}}\right)^2 + \left(\frac{m\pi}{L}\right)^2}\cdot\left(W_{eff} - z\right)\right]\end{array}\right\} \\ &\times B_{n,m}\sinh\left(\frac{n\pi}{H_{eff}}x\right)\cdot\sin\left(\frac{m\pi}{L}y\right) + \sum_{i=1}^{\infty}\sum_{m=1}^{\infty}H_{i,m} \\ &\times\sinh\left[\sqrt{\left(\frac{i\pi}{W_{eff}}\right)^2 + \left(\frac{m\pi}{L}\right)^2}\left(H_{eff} - x\right)\right] \\ &\times\sin\left(\frac{i\pi}{W_{eff}}z\right)\cdot\sin\left(\frac{m\pi}{L}y\right)\end{aligned} \tag{9a}$$

The values of A, B and series coefficients (B_n, E_n, $B_{n,m}$, $H_{i,m}$) are given in the APPENDIX. It is noted that the dominant terms of the power series solutions are the first thirty terms. Since the semiconductor fin and the gate dielectric are treated as a homogeneous semiconductor cuboid, the effective width (W_{eff}) and the effective height (H_{eff}) are given by

$$H_{eff} = H_{fin} + t_{ox}\frac{\varepsilon_{ch}}{\varepsilon_{ox}} \quad (10)$$

$$W_{eff} = W_{fin} + \frac{2\varepsilon_{ch}}{\varepsilon_{ox}}t_{ox} \quad (11)$$

After deriving the potential solutions, the subthreshold current can be calculated by [12]

$$I_{ds} = q\mu\frac{n_i^2}{N_{ch}}\frac{kT}{q}\left[1 - e^{-(qV_{ds}/kT)}\right]\cdot\frac{1}{L} \cdot\int_0^{H_{fin}}\int_0^{W_{fin}} e^{q\phi_{ch}(x,y_{\min},z)/kT}dzdx \quad (12)$$

where $\varphi_{ch}(x, y_{min}, z)$ is the highest potential barrier for carrier flow along the y (channel length) direction, and V_{ds} represents the potential difference between drain (V_d) and source (V_s). For devices biased in low V_{ds}, the highest potential barrier occurs at $y_{min} \sim L/2$ due to the nearly symmetrical potential distribution along the channel. The subthreshold model has been verified with the TCAD simulation that numerically solves the 3-D Poisson's equation [11].

III. IMPACT OF BUILD-IN SUBSTRATE BIAS ON DIBL

By using the analytical subthreshold model for tri-gate MOSFETs together with the TCAD numerical simulation [13], Fig. 2(a) compares the DIBL characteristics between GeOI and SOI tri-gate PFETs. It can be seen that for a given drain bias (V_{ds}), the DIBL of the GeOI PFET (open square) is always larger than that of SOI (open circle). Conventional wisdom may attribute this solely to the higher permittivity of Ge. However, even though the permittivity of Ge channel is changed to the same value as Si ($\varepsilon_r = 11.8$), the DIBL of the Ge device (open triangle) is still larger than that of SOI. It infers that, in addition to the channel permittivity, there exists another mechanism degrading the DIBL of the GeOI tri-gate PFET.

Fig. 2(b) further compares the DIBL of GeOI and SOI tri-gate PFETs under various substrate bias (V_{bs}). It can be seen that, after compensating the impact of channel permittivity, the DIBL of the GeOI PFET (open triangle) is larger than that of SOI (open circle) for any given V_{bs}. In fact, as indicated by the arrow mark, there is a constant shift between the two curves. In other words, relative to the SOI device, there exists a build-in negative substrate bias in the GeOI PFET so that the DIBL of the GeOI PFET is worse than what permittivity predicts.

This built-in effective substrate bias, $V_{bs,eff}$, is intrinsic to the GeOI p-MOSFET with Si substrate. It stems from the discrepancy in the source-to-substrate work-function

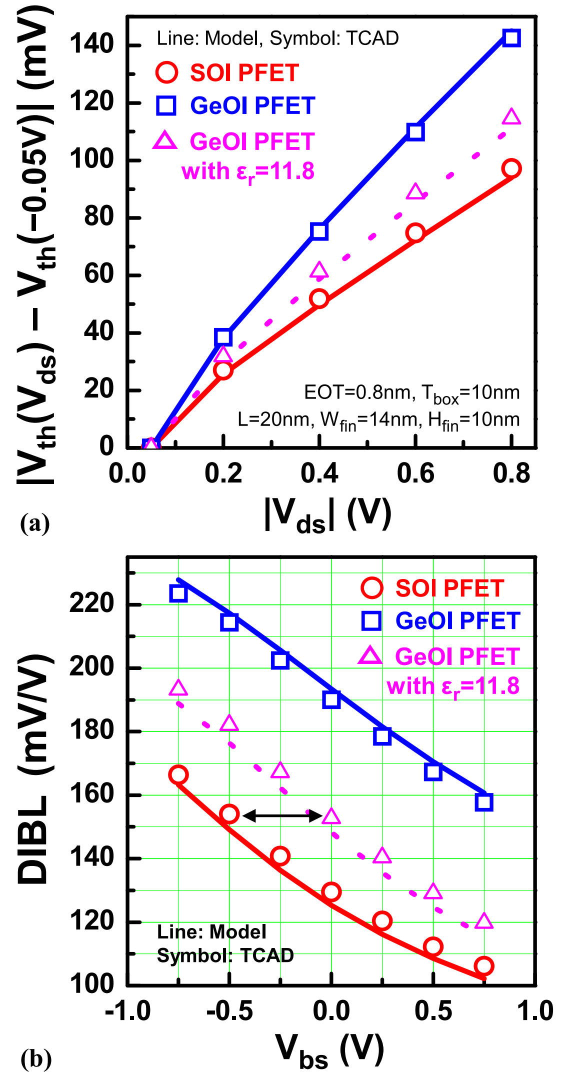


FIGURE 2. **(a) Comparison of DIBL characteristics between GeOI and SOI tri-gate PFETs. The threshold voltage, V_{th}, is extracted by a constant current criterion. (b) Substrate-bias dependence of DIBL [defined as $|V_{th}(V_{ds} = -0.8V) - V_{th}(V_{ds} = -0.05V)|/0.75$] for GeOI and SOI devices. The arrow mark indicates a constant shift between the open-triangle and open-circle curves.**

difference between the GeOI and SOI PFETs, and can be expressed as

$$V_{bs,eff} = \frac{1}{q}\left[\left(E_{g,Ge} - E_{g,Si}\right) + (X_{Ge} - X_{Si}) - kT\ln\left(\frac{N_{v,Ge}}{N_{v,Si}}\right)\right] \quad (13)$$

where E_g, X, and N_v represent the bandgap, electron affinity, and the effective density of states of valence band, respectively. From Eqn. (13), it can be shown that the built-in $V_{bs,eff} = -0.482$ V for the GeOI PFET. Since Ge and Si possess similar X and N_v, the $V_{bs,eff}$ results mainly from their discrepancy in bandgap ($E_{g,Ge} = 0.663$ eV while $E_{g,Si} = 1.12$ eV).

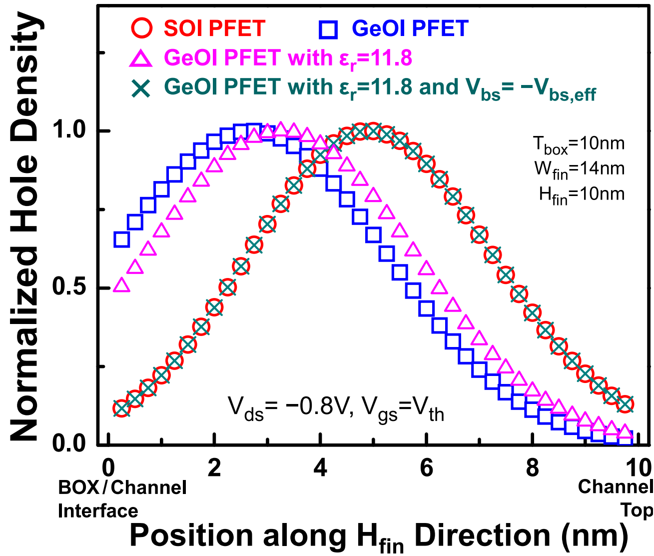
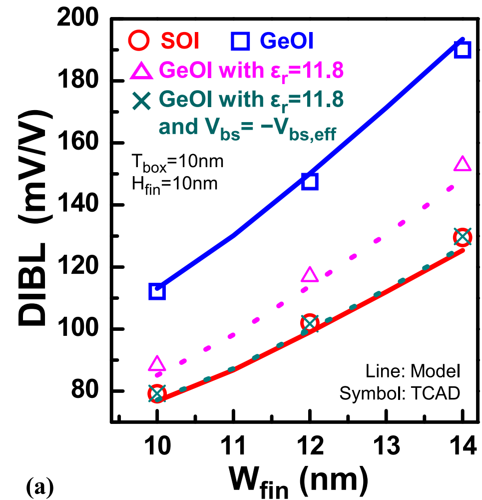


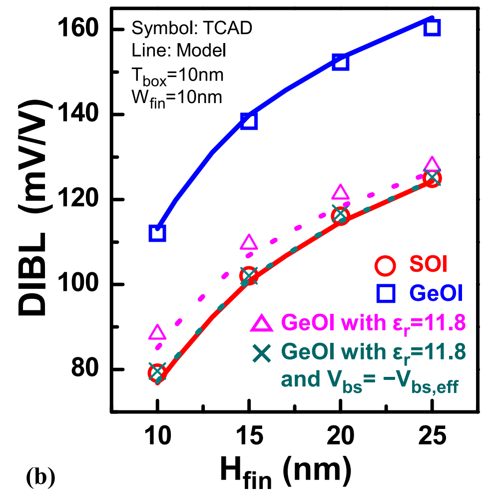
FIGURE 3. Comparison of the carrier profiles along the fin height direction for GeOI and SOI tri-gate PFETs. The hole density distributions are extracted at the location where the highest potential barrier occurs along the channel length direction and in the middle of the fin width.

This negative built-in $V_{bs,eff}$ affects the DIBL of the GeOI PFET because it alters the carrier profile as demonstrated in Fig. 3, which compares the hole distributions along the fin-height (H_{fin}) direction for GeOI and SOI PFETs. It can be seen that the carrier profile for the GeOI PFET (open square) is closer to the channel/BOX interface than that of SOI (open circle), and the impact of channel permittivity is modest (open triangle). However, if the built-in $V_{bs,eff}$ of the GeOI PFET is further compensated by applying an external substrate bias ($V_{bs} = -V_{bs,eff}$), the carrier profile of the GeOI PFET (cross) shows a fairly good agreement with that of SOI (open circle). This validates the accuracy of Eqn. (13), and explains why the DIBL of the GeOI PFET is worse than what permittivity predicts (Fig. 2).

Fig. 4 compares the DIBL characteristics for GeOI and SOI tri-gate PFETs over a wider range of design space. It can be seen that, after considering the impact of the built-in $V_{bs,eff}$ for the GeOI device, the discrepancy in DIBL between GeOI and SOI PFETs can be fully resolved. In addition, it can be seen from Fig. 4(b) and (c) that while the DIBL can be reduced by the fin-height (H_{fin}) and BOX-thickness (T_{box}) scaling, the impact of the built-in $V_{bs,eff}$ on DIBL (the gap between open triangle and open circle) also increases with the down-scaling of H_{fin} and T_{box}. This is consistent with the observations that tri-gate devices with thin BOX and low fin aspect-ratio can enhance the channel potential modulation efficiency through substrate biasing [14], [15]. On the other hand, Fig. 4(a) indicates that shrinking the fin width (W_{fin}) can mitigate the $V_{bs,eff}$ induced DIBL degradation for GeOI tri-gate PFETs.

Finally, it should be noted that the build-in substrate-bias effect reported in this work only occurs for GeOI PFETs. It is negligible in GeOI NFETs due to negligible band offset between conduction bands of Ge and Si.





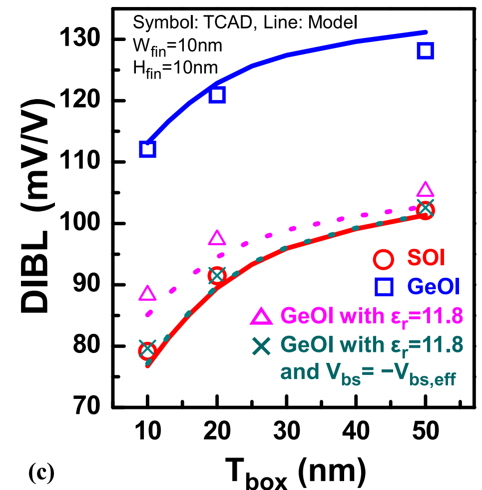


FIGURE 4. Impacts of (a) fin-width (W_{fin}), (b) fin-height (H_{fin}), and (c) BOX-thickness (T_{box}) scaling on the DIBL characteristics of GeOI and SOI tri-gate PFETs. The nominal devices are designed with L = 20 nm and EOT = 0.8 nm.

IV. CONCLUSION

We have investigated the intrinsic DIBL characteristics for tri-gate GeOI p-MOSFETs through analytical calculation corroborated with TCAD numerical simulation. We have

found that, relative to the SOI counterpart, there exists a build-in negative substrate bias in the GeOI PFET. This built-in $V_{bs,eff}$, stemming mainly from the large discrepancy in bandgap between Ge and Si, pulls the carriers toward the channel/BOX interface and thus degrades the DIBL of the GeOI PFET beyond what permittivity predicts. This effect has to be considered in the design and benchmark of tri-gate GeOI p-MOSFETs. Finally, it should be noted that the quantum-mechanical effect is not considered in our modeling and simulation. For GeOI PFETs with small dimensions, the quantum-mechanical effect may widen the bandgap and push the carriers away from the channel/BOX interface, thus reducing the negative impact of the build-in substrate bias on DIBL.

APPENDIX

The values of A and B for the solution of 1-D Poisson's equation, Eqn. 7(a), can be expressed as

$$A = \frac{(V_g - V_{fb}) - (V_b - V_{fb2}) + \frac{qN_{ch}}{2\varepsilon_{ch}}\left(H_{fin}^2 + 2H_{fin}\cdot t_{ox}\frac{\varepsilon_{ch}}{\varepsilon_{ox}}\right)}{H_{fin} + t_{ox}\frac{\varepsilon_{ch}}{\varepsilon_{ox}} + T_{box}\frac{\varepsilon_{ch}}{\varepsilon_{box}}} \tag{7b}$$

$$B = \frac{\varepsilon_{ch}}{\varepsilon_{box}}A\cdot T_{box} + (V_b - V_{fb2}) \tag{7c}$$

In addition, the coefficients B_n and E_n for the solution of 2-D Laplace's equation, Eqn. 8(a), can be described as

$$B_n = \frac{1}{\sinh\left(\frac{n\pi L}{H_{eff}}\right)}\left[\begin{array}{l}\frac{qN_{ch}\cdot(H_{eff})^2}{\varepsilon_{ch}}\left(\frac{2\cdot[(-1)^n-1]}{(n\pi)^3} - \frac{(-1)^n}{n\pi}\right)\\ + \frac{2AH_{eff}(-1)^n}{n\pi}\\ + 2(-\phi_{ms} + V_d - B)\frac{1-(-1)^n}{n\pi}\end{array}\right] \tag{8b}$$

$$E_n = \frac{1}{\sinh\left(\frac{n\pi L}{H_{eff}}\right)}\left[\begin{array}{l}\frac{qN_{ch}\cdot(H_{eff})^2}{\varepsilon_{ch}}\left(\frac{2\cdot[(-1)^n-1]}{(n\pi)^3} - \frac{(-1)^n}{n\pi}\right)\\ + \frac{2AH_{eff}(-1)^n}{n\pi}\\ + 2(-\phi_{ms} + V_s - B)\frac{1-(-1)^n}{n\pi}\end{array}\right] \tag{8c}$$

Besides, the coefficients $B_{n,m}$ and $H_{i,m}$ for the solution of 3-D Laplace's equation, Eqn. 9(a), can be described as

$$B_{n,m} = \frac{1}{\sinh\left(\sqrt{\left(\frac{n\pi}{H_{eff}}\right)^2 + \left(\frac{m\pi}{L}\right)^2}\cdot W_{eff}\right)} \times \left\{\begin{array}{l}\frac{2}{m\pi}\left(1-(-1)^m\right)\times\left[\begin{array}{l}2\left(V_g - V_{fb} - B\right)\frac{1-(-1)^n}{n\pi} + \frac{2AH_{eff}(-1)^n}{n\pi}\\ + \frac{qN_{ch}\cdot(H_{eff})^2}{\varepsilon_{ch}}\left(\frac{2\cdot[(-1)^n-1]}{(n\pi)^3} - \frac{(-1)^n}{n\pi}\right)\end{array}\right]\\ - B_n\frac{2}{L}\cdot\frac{\frac{-1}{m\pi/L}(-1)^m\sinh\left(\frac{n\pi L}{H_{eff}}\right)}{1+\left(\frac{n}{H_{eff}}\times\frac{L}{m}\right)^2} - E_n\frac{2}{L}\cdot\frac{\frac{1}{m\pi/L}\sinh\left(\frac{n\pi L}{H_{eff}}\right)}{1+\left(\frac{n}{H_{eff}}\times\frac{L}{m}\right)^2}\end{array}\right\} \tag{9b}$$

$$H_{i,m} = \frac{\sinh\left(\lambda_{i,m}\cdot T_{box}\right)}{\sinh\left(\lambda_{i,m}\cdot H_{eff}\right)}\times\frac{RHS_{n,m}}{LHS_{i,m}} \tag{9c}$$

where

$$\lambda_{i,m} = \sqrt{\left(\frac{i\pi}{W_{eff}}\right)^2 + \left(\frac{m\pi}{L}\right)^2} \tag{9d}$$

$$LHS_{i,m} = \lambda_{i,m}\cosh(\lambda_{i,m}T_{box}) + \frac{\varepsilon_{ch}}{\varepsilon_{box}}\frac{\sinh\left(\lambda_{i,m}\cdot T_{box}\right)}{\sinh\left(\lambda_{i,m}\cdot H_{eff}\right)}\lambda_{i,m}\cosh\left(\lambda_{i,m}H_{eff}\right) \tag{9e}$$

$$\begin{aligned} RHS_{n,m} = {} & \frac{\varepsilon_{ch}}{\varepsilon_{box}}\sum_{n=1}^{\infty}\left[\begin{array}{l}B_n\frac{2}{L}\cdot\frac{\frac{-1}{m\pi/L}(-1)^m\sinh\left(\frac{n\pi L}{H_{eff}}\right)}{1+\left(\frac{n}{H_{eff}}\times\frac{L}{m}\right)^2}\\ + E_n\frac{2}{L}\cdot\frac{\frac{1}{m\pi/L}\sinh\left(\frac{n\pi L}{H_{eff}}\right)}{1+\left(\frac{n}{H_{eff}}\times\frac{L}{m}\right)^2}\end{array}\right] \\ & \times\left(\frac{n\pi}{H_{eff}}\right)\times\frac{2\left(1-(-1)^i\right)}{i\pi} \\ & + \frac{\varepsilon_{ch}}{\varepsilon_{box}}\sum_{n=1}^{\infty}\left[B_{n,m}\cdot\frac{2}{W_{eff}} \cdot\frac{\frac{(-1)^{i+1}+1}{i\pi/W_{eff}}\sinh\left(\gamma_{n,m}\cdot W_{eff}\right)}{1+\left(\frac{\gamma_{n,m}}{i\pi/W_{eff}}\right)^2}\right] \\ & \times\left(\frac{n\pi}{H_{eff}}\right) \\ & - \sum_{n=1}^{\infty}\left[\begin{array}{l}K_n\frac{2}{L}\cdot\frac{\frac{-1}{m\pi/L}(-1)^m\sinh\left(\frac{n\pi L}{T_{box}}\right)}{1+\left(\frac{n}{t_{ox}}\times\frac{L}{m}\right)^2}\\ + P_n\frac{2}{L}\cdot\frac{\frac{1}{m\pi/L}\sinh\left(\frac{n\pi L}{T_{box}}\right)}{1+\left(\frac{n}{T_{box}}\times\frac{L}{m}\right)^2}\end{array}\right] \\ & \times\left(\frac{n\pi\cdot(-1)^n}{T_{box}}\right)\times\frac{2\left(1-(-1)^i\right)}{i\pi} \\ & - \sum_{n=1}^{\infty}\left[K_{n,m}\cdot\frac{2}{W_{eff}}\cdot\frac{\frac{(-1)^{i+1}+1}{i\pi/W_{eff}}\sinh\left(\Gamma_{n,m}\cdot W_{eff}\right)}{1+\left(\frac{\Gamma_{n,m}}{i\pi/W_{eff}}\right)^2}\right] \\ & \times\left(\frac{n\pi\cdot(-1)^n}{T_{box}}\right) \end{aligned} \tag{9f}$$

$$\Gamma_{n,m} = \sqrt{\left(\frac{n\pi}{T_{box}}\right)^2 + \left(\frac{m\pi}{L}\right)^2} \tag{9g}$$

$$\gamma_{n,m} = \sqrt{\left(\frac{n\pi}{H_{eff}}\right)^2 + \left(\frac{m\pi}{L}\right)^2} \tag{9h}$$

where K_n, P_n, and $K_{n,m}$ stem from the 2-D and 3-D potential solutions in the BOX region:

$$K_n = \frac{2}{\sinh\left(\frac{n\pi L}{T_{box}}\right)}\left(-\phi_{ms} + V_s - B\right)\frac{(-1)^{n+1}}{n\pi} \tag{9i}$$

$$P_n = \frac{2}{\sinh\left(\frac{n\pi L}{T_{box}}\right)}\left(-\phi_{ms} + V_d - B\right)\frac{(-1)^{n+1}}{n\pi} \tag{9j}$$

$$K_{n,m} = \frac{1}{\sinh\left(\sqrt{\left(\frac{n\pi}{T_{box}}\right)^2 + \left(\frac{m\pi}{L}\right)^2} \cdot W_{eff}\right)} \times \left\{ \begin{aligned} &\frac{2}{m\pi}\left(1-(-1)^m\right) \\ &\quad \times \left[\left(V_g - V_{fb} - B\right)\frac{(-1)^{n+1}}{n\pi}\right] \\ &\quad - K_n \frac{2}{L} \cdot \frac{\frac{-1}{m\pi/L}(-1)^m \sinh\left(\frac{n\pi L}{T_{box}}\right)}{1+\left(\frac{n}{T_{box}} \times \frac{L}{m}\right)^2} \\ &\quad - P_n \frac{2}{L} \cdot \frac{\frac{1}{m\pi/L}\sinh\left(\frac{n\pi L}{T_{box}}\right)}{1+\left(\frac{n}{T_{box}} \times \frac{L}{m}\right)^2} \end{aligned} \right\} \tag{9k}$$

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