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Fabrication and Characterization of Film Profile Engineered ZnO TFTs With Discrete Gates

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ABSTRACT By virtue of the film-profile engineering scheme and properly designed device structure, ZnO TFTs with discrete bottom gates and sub-micron channels were fabricated and characterized. In the fabrication, a suspended bridge constructed over the bottom gate is used to tailor the profile of subsequently deposited films. Superior electrical characteristics in terms of ultrahigh ON/OFF current ratio ($\sim 10^{10}$), steep sub-threshold swing (66∼108 mV/dec), and very low off-state leakage current are demonstrated with the fabricated devices. Effects of channel lengths on the device characteristics are also explored. Because of more effective shadowing of the depositing species with a longer suspended bridge, the deposited films become thinner at the central channel. As a result, the device shows more positive turn-on voltage and better subthreshold swing with increasing channel length.

INDEX TERMS Metal oxide, film profile engineering (FPE), ZnO, thin-film transistor.

I. INTRODUCTION

Oxide semiconductors such as ZnO and IGZO have shown their great potential to replace conventional hydrogenated amorphous silicon (a-Si:H) and polycrystalline Si (poly-Si) as the channel material of thin-film transistors (TFTs) due to a number of appealing properties, including high mobility, high transparency, and low process temperature [1], [2]. These merits could satisfy the requirements of most high-resolution large-area displays [3], [4], and flexible electronics [5]–[7]. More recently, attention was also put on the application of back-end-of-line (BEOL) active device technology integrated on advanced large-scale-integration (LSI) chips [8]–[11]. This is in part due to the wide bandgap of the metal oxide materials making the fabricated devices suitable for high-voltage operation.

Recently we proposed and demonstrated a new scheme dubbed film profile engineering (FPE) for the fabrication of oxide-based transistors [12], [13]. This scheme utilizes the features of deposition tools [13] and takes advantages of a shadow mask in affecting the directionality of depositing species [14] to tailor various thin films in a device with desirable profile. Such a concept has been demonstrated previously with ZnO TFTs fabricated with a one-mask process which utilizes the Si substrate as a common bottom gate [12], [13]. Although the fabrication is very simple and suitable for forming the test vehicle for the purpose of efficiently evaluating the properties of the channel materials, it is not practical for circuit applications because of the common-gate configuration. In this work we develop a refined scheme which adopts a discrete bottom gate and the fabricated devices are characterized. Although the fabrication is more complex as additional masks and process steps are needed, it represents a feasible way for the manufacturing of circuitries with the FPE scheme.

II. FPE DEVICE STRUCTURE AND FABRICATION

The device structure is shown in Fig. 1 in which the major thin films, namely, the gate oxide, channel and source/drain (S/D) pads are deposited with various profiles. For gate oxide, the film profile prefers conformal or slightly concave. Concave gate oxide means the oxide thickness is thinner in the central channel region which can help boost the drain current due to the increase in the effective gate

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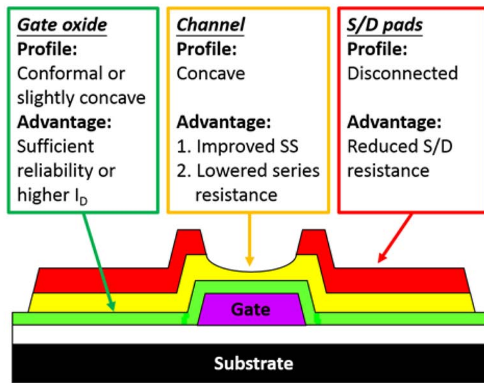


FIGURE 1. Desirable profiles for gate oxide, channel film, and S/D pads in a TFT.

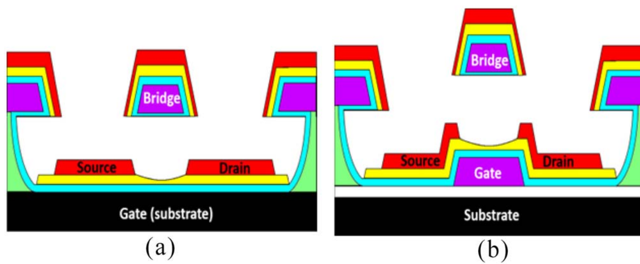


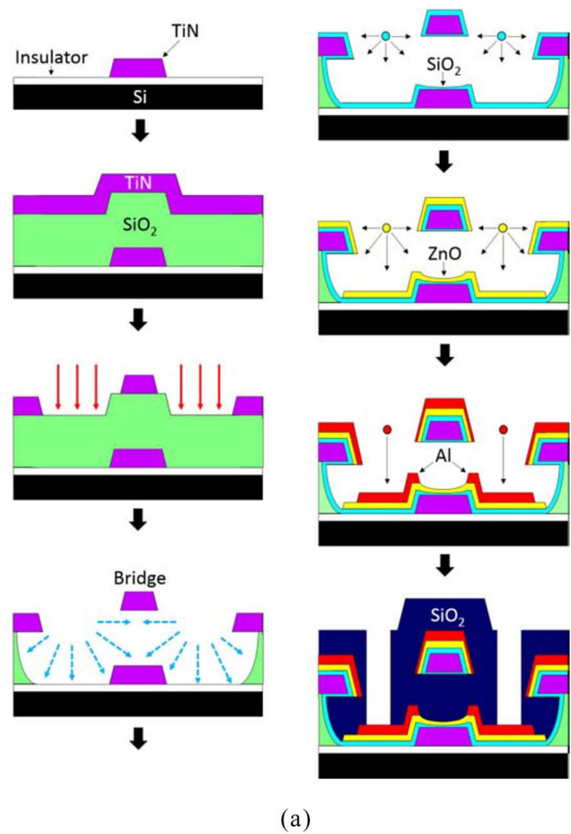
FIGURE 2. (a) Device structures utilized in [12] to demonstrate ZnO TFTs with FPE. For simplicity, the Si substrate is used as the gate. (b) Structure featuring a discrete bottom gate is employed in this paper for device fabrication.

oxide capacitance. However, as the reliability issues and the breakdown voltage are concerned, the oxide cannot be too thin. For the channel film, a highly concave shape helps achieve smaller subthreshold swing (SS). The value of SS of a device with a sufficiently thin channel can be expressed as [15]:

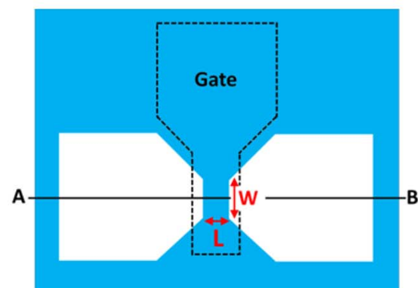
$$SS = 60\left(1 + \frac{qn_t}{C_{ox}}\right), \tag{1}$$

where C_{ox} is the oxide capacitance per unit area, q is the charge of an electron, n_t is the effective areal density of defects located in the channel or at the oxide/channel interface. As the total amount of defects contained in the channel is proportional to the channel thickness, the highly concave channel is expected to be helpful in improving the SS. In addition, the concave shape is advantageous for current spreading toward the metal pads, leading to the reduced parasitic resistances. Finally, the S/D pads should be disconnected for obvious reasons. Good metal contacts can further reduce the S/D resistance and improve the device performance.

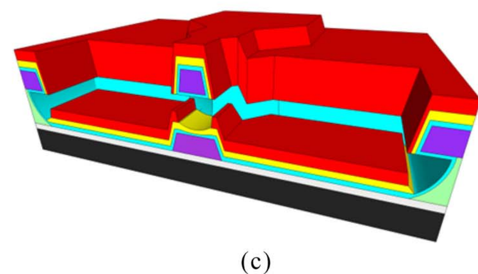
So the name of the game is how to achieve the desirable film profiles in a simple way. One solution is presented in our previous work [12], [13] which takes advantages of a suspended bridge formed on a Si substrate (Fig. 2(a)). The role of the suspended bridge is to shadow the depositing species during subsequent depositions. By selecting appropriate



(a)



(b)



(c)

FIGURE 3. (a) Fabrication sequence of the FPE ZnO TFTs. (b) Mask patterns used in this paper for the definition of discrete bottom gate (dotted line) and S/D opening holes (blue region). W and L represent the width and length, respectively, of the suspended bridge. (c) 3-D cross sectional view of the device (after deposition of Al pads) along line AB in (b).

tools and process conditions, the flux of depositing species reaching the channel region underneath the bridge can be adjusted.

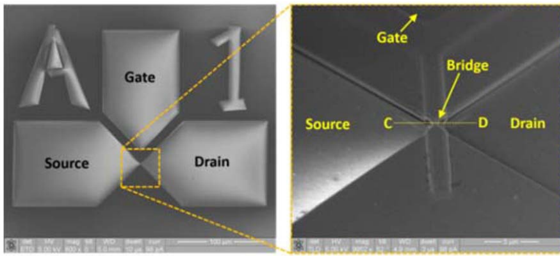


FIGURE 4. SEM images of a fabricated ZnO TFT.

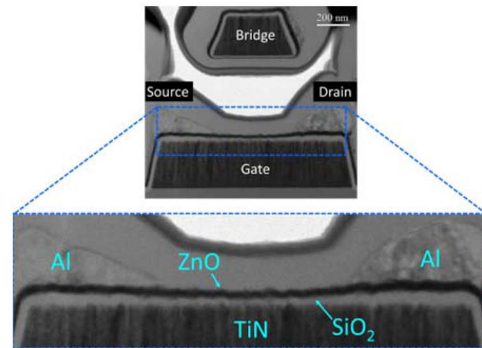


FIGURE 5. Cross sectional TEM image of a fabricated ZnO TFT.

However, the use of the Si substrate as a common bottom gate is not feasible for most of practical applications. To address this issue, we further investigate FPE approach in this study with a refined structure shown in Fig. 2(b) in which the suspended bridge is hanging over the center of a discrete bottom gate.

Fig. 3(a) is the fabrication sequence of the FPE ZnO TFTs. At the beginning, a TiN gate was formed on an insulator-capped Si substrate. Patterning of the gate was done with reactive-ion etching (RIE) with Cl_2/BCl_3 (50/30 sccm) chemistry at 8 mtorr. Next, a 400 nm-thick SiO_2 and a 200 nm-thick TiN were deposited in sequence to serve as the sacrificial layer and the hardmask layer, respectively. After generating a patterned photoresist on the top TiN layer with the mask shown in Fig. 3(b), the hardmask layer was etched by RIE with the same recipe used for gate formation to shape the two S/D opening holes. An isotropic wet etching with an HF-containing solution was executed in the next step to remove the SiO_2 and a suspended bridge was hence constructed. As the bridge was formed, the FPE steps were performed to prepare the three major films of the device. First, a 40nm-thick SiO_2 was deposited by plasma-enhanced chemical vapor deposition (PECVD) under the pressure of 300 mtorr, followed by a 50 nm-thick ZnO deposited by rf sputter with a controlled pressure of 5 mtorr. The isolated S/D pads were then formed by the deposition of a 100nm-thick Al with thermal coater. Finally, a 200 nm-thick SiO_2 was capped to serve as the passivation layer and the ZnO TFTs were completed after the contact hole opening. The structures of the fabricated ZnO TFTs were examined by scanning electron microscopy (SEM) and transmission electron microscopy (TEM). An HP 4156 parameter analyzer was employed to measure the electrical characteristics.

III. RESULTS AND DISCUSSION

Fig. 4 shows the top-view SEM images of a fabricated ZnO TFT with L of 0.4 μm. The cross-sectional TEM image along the line CD in Fig. 4 is shown Fig. 5. In these pictures, it can be seen that the bridge is rightly hung over the TiN bottom gate. In addition, continuous and concave ZnO and SiO_2 films are obtained under the bridge, while two isolated Al pads are formed on the two sides of the bottom gate. These are attributed to the different process conditions of the employed deposition tools pointed out in the former section and prove the practicability of FPE scheme and the importance of deposition films. Note that the channel length of the fabricated TFTs is defined as the distance between the two Al pads and it is almost equal to the bridge length, as the bridge could effectively shadow the deposited species during the evaporating deposition. Typical transfer characteristics of the fabricated ZnO TFTs with various L are shown Fig. 6(a)–(f). As can be seen in the figures, for the devices with L equal to or shorter than 1 μm, very high ON/OFF current ratio ($\sim 10^{10}$), steep subthreshold swing ($<$110 mV/dec), and very low off-state leakage current are obtained. Mobility values are in the range of 4 $\sim$ 12 cm^2/V-s. These results are comparable to previous works on high-performance TFTs with ZnO channel prepared by plasma-enhanced atomic layer deposition (PEALD) [16] or pulsed laser deposition (PLD) [17]. As compared with our previous work on the FPE devices with a simplified one-mask scheme [12], [13], the off-state leakage current is greatly reduced. This is because the designed discrete bottom gate structure adopted in this work can dramatically reduce the gate-to-S/D overlap area to $\sim 1\mu m^2$ from $\sim 10^4 \mu m^2$ of the previous structure. Comparison of device performance among this work and all mentioned previous works is listed in Table 1. Also noted in the Fig. 6 is that negligible drain-induced-barrier-lowering (DIBL) effect is observed from all devices even with L as short as 0.4 μm. Another interesting observation depicted in the figure is that the device with L of 2 μm exhibits no turn-on behavior. Through further characterization we confirm that the measured drain current for this device is actually contributed by the gate leakage current. The root cause of this phenomenon will be addressed later. Fig. 7(a) and (b) are the comparison of transfer curves measured at drain voltage of 0.1 and 3 V, respectively, among the devices with different channel lengths. It can be seen that the on current decreases while the curve moves toward more positive voltage with increasing channel length. The extracted fundamental parameters of TFTs from the transfer curves in Fig. 7(a) for the devices with L ranging from 0.4 to 1 μm are shown in Fig. 8. The subthreshold swing is ranging from 66 to 108 mV/dec and becomes better as the channel length increases.

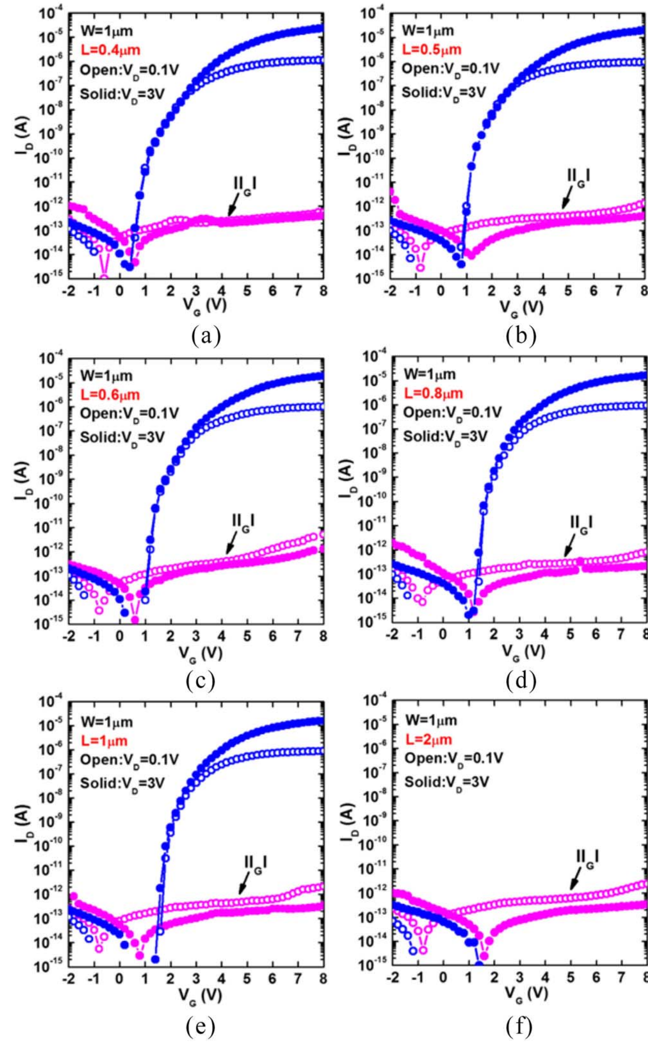


FIGURE 6. Typical transfer characteristics of the fabricated ZnO TFTs with L of (a) 0.4, (b) 0.5, (c) 0.6, (d) 0.8, (e) 1, and (f) 2 μm. The corresponding gate leakage currents are also shown.

The turn-on voltage (V_{ON}), which is defined as the gate voltage when the drain current jumps suddenly, is about 0.4V $\sim$ 1.5V and shifts positively with increasing channel length.

To explain the observed tendencies described above, we've checked the TEM images of devices with different channel length. Fig. 9(a)–(c) are the images collected from the devices with L of 0.4, 0.6, and 2 μm, respectively. The enlarged pictures at the central channel are also shown. It is easy to observe that the film thicknesses of ZnO and SiO_2 in each device are closely related to the bridge length. This is clearly evidenced by showing the thicknesses of Al, ZnO and SiO_2 of devices measured at the channel center as a function of L in Fig. 10. As can be seen, owing to the shadowing effects by the suspended bridge, the thicknesses of ZnO and SiO_2 at the channel center are much thinner than the nominal value. Certainly there is no Al found at the central channel according to the above descriptions about the nature of the thermal coater. From this figure, the devices with a longer L have thinner ZnO and SiO_2, leading to the tendencies shown in Fig. 8 that the V_{ON} increases and subthreshold swing gets better as L increases. The increase in V_{ON} with a thinner channel film is consistent with the previous work [18] owing to the fact that the type of majority carriers in ZnO is electron. The improvement in subthreshold swing can be understood with Eq. 1.

TABLE 1. Subthreshold swing and ON/OFF current ratio achieved in this paper and previous reports [12], [13], [16], [17].

Types of ZnO TFTs	S. S. (mV/dec)	ON/OFF ratio (A/A)
This work	66 ~ 108	~ 10^{10}
One-mask ZnO TFT [12], [13]	71 ~ 187	> 10^9
PEALD ZnO TFT [16]	< 300	> 10^9
PLD ZnO TFT [17]	200	> 10^{10}

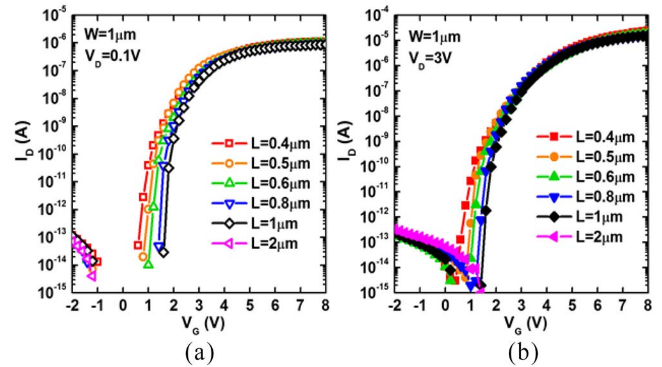


FIGURE 7. Comparisons of the transfer characteristics measured at V_D = (a) 0.1 V and (b) 3 V among ZnO TFTs with various L.

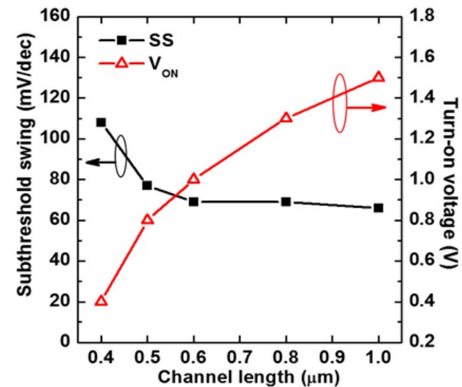


FIGURE 8. Extracted device parameters from the transfer curves shown in Fig. 7(a).

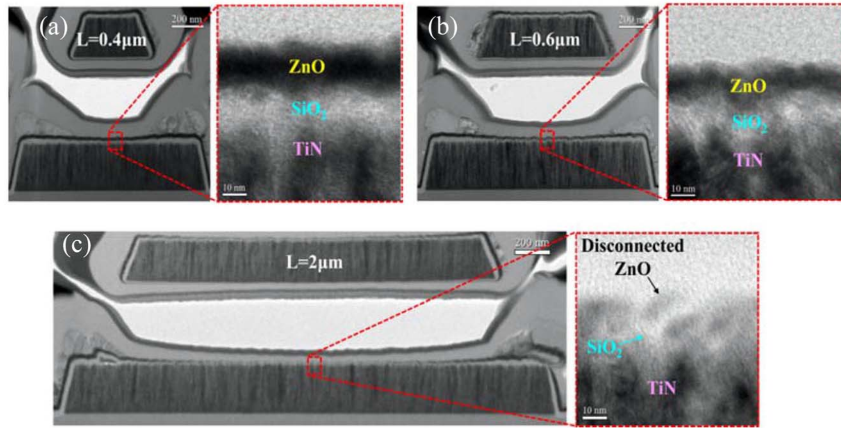


FIGURE 9. Cross sectional TEM images of ZnO TFTs with L of (a) 0.4, (b) 0.6, and (c) 2 μm. The magnified figures at central channel in the devices are also shown and marked in the red frames.

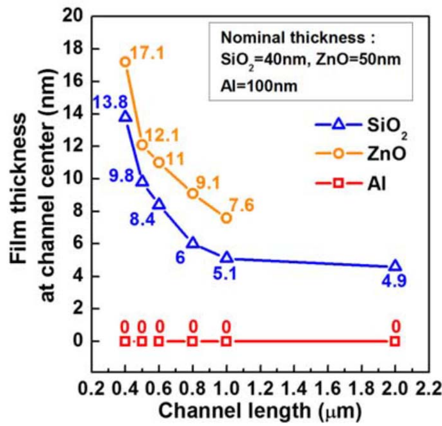


FIGURE 10. Film thicknesses of SiO_2, ZnO, and Al at the channel center in TFTs as a function of channel length.

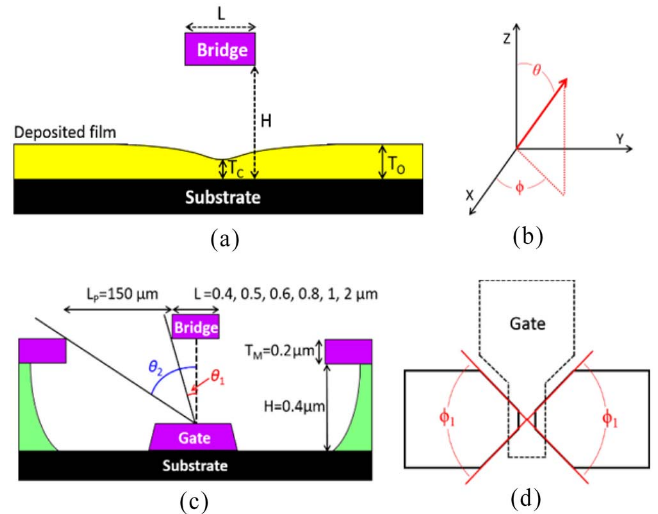


FIGURE 11. (a) Picture revealing the shielding effect of suspended bridge on the profile of the deposited film. The tailored film thickness under the bridge center is denoted as T_C, while T_O represents the nominal thickness at wide open regions. (b) Spherical coordinate system. (c) Influence of cross sectional device structure on the incident angle θ. (d) S/D hole patterns with fan-out angle ϕ_1 determine the range of ϕ.

The dependence of the film thickness at the channel center with L originates from the distinct shadowing ability of the suspended bridge, as we have described in the previous work [13]. Here we elucidate this phenomenon by quantitatively analyzing the relation between the central channel film (ZnO) thickness under the bridge (T_C) and the nominal thickness (T_O) in wide open regions, as shown in Fig. 11(a). Some assumptions are made in the analysis: (1) Sticking coefficient of the deposited species is set to be 1 for simplicity. (2) The energy of gas molecule in the sputter chamber obeys Maxwell-Boltzmann distribution. (3) The scattering of deposited species under the bridge is negligible. The final assumption is based on the fact that the mean free path during the deposition is much longer than the gap height (H). With the above assumptions, the deposition rate (D) of the thin film at a specific position has a simple form proportional to the flux (J) of the deposited species:

$$D = J/N, \tag{2}$$

where N is the density of the thin film. The flux could be further expressed according to the kinetic theory of gases [19]:

$$J = \rho \left(\frac{m}{2\pi kT}\right)^{\frac{3}{2}} \int_0^\infty e^{-\frac{mv^2}{kT}} v^3 dv \int \cos\theta \sin\theta d\theta \int d\phi, \tag{3}$$

where ρ is the density of gas, m is the mass of molecule, k is the Boltzmann constant, T is the temperature, v is the velocity of gas, and θ and ϕ are the incident angles based on the spherical coordinate system shown in Fig. 11(b). From Eq. 3, it is easy to infer that the flux of deposited species at the central channel under the bridge is different from that at the S/D sites due to the differences in the span ranges of θ and ϕ which are mainly determined by the dimensions of the suspended bridge. At the channel center under the bridge, as shown in Fig. 11(c) and (d), significant shadowing of the deposition species by the suspended bridge and

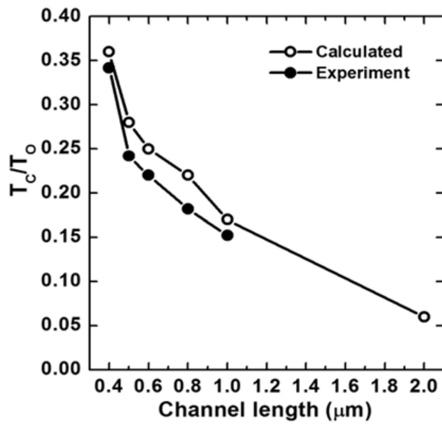


FIGURE 12. Comparison of calculated and experimental results of T_C/T_O.

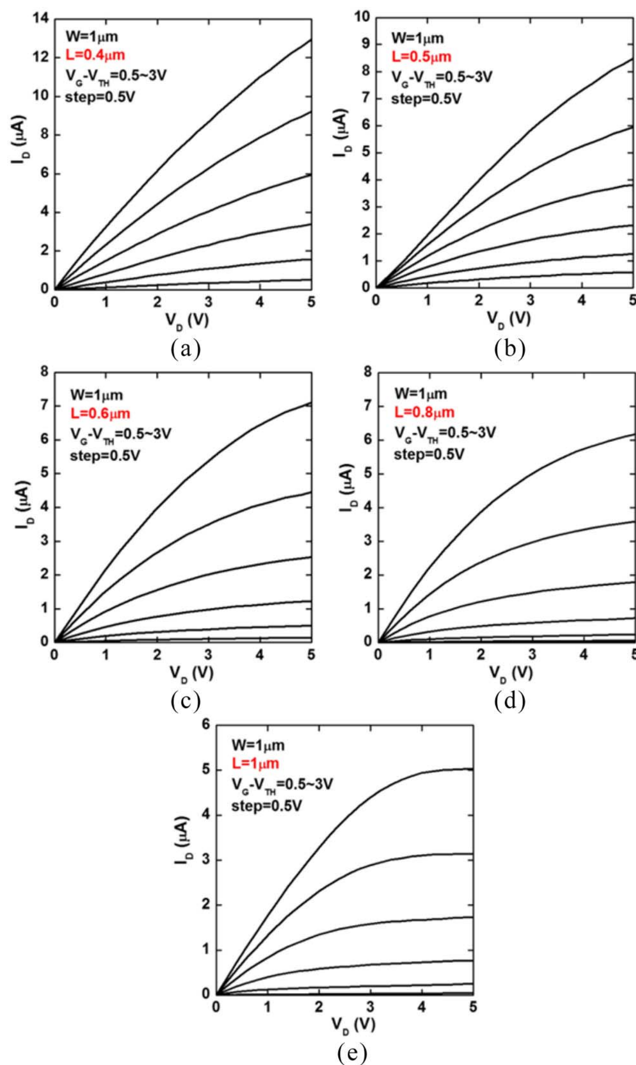


FIGURE 13. Typical output characteristics of the fabricated ZnO TFTs with L of (a) 0.4, (b) 0.5, (c) 0.6, (d) 0.8, and (e) 1 μm.

the hardmask patterns of S/D opening holes is expectable. Ranges of the incident angles can be obtained from the figures as well. For θ, the range is from θ_1 to θ_2 indicated in Fig. 11(c). Key structural parameters in affecting the indent angle θ, including bridge length L, gap height H, thickness of hardmask T_M, and size of opening holes L_P, are also shown in Fig. 11(c). For ϕ, the range is determined by the layout design and it spans $2\phi_1$ from the drawing shown in Fig. 11(d). Hence, in virtue of utilizing Eq. 3 with the above ranges of incident angles, T_C/T_O can be estimated. The results are shown in Fig. 12 in which we can see that the theoretical analysis exhibits a trend similar to what observed experimentally. However, the calculated value is found to be higher than the experimental datum, implying the assumption made on the sticking coefficient (assumed to be 1) of the deposition species needs to be modify. In the device with a longer length, the range of incident angle θ (i.e., $\theta_2 - \theta_1$) for scattered species to deposit under the bridge is larger, resulting in a reduced flux and thus a thinner film at the channel center.

Fig. 13(a)–(e) are the output characteristics of the ZnO TFTs with L of 0.4, 0.5, 0.6, 0.8 and 1 μm, respectively. For simplicity, V_{TH} of the devices is defined by the constant current method as the V_{TH} at W/Lx10^{-7}A. Well-behaved device characteristics are achieved as shown in the figures. The above results confirm that excellent device performance can be obtained with the new FPE structure. By masterfully adjusting geometrical factors in device and cautiously selecting deposition tools, we can ingeniously tailor the profiles and film thicknesses of gate oxide, channel film and metal pads to get well-behaved TFTs. This makes the novel FPE concept promising in the manufacturing of functional circuits such as inverters or ring oscillators.

IV. CONCLUSION

In this work, we've developed a new FPE device structure with a discrete bottom gate. The devices were fabricated with a four-mask process with film-profile-engineered gate oxide, channel oxide, and metal S/D pads. The fabricated ZnO TFTs with sub-micron channel length demonstrate excellent characteristics including ultra-high ON/OFF current ratio of $\sim 10^{10}$ and steep subthreshold swing of 66 $\sim$ 108 mV/dec. The significant reduction in drain leakage current as compared with our previous work is attributed to the greatly reduced overlap area between S/D and gate. Our results also indicate that the device performance is dramatically affected by the structural parameters of the device. The tendencies that transfer curve shifts positively and subthreshold swing becomes better with increasing L stem from the fact that both ZnO and SiO_2 get thinner as L becomes longer are owing to the shadowing effect of the suspended bridge.

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