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Electrical characteristic fluctuation of 16-nm-gate trapezoidal bulk FinFET devices with fixed top-fin width induced by random discrete dopants

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Abstract

In this work, we use an experimentally calibrated 3D quantum mechanically corrected device simulation to study the random dopant fluctuation (RDF) on DC characteristics of 16-nm-gate trapezoidal bulk fin-type field effect transistor (FinFET) devices. The fixed top-fin width, which is consistent with the realistic process by lithography, of trapezoidal bulk FinFET devices is considered in this study. For RDF on trapezoidal bulk FinFETs under the fixed top-fin width, we explore the impact of geometry and RDF on the on-/off-state current and the threshold voltage (V_{th}) fluctuation with respect to different channel fin angles. For the same channel doping concentration, compared with an ideal FinFET (i.e., device with a right angle of channel fin), the off-state current is large in trapezoidal bulk FinFETs with a small fin angle. Furthermore, the short-channel effect and V_{th} variation degrade as the fin angle is getting smaller. The magnitude of the normalized σV_{th} increases 7% when the fin angle decreases from 90° to 70°.

Keywords: Random dopant fluctuation; Characteristic fluctuation; Short-channel effect; Bulk FinFET; Channel fin angle; Trapezoidal; Ideal channel fin; Nonideal channel fin; Top-fin width

Background

Scaling down the CMOS technology node beyond the sub-20 nm causes the transistor to go through a transition from planar to multi-gate FETs such as bulk fin-type field effect transistors (FinFETs) because of the requirement of better gate control and suppression on short-channel effects (SCEs) [1-3]. In addition to the improvement on DC characteristics of individual device, however, continuously scaling not only overcomes challenges on fabrication but also suppresses systematic variation and random effects [4,5]. In practical fabrication, it is difficult to obtain uniform thickness along the height of the fin channel due to limitations in process technology [6]. The actual fins channel may be fabricated as trapezoidal shape and degrade the device performance by significant SCEs. For variability issues, there are many serious fluctuation sources such as random dopant fluctuation (RDF) [7], work-function fluctuation [8], interface trap fluctuation [9], and the line edge roughness [10]. For low-standby-power device technologies and applications, channel doping is still needed to adjust the threshold voltage (V_{th}) and RDF has been shown as the major source of variations for high-K metal gate (HKMG) bulk FinFET devices [11] among various fluctuation factors. Recent researches on RDF and fin-shape effects were reported for FinFET devices; however, the studies on FinFET's RDF were only considered for devices with a rectangular-shape fin channel [12]. However, the channel fin is not always with an ideal shape owing to process challenges. To the best of our knowledge, a research which simultaneously considers the aforementioned issues has not been well investigated yet.

In this study, we explore the RDF on DC characteristics of 16-nm-gate trapezoidal bulk FinFETs with the fixed top-fin width (W_{top}) condition. We further intensively analyze the on-/off-state current characteristic and V_{th}'s fluctuation of the 16-nm-gate trapezoidal HKMG bulk FinFET. The article is organized as follows. The 'Methods' section introduces the simulation technique for studying the RDF on trapezoidal bulk FinFET devices

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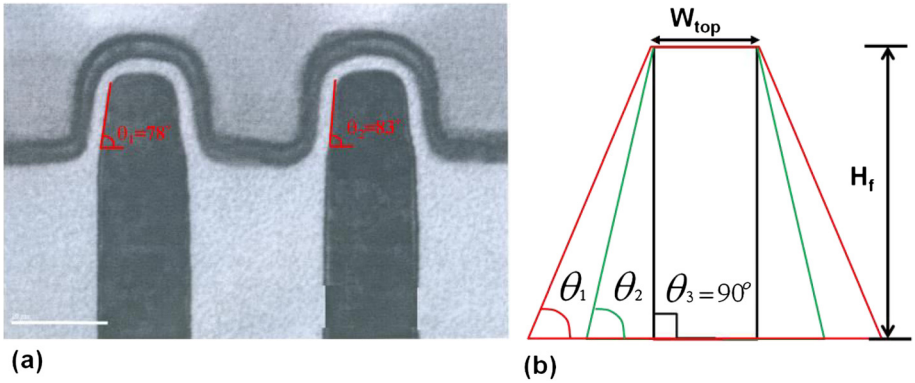


Figure 1 TEM and schematic cross-section views of channel fin. (a) A TEM view of realistic shape of fabricated channel fin to show the fin angle variation. **(b)** The schematic cross-section view of channel fin with respect to different fin angles for devices with a fixed-top-fin width (W_{top}), in this study.

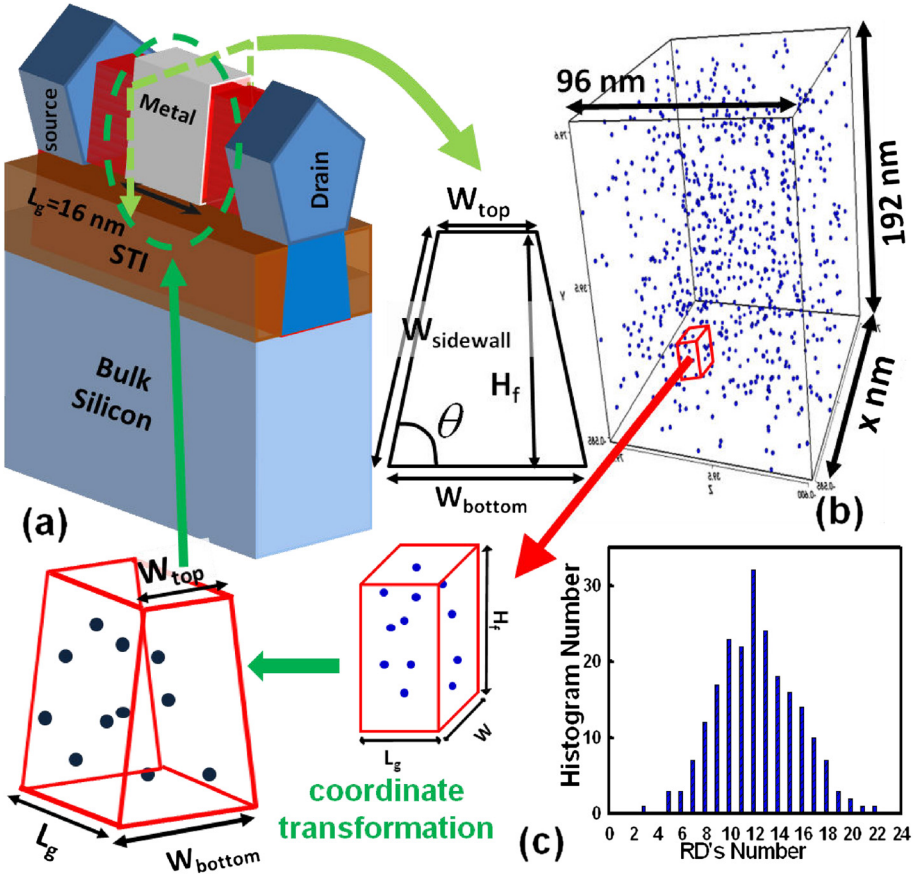


Figure 2 The large-scale statistical device simulation method of RDF on the device's channel region. (a) The schematic structure of the 16-nm-gate trapezoidal bulk FinFET device and the cross-section view of fin channel. **(b)** Discrete dopants are randomly distributed in a large cube with the average concentration of 1.5×10^{18} cm^{-3}. The number of RDs is dependent on the magnitude of the fin angle. **(c)** The right plot is the bar chart of distribution of number of dopants of each fin-angle bulk FinFET. The left plot is the procedure of generating fluctuated cases. The cube is partitioned into many subcubes. The coordinate transform is performed on those subcubes to make them become trapezoidal-shaped channels and map them into device channel regions.

Table 1 The simulation settings of nominal bulk FinFET devices

Fin angle θ(°)	90	85	80	75	70
Top-fin width, W_{top} (nm)	8	8	8	8	8
Bottom-fin width, W_{bottom} (nm)	8	13.6	19.3	25.1	31.3
Total fin width, W_{total} (nm)	72	72.24	72.99	74.26	76.1
Fin height, H_f (nm)	32				
Effective oxide thickness, EOT (nm)	1				
Gate length, L_g (nm)	16				
Source/drain doping (cm¯3)	1.0E20				
Punch-through stopper (cm¯3)	1.5E19				
Channel doping (cm¯3)	1.5E18				
Drain voltage, V_{DD} (V)	0.8				

The V_{th} are calibrated to 250 mV.

with different fin angles and the same W_{top}. The 'Results and discussion' section focuses mainly on the analysis and discussion of characteristic fluctuation from RDF of 16-nm-gate trapezoidal HKMG bulk FinFET devices. Finally, we draw conclusions and suggest future work.

Methods

The device configuration and simulation technique

Figure 1a shows various TEM views of realistic shape of fabricated two-channel fin in 16-nm technological node. Due to the process capabilities, the fin angles θ_1 and θ_2, as shown in these two images, may vary with the lithography and etching, etc. Therefore, devices with different trapezoidal shapes are fabricated. In this study, we assume the top-fin width is fixed at 8 nm for the 16-nm-gate HKMG bulk FinFET devices. Figure 1b shows the schematic cross-section view of channel fin for the identical-W_{top} setting. The fin angle (θ) is thus defined as the angle between the bottom line and sidewall and ranges from 70° to 90°. Besides the fixed W_{top}, the channel doping concentration, which means the needed number of impurity in the channel region increases when the fin angle is getting smaller, is set the same for all simulation cases.

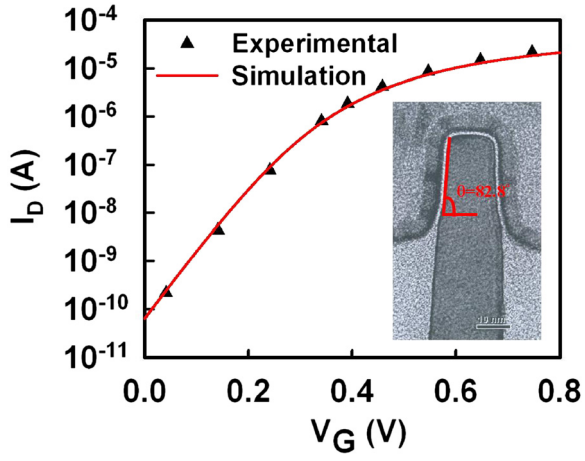
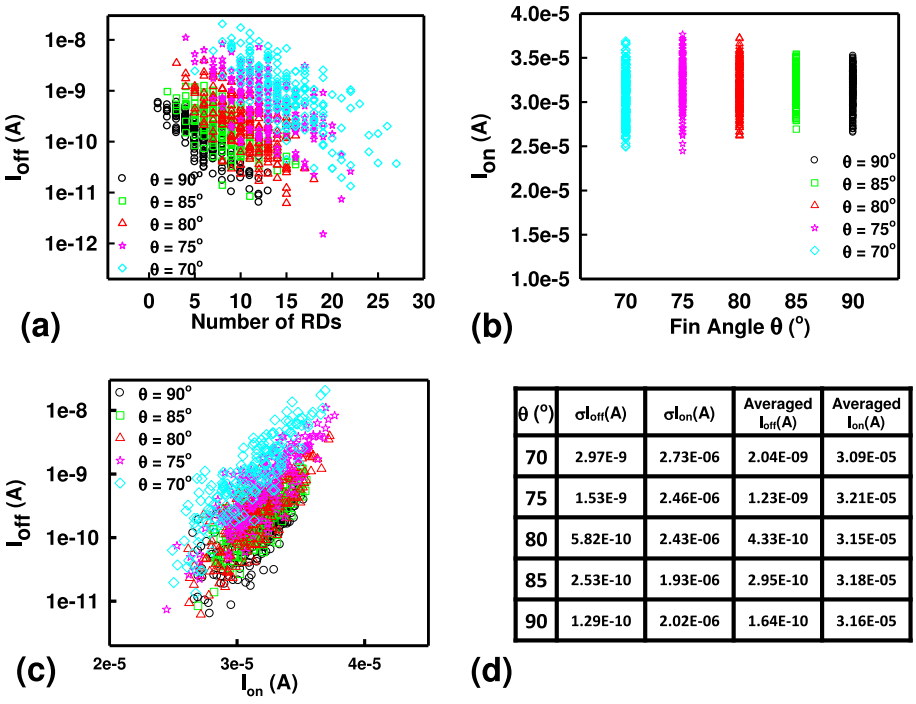


Figure 3 Plot of calibrated I_D-V_G curves. The red solid line is the I_D-V_G of simulation result, and the triangular symbols are experimental data. The inset shows the TEM cross-section view of the fabricated and measured device.

Figure 2a shows the simulated bulk FinFET's structure and the cross-section of fin channel. Table 1 lists the simulation settings and the achieved DC-characteristic parameters of each trapezoidal FinFET. The W_{top}, bottom-fin width (W_{bottom}), and the total fin width (W_{total}), which is defined as $2 \times W_{sidewall} + W_{top}$, are also listed in Table 1. The value of W_{total} is getting larger when the fin angle is getting smaller, and it is related to on-state current. The effective work function ranges from 4.4 to 4.5 eV, which is used to adjust the value of V_{th}. The constant current method at 0.1 μA × W_{total}/L_g is used to extract the magnitude of V_{th}, and the absolute value of the nominal V_{th} of each different-fin-angle trapezoidal FinFET is 250 mV. For the comparison of RDF on trapezoidal bulk FinFETs, the simulation is based on the same V_{th}, where the adopted device parameters are listed in Table 1. Figure 2b,c shows the large-scale statistical simulation method of RDF on the channel region. For RDF simulation, many discrete dopants dependent on the geometry are randomly generated in a large cube, where the dopant concentration in the large cuboid is equivalent to a channel doping concentration of 1.5×10^{18} cm^{-3}. Then, the large cube is partitioned into many subcubes, where the distribution of RDs' number follows Gaussian distribution, as shown in the right plot of Figure 2c. Then, a transformation of coordinate is performed on those subcubes to make them become trapezoidal-shaped channels and map them into 3D device channel regions. Notably, each coordinate of RDs is also transformed so that they appear in the trapezoidal-shaped channel exactly. To investigate the devices' characteristics, a set of 3D drift-diffusion equations coupled with the density gradient equation for quantum correction is solved [13,14]. The mobility model used in the device simulation mainly follows our earlier work [15] which involves surface roughness, high-field saturation, and impurity scattering. Notably, the mobility model activated in our device simulation considers the influence of surface orientations on the on-state current by the term of effective electric field for every fin angle [16]. The mobility model is quantified with our recent device measurements for the best accuracy of simulation, and the characteristic fluctuation has been validated with the experimentally measured DC base band data from 15/20 CMOS devices [15]. For each statistical device simulation, 216 RD-fluctuated FinFET devices are randomly generated for every fin angle to estimate the magnitude of the RDF-induced characteristic fluctuation.



θ (°)	σI_{off}(A)	σI_{on}(A)	Averaged I_{off}(A)	Averaged I_{on}(A)
70	2.97E-9	2.73E-06	2.04E-09	3.09E-05
75	1.53E-9	2.46E-06	1.23E-09	3.21E-05
80	5.82E-10	2.43E-06	4.33E-10	3.15E-05
85	2.53E-10	1.93E-06	2.95E-10	3.18E-05
90	1.29E-10	2.02E-06	1.64E-10	3.16E-05

Figure 4 Plots of I_{off} versus I_{on} and values of σI_{off}, σI_{on}, averaged I_{off}, and averaged I_{on}. (a) The *I*off versus RDs' number plot. **(b)** The I_{on} versus RDs' number plot. **(c)** The on/off current characteristic plot. **(d)** The value of σI_{off}, σI_{on}, averaged I_{off}, and averaged I_{on} of trapezoidal FinFET device with different fin angles.

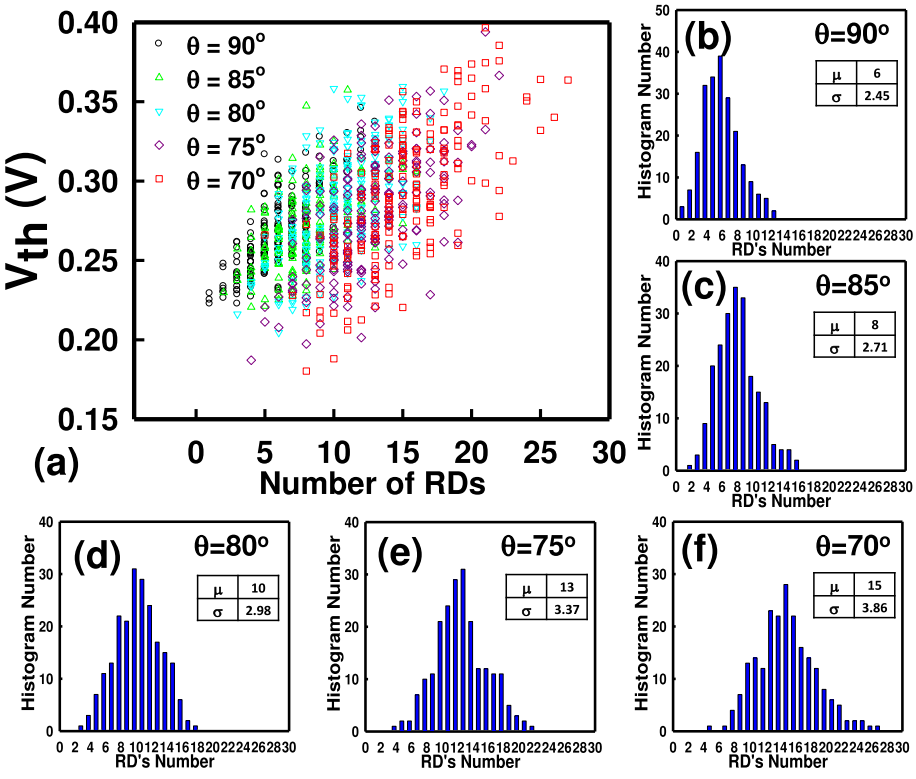


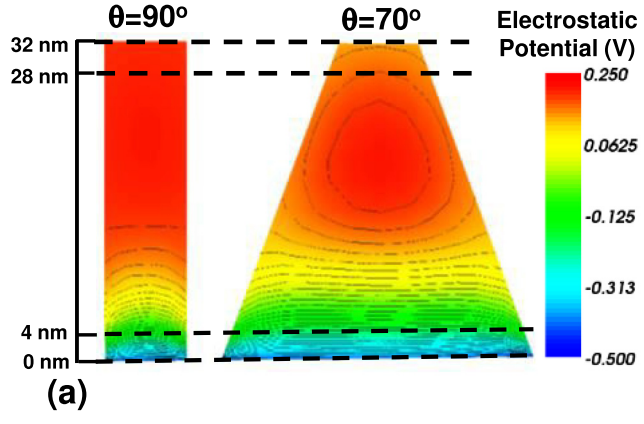
Figure 5 Plot of V_{th} versus the number of RDs and the RDs' number distribution. (a) The *V*th versus the number of RDs. **(b) to (f)** RDs' number distribution for every fin angle, where the μ is the mean and σ is the fluctuation.

Results and discussion

The inset of Figure 3 shows a TEM cross-section view of fabricated 16 nm n-type bulk FinFET device (gate length $L_g = 16$ nm) with amorphous-based TiN/HfSiON gate stacks with an EOT of 1.0 nm. The channel fin width is 16 nm, and the fin height is 32 nm. To ensure the best accuracy of device simulation, the I_D-V_G curve of the FinFET at $V_D = 0.8$ V is experimentally calibrated with measured data (symbols), as shown in Figure 3, where the extracted physical and process parameters are used for the following study.

Figure 4 shows the on-/off-state current characteristics of the trapezoidal bulk FinFETs with the fixed W_{top}. The plot of I_{off} versus RDs' number is shown in Figure 4a. The magnitude of I_{off} of rectangle-shaped bulk FinFETs is small, and 70° bulk FinFET has large I_{off} . In addition, the distribution of I_{off} is getting more dispersive when the fin angle is getting smaller. Under the same W_{top}, the phenomena are as a result of the weak lateral gate control of large bottom-fin width (i.e., small fin angle). The plot of I_{on} versus RDs' number is shown in Figure 4b. Though the W_{total} of 70° bulk FinFET is large, the on-state should be the largest of all. However, in rectangle-shaped bulk FinFETs, the fin width is narrow enough to induce strong volume inversion, where the electron mobility is enhanced due to less surface roughness. Therefore, the on-state current is comparable in the rectangle-shape bulk FinFET with the 70° bulk FinFET. Figure 4c shows the plot of I_{off} versus I_{on}. The FinFET with large fin angle has better on-/off-state current ratio and wider distribution of on-/off-state current than that of the FinFET with relatively smaller fin angles.

Figure 5 shows the plot of the V_{th} versus the number of RDs and the RDs' number distribution for every fin angle. We note that each RD has the same size and concentration; therefore, the bulk FinFET with a small fin angle needs more amount of RDs' number to achieve the same channel concentration due to large channel volume. As shown in Figure 5a, the trend of V_{th} fluctuation is dominated by RDs' number distributions, as shown in Figure 5b,c,d,e,f. The bulk FinFET whose fin angle is right angle has the smallest σV_{th}. It has been known that the calculation of σV_{th} follows the equation [17]:



θ (°)	H (nm)	Barrier (eV) -continuous doping	Barrier (eV) -Discrete dopants	Barrier Difference (eV)	Variation percentage (%)
70	28	0.295	0.410	0.115	39
	4	0.558	0.767	0.209	37
90	28	0.284	0.418	0.134	32
	4	0.554	0.710	0.154	28.29

(c)

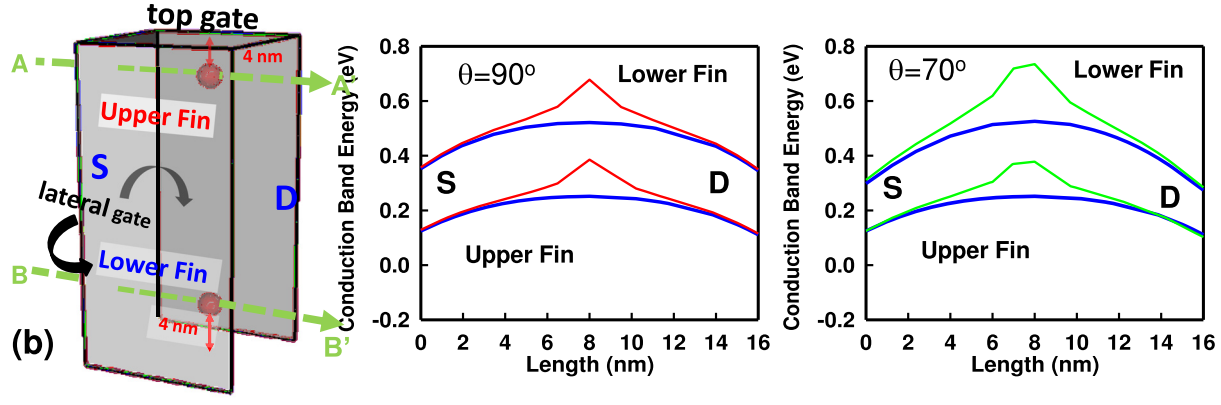


Figure 6 Off-state potential distribution of FinFET device and influence of one dopant on conduction band energy. (a) The off-state potential distribution of FinFET device with the right angle and 70° fin angle. **(b)** The influence of one dopant on upper-fin and lower-fin conduction band energy of FinFET device with the right angle and 70° fin angle. **(c)** The related value in **(b)**, which can indicate the influence of dopant is dependent on the position and the fin angle and the ability of inducing inversion charge is not the same everywhere of gate.

$$\sigma V\mathrm{th,\,RDF} = \frac{A_{\mathrm{VT}}}{\sqrt{W \times L_{\mathrm{g}}}}, \tag{1}$$

where A_{VT} is the factor which is governed by manufacturing process and semiconductor material, W stands for the device's width, and L_{g} is the gate length. The denominator is dependent on the dimension and structure of devices. If we simply consider W as the effective channel width, which is defined by $2 \times H_{\mathrm{f}} + W_{\mathrm{top}}$ for the rectangular-shape FinFET (or $2 \times W_{\mathrm{sidewall}} + W_{\mathrm{top}}$ for various trapezoidal FinFETs), it cannot be used to explain our results of Figure 5a. It is because the estimation of Equation 1 is originally derived from planar MOSFETs, based on an assumption of the ability on inducing inversion charge is the same for whole gate region.

For FinFET devices, the ability of 3D vertical channel structure on inducing inversion charge is not the same due to the different coupling strengths of the top gate and the lateral gates. This phenomena could also be observed by examining the off-state ($V_{\mathrm{G}} = 0$ V) potential distribution, as shown in Figure 6a, where the high potential region is easy to induce charge and the low potential region in the lower fin would block off most transport electrons. As shown in plots of Figure 6b, if we slice the channel fin of bulk FinFET device (the left plot is for an ideal structure) along the lines in green, the conduction band energies of continuous-doping device and discrete-dopant device (we assume there is 1 RD on upper/lower fin in this case, respectively) at upper/lower fin are obtained, respectively. The same way is also applied on the 70° trapezoidal FinFET. The right two plots of Figure 6b indicate the off-state potential energies, and their fluctuated barriers are rather different not only for RDs appearing in different fin regions but also for devices with different fin angles.

Consequently, the influence of RDs on device's subthreshold region is strongly dependent on the RDs' position, the shape of channel, and the fin angle. Thus, the fin-angle-dependent ability on inducing inversion charge is indeed not the same for the entire gate region. Therefore, the argument of W_{top} is not suitable to be regarded as the W in Equation 1. The effective W would be decreased with the fin angle getting smaller, and σV_{th} will be increased. The dopant variation induced V_{th} fluctuation is significant when the fin angle is small due to the less gate control. Therefore, based on the simulation results of Figures 4 and 5, in particular, from the analysis of RD's position effect, we further propose an analytical expression to phenomenologically correct Equation 1:

$$\sigma V\mathrm{th} = \frac{A'_{\mathrm{VT}} \times \left[\left(a \times e^{-b\times\theta}\right) \times N_{\mathrm{ch}}\right]^{0.25}}{\left(W_{\mathrm{total}} \times L_{g}\right)^{0.25}}, \tag{2}$$

where the fitting coefficients $a = 5.5 \times 10^5$ and $b = 0.12$.

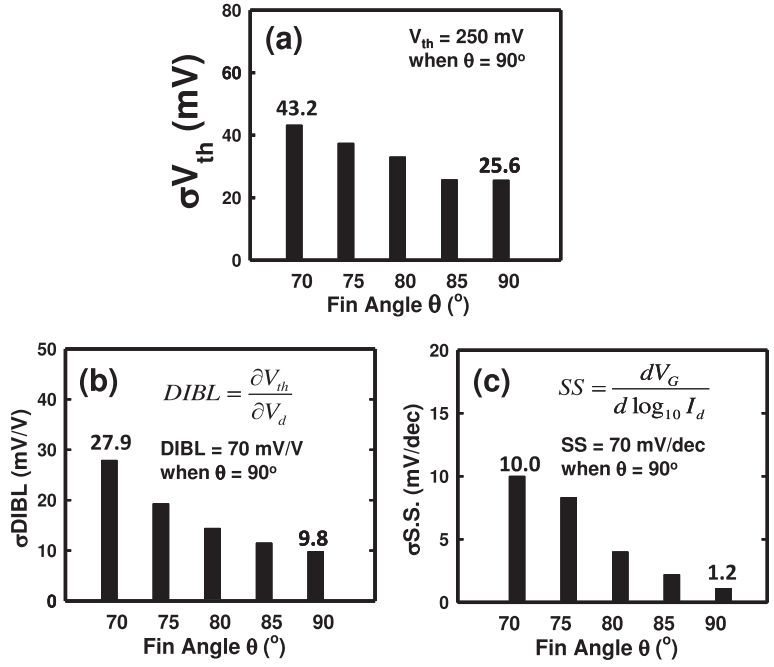


Figure 7 RDF stimulation result and magnitudes of σV_{th}, σDIBL, and σSS. (a) The RDF simulation result of bulk FinFET devices with respect to different fin angles. The magnitude of σV_{th} is getting larger when the fin angle is getting smaller. **(b)** The magnitude of σDIBL versus the fin angle. The magnitude of σDIBL increases when the fin angle decreases owing to the wider bottom-fin width. **(c)** The magnitude of σSS versus the fin angle.

The A'_{VT} is a technologically dependent parameter except the channel dopant concentration and N_{ch} is the channel doping concentration and θ is the fin angle which ranges from 70° to 90°. Notably, the denominator is dependent on the dimension and structure of devices and the factor 0.25 is mainly determined from the device structure which is different from the value of 0.5 used for planar MOSFET devices [18]. Two significant factors could be distinguished from this formula: one is the so-called structural effect as a result of the W_{total} under the fixed gate length, and the other is related to the RDs' position effect. The relationship between the effective channel dopants and the magnitude of the fin angle follows the trend of exponential decay. The influence of the fin angle dependent effective channel dopants dominates V_{th} fluctuation as the result of the small variation on the magnitude of W_{total} from variation of the fin angles. Not shown here, our model prediction is within 3% of accuracy, compared with the results in Figure 7a.

As shown in Figure 7, we estimate the fluctuations of the threshold voltage, the drain-induced barrier lowering (DIBL), and the subthreshold swing (SS) with respect to the fin angle. Consequently, as shown in Figure 7a, the V_{th} fluctuation decreases when the fin angle increases for the trapezoidal bulk FinFET devices under the constant top-fin width. There is more than 7% increase on the V_{th} fluctuation when the fin angle varies from 90° to 70° $\left(\left(\frac{43.2-25.6}{250}\right) \times 100\% \approx 7\%\right)$, where the denominator is the nominal $V_{th} = 250$ mV when $\theta = 90°$. Figure 7b,c shows the plots of the fluctuations of DIBL (σDIBL) and SS (σSS) versus the fin angle, respectively. Both DIBL and SS fluctuations are getting significant when the fin angle is getting smaller. The relationship between DIBL as well as SS fluctuation and the fin angle corresponds with the V_{th} analysis. The bulk FinFETs with a small fin angle suffers serious σDIBL (about 25.9% increases) due to large fin width. The increase of σSS is about 12.6% when the fin angle varies from 90° to 70°.

Conclusions

RDF on trapezoidal bulk FinFET devices with the fixed W_{top} and different fin angles is studied by experimentally validated 3D device simulation. The bulk FinFET devices with large fin angle have small off-state current due to the strongest gate control. For the tested channel fin width of 8 nm, the on-state current of the 16-nm-gate HKMG bulk FinFET device is almost the same for all trapezoidal-shaped channels. Furthermore, V_{th}'s fluctuation is affected by RDs' number distribution under the same channel doping concentration and the right-angle bulk FinFET device has the smallest V_{th}'s fluctuation among all devices with nonideal channel fins. We note that Equation 1 should be subject to further investigation for the calculation of σV_{th} of bulk FinFET devices.

Definitely, an assumption that fixed the bottom-fin width and let the top-fin width be varied with the fin angle could be an interesting issue to be investigated in a future work. In addition, for bulk FinFET devices, a punch-through stopper is adopted for reducing the subthreshold leakage. The punch-through stopper may result in another RDF source owing to high substrate doping near the bottom channel. RDF simulation with including the impact of punch-through stopper could be subjected to further investigation, and it definitely will input more accurate estimation on the characteristic fluctuation.

Abbreviations

FinFET: fin-type field effect transistor; RDF: random dopant fluctuation; RD: random dopant; SCE: short-channel effect; V_{th}: threshold voltage; W_{top}: top-fin width; W_{bottom}: bottom-fin width.

Competing interests

The authors declare that they have no competing interests.

Authors' contributions

W-TH performed the numerical simulation and data analysis, and YL conducted the whole study including data analysis and manuscript preparation. All the authors read and approved the final manuscript.

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References

1. Mil'shtein S, Devarakonda L, Zanchi B, Palma J. 3D modeling of dual-gate FinFET. Nanoscale Res Lett. 2012;7:625.
2. Magnone P, Subramanian V, Parvais B, Mercha A, Pace C, Dehan M, et al. Gate voltage and geometry dependence of the series resistance and of the carrier mobility in FinFET devices. Microelectron Eng. 2008;85:1728–31.
3. Kuhn KJ, Avci U, Cappellani A, Giles MD, Haverty M, Kim S, et al. The ultimate CMOS device and beyond. In: Proceedings of the IEEE International Electron Devices Meeting: December 10–13, vol. 2012. San Francisco, CA: IEEE; 2012. p. 171–4.
4. Li Y, Hwang CH, Han MH. Simulation of characteristic variation in 16-nm-gate FinFET devices due to intrinsic parameter fluctuations. Nanotechnology. 2010;21:095203.
5. Matsukawa T, O'uchi S, Endo K, Ishikawa Y, Yamauchi H, Liu YX, et al. Comprehensive analysis of variability sources of FinFET characteristics. In: Proceedings of the IEEE Symposium on VLSI Technology: June 16–18, vol. 2009. Honolulu, HI: IEEE; 2009. p. 118–9.
6. Li Y, Hwang CH. Effect of fin angle on electrical characteristics of nanoscale round-top-gate bulk FinFETs. IEEE Trans Electron Devices. 2007;54:3426–9.
7. Li Y, Hwang CH. Discrete-dopant-induced characteristic fluctuations in 16 nm multiple-gate silicon-on-insulator devices. J Appl Phys. 2007;102:084509.
8. Nam H, Shin C. Study of high-κ/metal-gate work function variation in FinFET: the modified RGG concept. IEEE Electron Device Lett. 2013;34:1560–2.
9. Wang X, Cheng B, Brown A, Millar C, Kuang JB, Nassif S, et al. Impact of statistical variability and charge trapping on 14 nm SOI finFET SRAM cell stability. In: Proceedings of the IEEE European Solid-State Device Research Conference: September 16–20, vol. 2013. Bucharest, Romania: IEEE; 2013. p. 234–7.

10. Chen CH, Li Y, Chen CY, Chen YY, Hsu SC, Huang WT, et al. Mobility model extraction for surface roughness of SiGe along (110) and (100) orientations in HKMG bulk FinFET devices. Microelectron Eng. 2011;109:357–9.
11. Bohr M. The evolution of scaling from the homogeneous era to the heterogeneous era. In: Proceedings of the IEEE International Electron Devices Meeting: December 5–7. Washington, DC: IEEE; 2011. p. 1–6.
12. Leung G, Chui CO. Variability impact of random dopant fluctuation on nanoscale junctionless FinFETs. IEEE Electron Device Lett. 2012;33:767–9.
13. Li Y, Liu JL, Chao TS, Sze SM. A new parallel adaptive finite volume method for the numerical simulation of semiconductor devices. Comput Phys Commun. 2001;142:285–9.
14. Ancona MG. Density-gradient theory: a macroscopic approach to quantum confinement and tunneling in semiconductor devices. J Comp Elect. 2011;10:65–97.
15. Li Y, Yu SM, Hwang JR, Yang FL. Discrete dopant fluctuated 20 nm/15 nm-gate planar CMOS. IEEE Trans Electron Devices. 2008;55:1449–55.
16. Takagi S-I, Toriumi A, Iwase M, Tango H. On the universality of inversion layer mobility in Si MOSFET's: part II—effects of surface orientation. IEEE Trans Electron Devices. 1994;41:2363–8.
17. Takeuchi K, Nishida A, Hiramoto T. Random fluctuations in scaled MOS devices. In: Proceedings of the IEEE International Conference on Simulation of Semiconductor Processes and Devices: September 9–11, vol. 2009. San Diego, CA: IEEE; 2009. p. 1–7.
18. Li Y, Hwang C-H. Discrete-dopant-fluctuated threshold voltage roll-off in sub-16 nm bulk fin-type field effect transistors. Jpn J Appl Phys. 2008;47:2580–4.