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Characteristics of Gate-All-Around Junctionless Polysilicon Nanowire Transistors With Twin 20-nm Gates

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ABSTRACT A high performance gate-all-around (GAA) junctionless (JL) polycrystalline silicon nanowire (poly-Si NW) transistor with channel width of 12 nm, channel thickness of 45 nm, and gate length of 20 nm has been successfully demonstrated, based on a simplified double sidewall spacer process. Without suffering serious short-channel effects, the GAA JL poly-Si NW device exhibits excellent electrical characteristics, including a subthreshold swing of 105 mV/dec, a drain-induced barrier lowering of 83 mV/V, and a high $I_{\mathrm{on}}/I_{\mathrm{off}}$ current ratio of 7×10^8 ($V_G = 4$ V and $V_D = 1$ V). Such GAA JL poly-Si NW devices exhibit potential for low-power electronics and future 3-D IC applications.

INDEX TERMS Gate-all-around (GAA), poly-Si, junctionless (JL), nanowire (NW), sidewall spacer, transistor.

I. INTRODUCTION

Recently, junctionless (JL) field-effect transistors with the same doping concentration and doping type at channel and source/drain (S/D) regions have attracted many researchers due to their relatively simple process that can still provide potential to overcome the scaling issue resulting from dopant diffusion [1], [2]. The JL structure has also been proposed in polycrystalline silicon (poly-Si) transistors, including planar and multiple gate devices [3]–[6]. In order to fully deplete the channel by gate electrostatic field, the channel dimension needs to be scaled down close to 10 nm [1]. There are several reports of JL and inversion-mode (IM) transistors having very small nanowire (NW) channels made by interesting top-down approaches and I-line photolithography (365 nm) [5], [7], [8] without using expensive lithographic tools like ArF photolithography (193 nm) [9] or electron beam (E-beam) writer. However, most of these top-down approaches are complex and difficult to define the gate length, and the devices still possess large gate length ($L_G > 0.35$ μm). Therefore, poly-Si NW devices with sub-50 nm L_G usually require an e-beam lithography tool [10], [11]. Among those reporting these interesting top-down approaches, the sidewall spacer is a commonly used method to create a nanoscale hard mask for nanowire channel [8] and lightly-doped drain (LDD) structure [12]. Such a patterning technique can produce a feature size down to 7 nm, as well as uniformity superior to the e-beam lithography and trimming process [13]. In this letter, we present for the first time a sub-30 nm JL poly-Si transistor fabricated through a simplified double spacer patterning technique. These devices with feature size of channel (∼12 nm) and L_G (∼20 nm) were successful fabricated by a successive top-down approach and assisted by an i-line stepper. Such ultra-short channel GAA JL devices without suffering thermal budget limit and serious short-channel effects (SCEs). Such devices with a simple fabrication process are highly promising for low power and future 3-D IC applications.

II. DEVICE FABRICATION

Fig. 1 shows the key process flow of the GAA JL poly-Si NW devices utilizing a double simplified sidewall spacer technique. On the wafer, a 500-nm thick thermal oxide layer was first grown as starting substrate. Then an 80-nm thick amorphous silicon (α-Si) layer was deposited through low pressure chemical vapor deposition (LPCVD) [Fig. 1(a)]. Next, the α-Si layer was patterned into a mesa structure and

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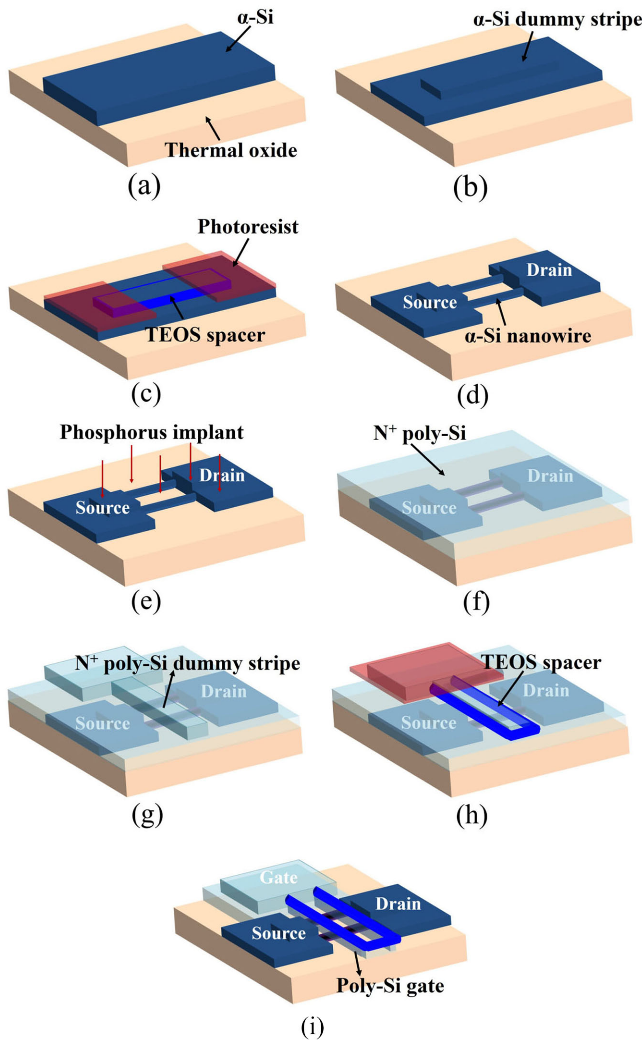

FIGURE 1. **(a)–(i) Key process flow of the GAA JL poly-Si device with double simplified sidewall spacer technique.**

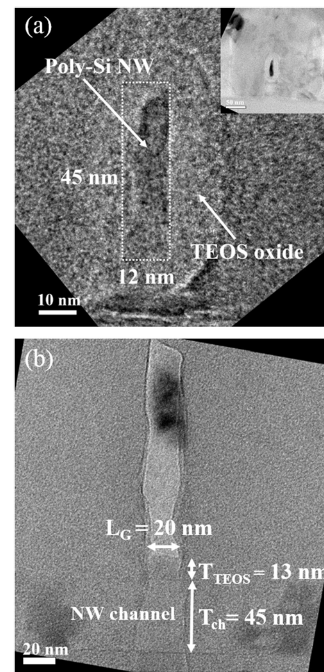

FIGURE 2. **(a) Cross-sectional TEM images of poly-Si NW surrounded by gate dielectric (TEOS oxide = 13 nm) and a poly-Si gate with channel width ∼12 nm and thickness ∼45 nm. (b) TEM image along the channel direction showing the physical gate length is ∼20 nm.**

etched by reactive ion etching (RIE). In this step, the α-Si layer was transformed into two parts, the thick part serving as a dummy stripe while the thinner serves as the device active layer [Fig. 1(b)]. A 60-nm thick tetraethyl orthosilicate (TEOS) oxide layer was deposited by LPCVD, and etched through RIE to leave sidewall hard masks. Before NW formation, the S/D were patterned by an i-line stepper [Fig. 1(c)]. Next, the α-Si NWs were formed through TEOS hard masks by high-selective RIE, and the TEOS hard masks were removed by diluted HF solution (1:50) [Fig. 1(d)]. After NWs formation, the phosphorus implantation was performed at a dose of 5×10^{13} cm^{-2} (13 keV) [Fig. 1(e)], and the solid-phase-crystallization (SPC) was performed at 600 °C for 24 h in N_2 ambient to turn the α-Si into polycrystalline silicon. The poly-Si NWs were suspended during standard RCA cleaning. Then a 13-nm thick TEOS oxide gate dielectric layer and a 150-nm in-situ N^+ doped poly-Si gate were deposited using LPCVD [Fig. 1(f)]. Next, the poly-Si gate was patterned and a part was etched to serve as a dummy stripe [Fig. 1(g)]. The 60-nm TEOS oxide layer was then deposited by LPCVD, and the sidewall hard mask was formed again by RIE. Before poly-Si gate formation, the gate electrode was patterned by an i-line stepper [Fig. 1(h)]. Next, the doped poly-Si layer was etched by high-selective RIE, and the poly-Si gate was formed through TEOS oxide hard mask [Fig. 1(i)]. After poly-Si gate formation, the TEOS hard mask was left and combined with the passivation layer deposited in the following step. Next, a 300-nm thick TEOS oxide layer was deposited as a passivation layer using LPCVD. Finally, Al metallization was sintered at 400 °C in nitrogen ambient for 30 min. In the fabrication process, the poly-Si NW channels and the gates were both obtained through the simplified sidewall spacer process.

III. RESULTS AND DISCUSSION

Fig. 2 presents the cross-sectional TEM images of the GAA JL poly-Si NW transistor device along the gate and the channel directions. Fig. 2(a) presents the cross-sectional TEM image of the poly-Si NW channel, with the upper inset showing a full view of the poly-Si NW channel surrounded by a gate dielectric layer (TEOS oxide = 13 nm) and a 120-nm poly-Si gate. The channel width and the thickness are ∼12 nm and ∼45 nm, respectively. Fig. 2(b) shows the cross-sectional TEM image along the channel direction. The physical gate length of GAA JL poly-Si NW device is ∼20 nm, and the thickness of gate dielectric and the thickness of NW channel correspond to those shown in Fig. 2(a).

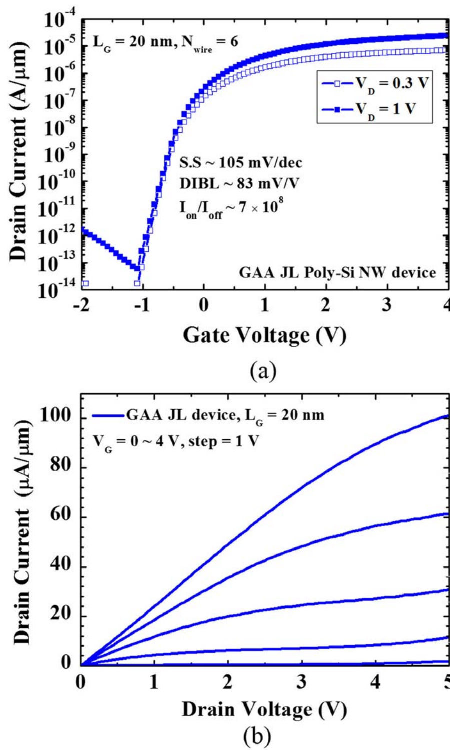

FIGURE 3. (a) Transfer characteristics and (b) output characteristics of the GAA spacer-JL poly-Si transistor.

The sidewall undercut of poly-Si gate at bottom region during RIE was observed as shown in Fig. 2(b). This was resulted from when etch front reaches the interface of gate dielectric layer and poly-Si gate, the conductive current path was broken and led to the charge separation. The positive ions tend to accumulate at the bottom and then attract reactant ions. As a result, it led to the side etching and undermined the sidewall profile of poly-Si gate [14], [15]. In addition, this effect becomes more evident as etching time increases. The sidewall roughness can be minimized by reducing the overetch time.

Fig. 3(a) presents the transfer characteristics of the GAA JL poly-Si NW devices ($L_G = 20 \times 2$ nm, $W_{eff} = 0.684$ μm, $N_{wire} = 6$). A small threshold voltage value of -0.26 V was obtained (at $I_D = (W_{eff}/L) \times 10^{-9}$ A and $V_D = 0.3$ V). In addition, the devices also present excellent characteristics, with a small subthreshold swing (SS) value of ~105 mV/dec at $V_D = 0.3$ V, a high I_{ON}/I_{OFF} current ratio of $\sim 7 \times 10^8$ (at $V_G = 4$V, $V_D = 1$ V), and a reasonable DIBL value of ~83 mV/V (extracted from DV_{gs}/DV_{ds} of $V_D = 0.3$ V and 1 V at $I_D = 1 \times 10^{-8}$ A). Although the channel depletion region was very narrow under the gate, the GAA structure combined with very small NW channel of ~12 nm × 45 nm still shows good gate controllability. The electrical characteristics can be further improved by thinning the gate oxide or providing an NH_3 plasma treatment [11]. Fig. 3(b) shows the I_D-V_D curves of the GAA JL poly-Si NW device. The result shows that a high output current

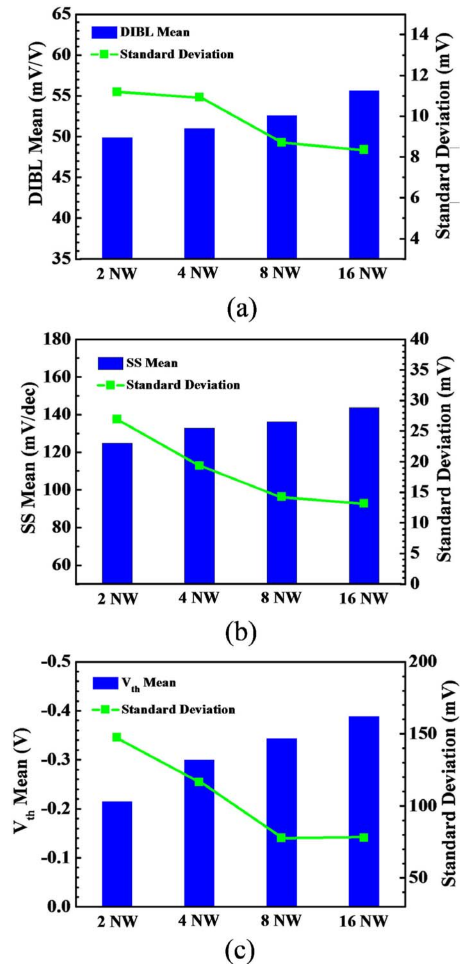

FIGURE 4. Device variability of 20-nm JL NW devices. Mean value and standard deviation of (a) DIBL, (b) SS, and (C) V_{th} for JL NW devices with various channel number.

was obtained. The output current can be further improved via a reduction of the length of NW (~350 nm) between the two poly-Si gates such that the series resistance is reduced. The kink effect occurred at low V_G and high V_D in the output characteristics is attributed to impact ionization at drain/channel region caused by the high longitudinal E-field and the grain boundary traps [16]. Fig. 4 presents the variability of electrical characteristics of 20-nm JL NW devices with different channel numbers. The statistics was extracted from 36 devices (9 devices for each JL NW transistor containing different channel numbers). Fig. 4(a)–(c) present both the mean values and the standard deviations of DIBL, SS and V_{th}, respectively. The standard variation of electrical characteristics of 20-nm JL NW devices is enhanced through the increase of the number of NW channel. However, with an increase of channel number from 2 to 16, the mean value of DIBL increases from 49.8 to 55.6 mV/V, SS increases from 124.4 to 143.8 mV/dec, and V_{th} rolls off from -0.215 to -0.388 V. The non-uniform gate length resulting from the undercut of poly-Si gate is likely to form especially in multiple-channel structure

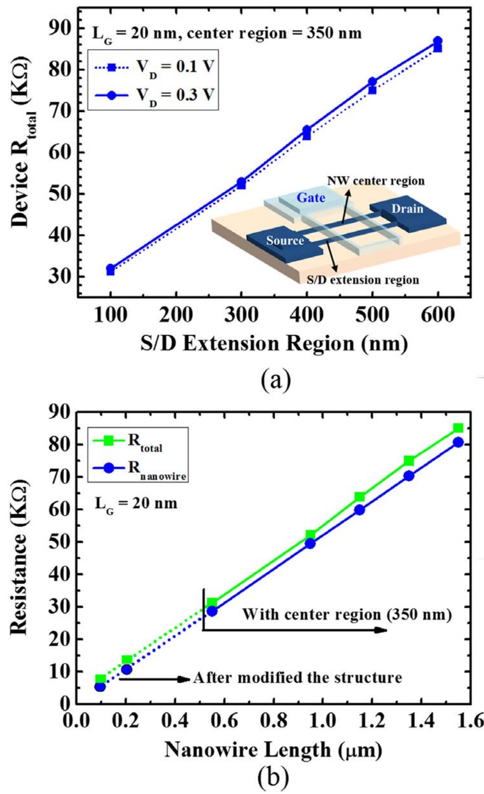

FIGURE 5. **(a) Total resistance of JL devices with different S/D extension region. (b) R_{NW} and R_{total} for various NW lengths.**

during RIE. Therefore, SCEs becomes evident as the number of NW channel increases. However, the multiple-channel NW structure provides advantage in minimizing the standard deviations of electrical properties.

In this study, the NW structure of JL NW poly-Si device contains two S/D extensions and a 350-nm center region as shown in the inset of Fig. 5(a). The junctionless device functions as a gated resistor. The additional series parasitic resistance can undermine the output characteristics. Fig. 5(a) shows the total resistance (R_{total}) of a 20-nm JL device (include the contact resistance). The R_{total} values were extracted from saturation region at $V_G = 5$ V, and $V_D = 0.1$ V and 0.3 V. The R_{total} increases linearly with respect to the length of S/D extension. Fig. 5(b) shows the resistances of GAA JL devices with different lengths of NWs. The NW resistance (R_{NW}) was estimated from the difference of resistance between devices with different S/D extensions at $V_G = 5$ V and $V_D = 0.1$ V. The R_{total} and the resistance of 100-nm S/D extensions are 31 KΩ and 10 KΩ, respectively. The total resistance exhibits a slight rise in devices with longer NW presumably because of more defects and grain boundaries were introduced in the channel. Although, S/D extensions and center region (17.5 KΩ) led to the additional parasitic resistance, the device resistance can be minimized by removal of one side of TEOS spacer and therefore the central region, and by shortening the S/D extensions via a modified fabrication process

TABLE 1. **Comparison of key characteristics of recently reported poly-Si JL devices.**

Source	This work	[3]	[4]	[5]	[6]
Gate structure	GAA	Planar	Tri-gated	GAA	GAA
Channel dimension (nm^2)	12×45	10μm×10	93×11	12×23	2×70
Gate length (μm)	0.02×2	5	0.09	1	1
EOT (nm)	13	10	11	15	17
S.S. (mV/dec)	105	240	285	199	61
DIBL (mV/V)	83	N/A	420	N/A	6
I_{ON}/I_{OFF} V_G; V_D	>10^8 4V;1V	>10^7 3V;1V	>10^7 4V;0.1V	>10^6 5V; 2V	>10^7 3V;0.5V

(process not shown). After the removal of the central region and shortening of the S/D extensions, the total length of NW can be scaled down to 100 nm ~200 nm, and the R_{total} can be pushed down to 8.5 KΩ ~13.5 KΩ as shown in Fig. 4(b). Table 1 shows the key parameters of poly-Si JL transistors recently reported through different top-down approaches. In this paper, we present a sub-30 nm JL poly-Si transistor fabricated through a simplified double spacer patterning technique and the traditional I-line photolithography. Moreover, both nanowire channel and gate length were for the first time prepared via the same technique. Although some other reports presented different top-down fabrication approaches to obtain very small poly-Si NW channel [5], [7], [8], these techniques are either too complex or too difficult to define the gate length. Therefore, the gate lengths of reported devices were usually above 0.35 μm. Compared with other long-channel devices ($L_G > 0.35$ μm) listed in Table 1, device prepared in this study show higher current ratio (close to 10^9 at $V_G = 4$ V; $V_D = 1$V) and smaller SS (close to 100 mV/dec) as a result of the reduction of the defects and leakage path under the gate. In addition, compared with other reported short-channel devices ($L_G < 100$ nm) [4], [11], our devices exhibit limited SCEs (DIBL ~83 mV/V), and present excellent gate controllability presumably because of a smaller NW channel dimension and a thinner gate dielectric. This GAA JL poly-Si NW device presents excellent electric characteristics without suffering serious SCEs exhibit potential for low-power device and future 3-D IC applications.

IV. CONCLUSION

We characterized for the first time GAA JL poly-Si NW transistors with twin 20-nm gates prepared by a double sidewall spacer patterning technique. The channel width and channel thickness of the GAA JL poly-Si NW devices were 12 nm and 45 nm, respectively. The combination of a very small channel and the GAA structure produces devices which suffer no serious SCEs and which show excellent characteristics

with small S.S. (~105 mV/dec), DIBL (~83 mV/V), and a high I_{ON}/I_{OFF} (~7×10^8) current ratio.

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