Received 18 August 2015; revised 15 October 2015, 23 November 2015, and 23 December 2015; accepted 28 December 2015. Date of publication 31 December 2015; date of current version 23 February 2016. The review of this paper was arranged by Editor M. Östling.

Digital Object Identifier 10.1109/JEDS.2015.2514060

Suppressing Non-Uniform Tunneling in InAs/GaSb TFET With Dual-Metal Gate

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This work was supported in part by ATMI/Entegris, in part by Applied Materials, in part by the NCTU-UCB

I-RiCE Program, Ministry of Science and Technology, Taiwan, under Grant MOST-105-2911-I-009-301.

ABSTRACT Non-uniformity in electric field causes early onset of tunneling near the edge of InAs/GaSb hetero-junction tunneling field-effect transistors. When a small area, often an edge, of the tunneling junction has a lower turn-on voltage, the steep switching characteristic is degraded. Fermi pinning at InAs surface greatly worsen the uniformity. We propose a dual-metal gate structure to address the non-uniformity issue. With proper choice of work functions, the dual-metal gate structure can effectively suppress the early onset of edge tunneling and significantly improve the subthreshold swing.

INDEX TERMS InAs/GaSb, tunneling FET (TFET), quantum well, surface states, Fermi pinning, non-uniformity, dual-metal gate, steep turn-on.

I. INTRODUCTION

CMOS voltage reduction has become increasingly difficult. The 60 mV/dec limitation of MOSFET subthreshold swing is a huge stumbling stone for VLSI voltage and power reductions. TFET is a promising candidate for the green transistor that breaks this limitation [1]–[3]. For achieving high on-current, a lower tunneling barrier is essential. Type-II hetero-junction tunneling field-effect transistors (TFETs) can be designed to have low tunneling barrier [4], [5]. InAs/AlGaSb TFET is well studied due to its small effective band gap [6]–[13]. However, InAs/AlGaSb TFETs mostly do not exhibit steep characteristics experimentally. We believe that one reason is the non-uniform onset of tunneling in the TFET structures.

InAs surface has an electron accumulation layer due to Fermi level pinning at surface states which is above the conduction band minimum (CBM) [14]. A surface under the InAs cantilever was exposed in the TFET after lateral etching as shown in Fig. 1(a) [15]. In this letter, we reveal that Fermi pinning of the exposed InAs surface enhance tunneling non-uniformity and degrade subthreshold swing. Then we propose using the dual-metal gate structure to suppress the early onset of tunneling near the junction edge and greatly improve subthreshold swing.

Sentaurus TCAD simulation tool is employed in this investigation. It should be noted that the semi-classical band-to-band tunneling model in Sentaurus lead to overestimation of tunneling device performance due to neglecting phonon scattering and other assumptions. Therefore, the on-state current and the subthreshold slope aren't emphasized in this article. The emphasis is the modification of electrostatic potential with the dual-metal TFET configuration. Sentaurus simulator is well suited for electrostatic simulation.

II. DEVICE SIMULATION AND EFFECT OF FERMI PINNING

Fig. 1(a) shows the structure of an InAs/GaSb TFET. The band diagram along the cutline A is shown in Fig. 1(b). There is a 5 nm InAs quantum well upon bulk GaSb, and ZrO_2 (ε_r= 23.2) is used as the gate oxide. The first sub-band in 5 nm InAs quantum well was calculated by solving the one-dimensional Schrödinger equation with the effective mass method by the Nextnano simulator. First sub-band is higher than the valence band maximum (VBM) of GaSb by

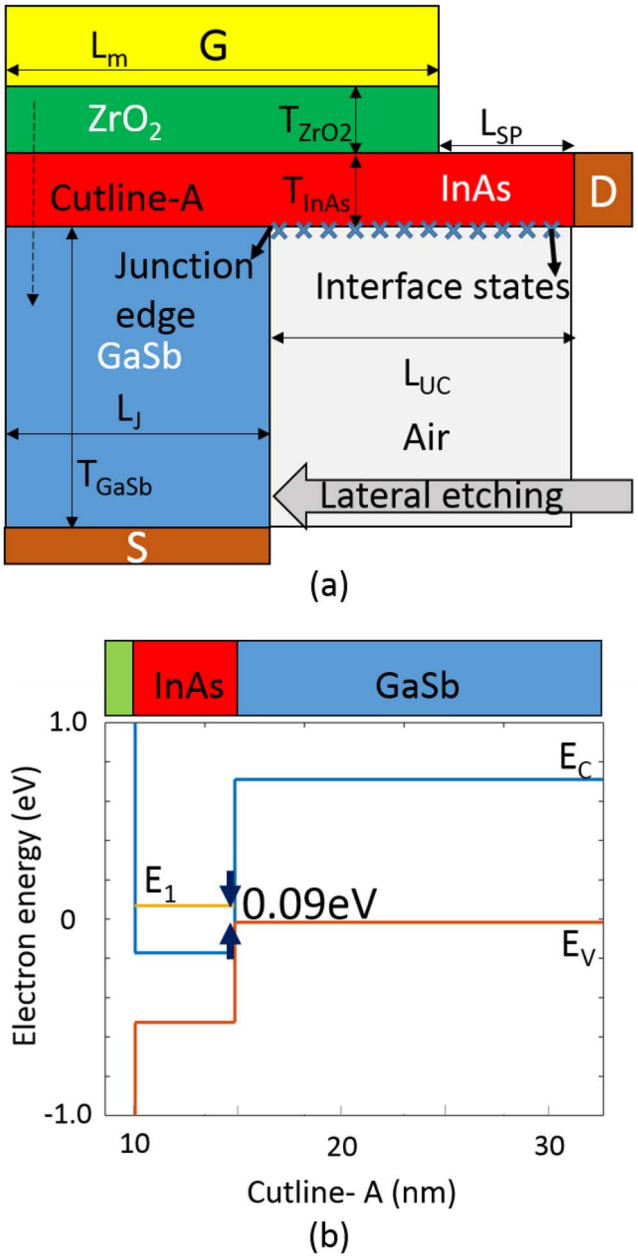

FIGURE 1. (a) Simulated device structure: $L_G = 70$ nm, $L_{SP} = 50$ nm, undercut $L_{UC} = 70$ nm, junction width $L_J = 50$ nm, ZrO_2 thickness $T_{ZrO2} = 10$ nm, InAs thickness $T_{InAs} = 5$ nm, GaSb thickness $T_{GaSb} = 100$ nm, n-type doping concentration in InAs $N_D = 1 \times 10^{17}$ cm^{-3}, p-type doping concentration in GaSb $N_A = 1 \times 10^{19}$ cm^{-3}, work function of gate metal is 4.9 eV (b) Band diagram along cutline A in Fig. 1(a). E_1 is the ground state of the quantum well.

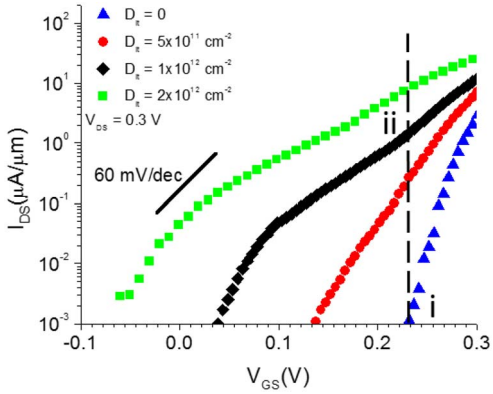

FIGURE 2. I_{DS}–V_{GS} characteristics for different D_{it}.

TABLE 1. Summary of average subthreshold swing for different surface state densities.

Desity of surface states D_{it} (cm^{-3})	SS_{avg} (mV/dec)	I_{60} (μA/μm)
0	17	16.3
5×10^{11}	40	15.6
1×10^{12}	60	4.8×10^{-2}
2×10^{12}	65	3.8×10^{-2}

0.09 eV, making this a type-II hetero-junction. The effective mass method is a simplified model. The wave vector penetration isn't considered in the method, which results an overestimation of the band offset. However, the conclusion of this article, in which useful modification of the electrostatic potential with a dual metal structure, is not clouded by these simplifications. This first sub-band energy was entered into the Sentaurus TCAD simulator as CBM of InAs, making the modified band-gap energy of InAs 0.55 eV. In the TCAD simulation, WKB-based dynamic nonlocal path band-to-band tunneling model was enabled to simulate tunneling [16], [17]. The surface states were added to the interface between InAs and air. According to the literature, the surface states are 0.78 eV above the VBM of InAs [18].

The surface states greatly influence the switching characteristics of the TFET as shown in Fig. 2 and Table 1. The average subthreshold swing SS_{avg} degrade by several hundred percent with increasing density of surface states (D_{it}). In this paper, SS_{avg} refers to average subthreshold swing between $I_{DS} = 10^{-3}$ μA/μm and $I_{DS} = 1$ μA/μm. I_{60} is defined as the current at which the device operation transits from sub-60 mV/dev to super-60 mV/dec [19]. The degradation of I_{60} is also observed with higher D_{it} as listed in Table 1.

Fig. 3 explains how Fermi pinning worsens the switching characteristic. Fig. 3(a) shows the band diagram of InAs along cutline B-B'. We observe that the surface states beneath the InAs cantilever drag the energy band downward at and beyond the GaSb edge. Fig. 3(b) plots the tunneling induced carrier generation rate contours for the $D_{it} = 0$ case (top figure) and the case of $D_{it} = 1 \times 10^{12}$ cm^{-2} (bottom figure). The contours show the electron generation rate in InAs and hole generation rate in GaSb. These plots are for $V_{GS} = 0.23$ V (the vertical line in Fig. 2). The bottom figure shows that electrons tunnel out of the valence band (generating holes) from the upper left corner of GaSb diagonally into the conduction band (generating electrons) of the InAs film. Fermi pinning induced band lowering in Fig. 3(a) effectively lowered the onset voltage for tunneling in this diagonal direction. Therefore, tunneling occurs at this edge much earlier than the interior.

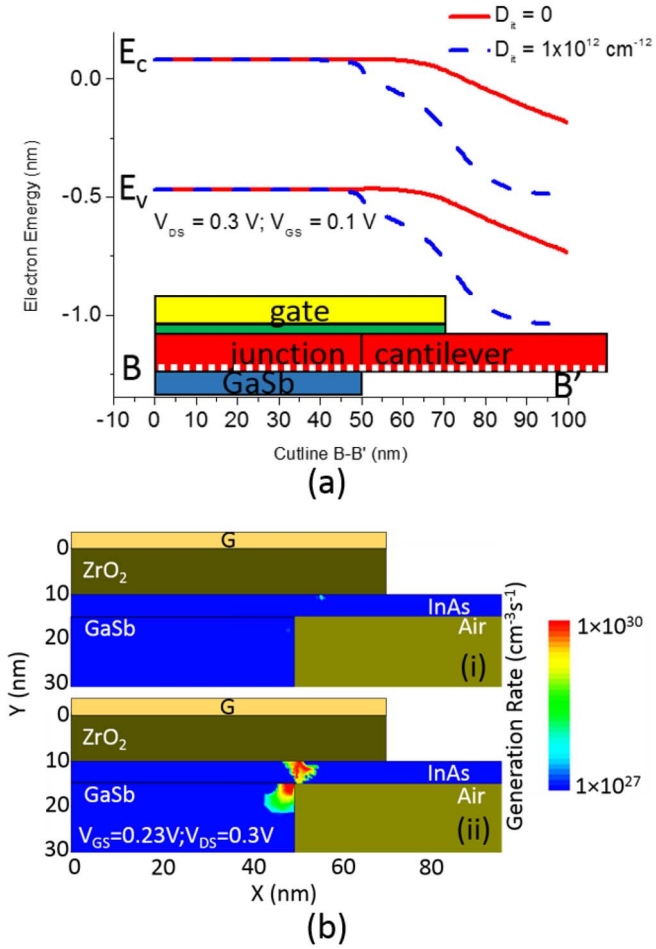

FIGURE 3. **(a) Band diagram along cutline B-B' in InAs layer, close to the bottom of InAs. (b) Contour plot of carriers generation rate due to tunneling for $D_{it} = 0$ (top) and $D_{it} = 1 \times 10^{12}$ cm^{-2} (bottom).**

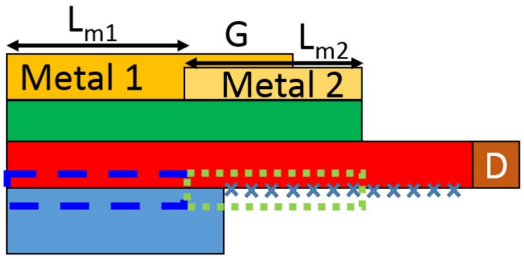

FIGURE 4. **Dual-metal gate TFET structure. In this simulation, the gate length of metal 1 (L_{m1}) is 38 nm and the gate length of metal 2 (L_{m2}) is 30 nm. The overlap of metal 2 over the junction is 10 nm.**

III. DUAL-METAL GATE FOR IMPROVED STEEP SWITCHING

The dual-metal gate structure depicted in Fig. 4 is proposed to suppress the early onset of tunneling at the edge of InAs/GaSb hetero-junction. Metal 1 with a lower work function is the main gate electrode that determines the tunneling onset voltage of the interior region (boxed by blue dash line). Metal 2 with a higher work function is introduced to raise the tunneling onset voltage of the edge region (boxed by light green dotted line). Metal 1 and metal 2 are simply electrically and physically connected to each other and share the same gate voltage. However, in the simulation, we separate the two gate metals by 2 nm to avoid non-convergence. We fix the work function for metal 2 (WF_{m2}) at 4.9 eV and the work function of metal 1 (WF_{m1}) is varied in simulation.

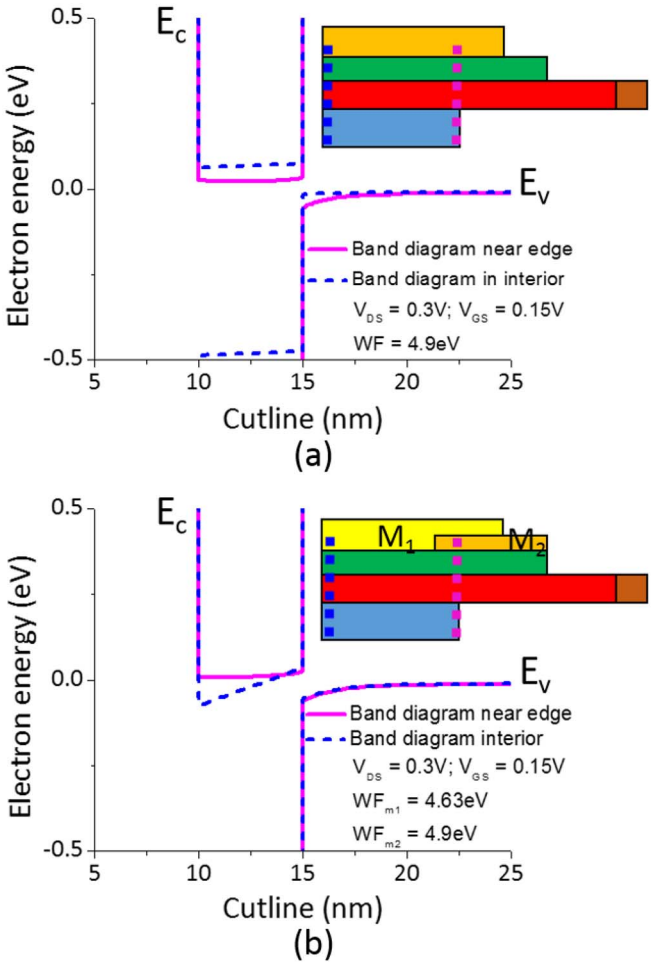

FIGURE 5. **Comparison of band diagrams in the interior (blue cutline) and at the edge (purple cutline) of (a) single metal gate and (b) dual-metal gate TFETs.**

The 10 nm overlap of metal 2 over the GaSb is a somewhat arbitrary estimation of the fabrication variability [15]. The key idea of this structure is to use a lower WF_{m1} to decrease the onset voltage of the large interior area of the junction so that the steep turn on of this large tunneling current is not degraded by the premature tunneling at the edge (under metal 2). Fig. 5 shows the band diagrams along cutlines in the interior and in the edge. Fig. 5(a) is the case of single metal gate. Clearly the edge is about to enter the tunneling regime (valence and conduction band states overlapping) while the interior is not. Fig. 5(b) is the case of dual-metal gate. The interior is well into the tunneling regime with large overlap of valence and conduction band states while the edge is not. In the dual-metal gate structure, the tunneling onset voltage in the interior should be chosen

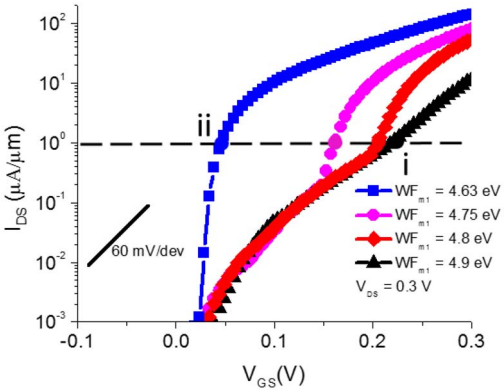

FIGURE 6. I_{DS}–V_{GS} curves with WF_{m1} varying from 4.9 eV to 4.63 eV.

TABLE 2. Summary of average subthreshold swing.

Work Function of Metal 1 WF_{m1} (eV)	SS_{avg} (mV/dec)	I_{60} (μA/μm)
4.9	60	4.8×10^{-2}
4.8	57	13
4.75	45	9.6
4.63	8	4.9

to be lower than the tunneling onset voltage in the edge region. Notice that the band-bending of GaSb (associated with the depletion width) near the tunneling region is very small. This type of feature has already been observed in other heterojunction TFETs [20]. The small band-bending of type-II heterojunction TFETs is different from the larger band-bending observed in homojunction TFETs [21]. The depletion region has been shown to have a strong impact on the performance of ultra-scaled TFETs.

Fig. 6 and Table 2 illustrate how I_{DS}–V_{GS} changes with WF_{m1}. The D_{it} is set as 1×10^{12} cm^{-2}. With decreasing WF_{m1} from 4.9 eV to 4.63 eV, the switching characteristic becomes more abrupt. The I_{DS}–V_{GS} curves in Fig. 6 can be recognized as having two parts. The larger subthreshold swing part is caused by tunneling near the edge region where a range of low onset voltages (depending on distance from the edge) exist. The wide range of lower onset voltage is caused by non-uniformity of band bending and electric field near the edge as shown in Fig. 3(a). As V_{GS} increases, more and more parts of the edge region contribute to tunneling and result in a slow rise of current. The smaller subthreshold swing part of the I_{DS}–V_{GS} curves is the tunneling current produced in the interior region, which has uniform potential and electric field (see Fig. 3(a)). The entire interior region turns on and off together and produces steep switching [22]. With $WF_{m1} = 4.63$ eV, the intrinsic switching characteristic can overwhelm the early edge tunneling. In that case, subthreshold swing is even lower than the 17 mV/dec for the case of $D_{it} = 0$ in Table 1. This illustrates that electrostatic non-uniformity exists at the edge even in the absence of surface states. The dual-metal gate solution is also effective to suppress unwanted early onset tunneling due to other causes of non-uniformity. One issue

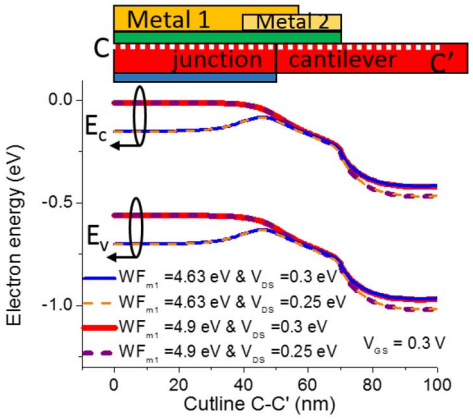

FIGURE 7. Band diagram of cutline C-C′ in InAs layer, close to the oxide/InAs interface.

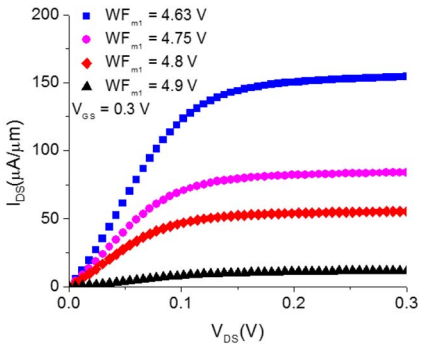

FIGURE 8. I_{DS}–V_{DS} curves with WF_{m1} varying from 4.9 eV to 4.63 eV.

needs to be reminded, the choosing of $WF_{m2} - WF_{m1}$ is quite restrictive. The available WF_{m1} window for subthreshold improvement is small ($\sim$ 0.1 eV, from 4.75 to 4.63 eV) as shown in Fig. 6. Hence the precise work function control is required for practical applications. The required precision may be achieved by considering, e.g., that the grain size of metal impacts the work function variation. Hence the amorphous metal gate may serve as a solution for precise control of work function [23].

Fig. 7 shows the presence of a barrier under metal 2. The induced barrier impedes electron conduction from the interior region to the drain. As a result, Table 2 shows that I_{60} can decrease with decreasing WF_{m1}. This stems from the higher barrier induced by larger $WF_{m2} - WF_{m1}$. On the other hand, even at $WF_{m1} = 4.63$ eV, I_{60} is still considered high [19] and I_{DS} in Fig. 6 is higher for this case than for the larger WF_{m1} values.

Fig. 8 shows the $I_{DS} - V_{DS}$ for several WF_{m1}. Under the same gate bias, $V_{GS} = 0.3$ V, the drain current is higher when WF_{m1} is reduced. While the potential barrier shown in Fig. 7 is undesirable and may be reduced or eliminated with further device optimization, its presence does not preclude I_{DS} improvement with the dual metal gate configuration. Fig. 7 further shows that the potential barrier height hardly changes when V_{DS} changes from 0.25 V to 0.3 V. This explains the good current saturation behavior in Fig. 8.

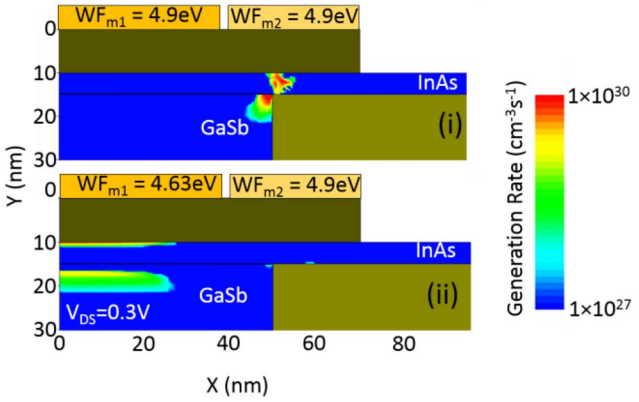

FIGURE 9. Carriers generation rate contour plots for $WF_{m1} = 4.9$ eV (top) and $WF_{m1} = 4.63$ eV (bottom) at i and ii in Fig. 6.

Fig. 9 shows the plots of electron and hole generation rates at the V_{GS} that produces $I_{DS} = 1$ μA/μm in each structure (i and ii in Fig. 6). It's clear that the tunneling current in the case of $WF_{m1} = 4.63$ eV, nearly all tunneling occurs in the interior and metal 2 effectively suppresses the edge tunneling. In the single metal structure, all the tunneling occurs at the edge.

IV. CONCLUSION

We report that the non-uniform tunneling onset voltage in the junction edge region of InAs/GaSb cantilever TFET leads to degradation of the switching steepness. Fermi level pinning worsens the degradation of subthreshold swing greatly. Dual-metal gate structure is proposed to suppress the early onset of local tunneling and avoid the loss of switching steepness due to this phenomenon. It is expected to be useful for mitigating subthreshold swing degradation caused by other structural non-uniformity.

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CHENMING HU (F'90) received the B.S. degree from National Taiwan University, and the M.S. and Ph.D. degrees from University of California, Berkeley, all in electrical engineering. He has been called the Father of 3-D Transistor for developing the FinFET in 1999. Intel is the first company to use FinFET in 2011 production calling it the most radical shift in semiconductor technology in over 40 years. He is a Professor with the Graduate School, University of California, Berkeley, the Board Director of SanDisk Corporation. From 2001 to 2004, he was the Chief Technology Officer of TSMC, world's largest dedicated integrated circuits manufacturing company.

Prof. Hu's field of research is semiconductor technology, transistor compact models BISM, FinFET, tunnel transistor, and NCFET. He was a recipient of the 2011 Distinguished Alumni Award.