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Evaluation of Monolithic 3-D Logic Circuits and 6T SRAMs With InGaAs-n/Ge-p Ultra-Thin-Body MOSFETs

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ABSTRACT This paper evaluates monolithic 3-D logic circuits and 6T SRAMs composed of InGaAs-n/Ge-p ultra-thin-body MOSFETs while considering interlayer coupling through TCAD mixed-mode model. This paper indicates that monolithic 3-D InGaAs/Ge logic circuits provide equal leakage and better delay performance compared with planar 2-D structure through optimized 3-D layout. The monolithic 3-D InGaAs/Ge 6T SRAMs can simultaneously improve the cell stability and performance through optimized 3-D layout. We suggest two 3-D SRAM layout designs for high performance and low power applications, respectively. Moreover, with optimized 3-D layout designs, InGaAs/Ge logic circuits exhibit larger delay improvement, and the 6T SRAMs exhibit larger read access time and time-to-write improvement compared with Si counterparts.

INDEX TERMS InGaAs/Ge, monolithic 3-D, logic circuits, SRAM, interlayer coupling.

I. INTRODUCTION

3D integration is crucial for improving chip density, reducing interconnect delay and enabling heterogeneous integration. Among various 3D technologies, monolithic 3D integration, which stacks multiple layers sequentially, exhibits better alignment accuracy compared with through-silicon via (TSV) technology [1]. The aspect ratio and diameter of TSV are limited by the via filling process. The ultra-fine via size of monolithic inter-tier vias leads to higher chip density and smaller parasitic resistance and capacitance compared with TSV technology [2]. Therefore, monolithic 3D integration is promising for high density integration such as logic circuits and SRAM cells. Monolithic 3D IC can be categorized into four levels in term of partitioning granularity [2]–[4]. Transistor-level design, which separates NMOSFETs and PMOSFETs into two tiers, is suggested for its advantages in footprint, wire length, timing and power [2].

Heterogeneous integration enables different materials and technologies to integrate onto Si substrate. High-mobility channel materials have garnered much attention for the potential to achieve high speed and low power operation. The electron mobilities of III-V materials and the hole mobility of Germanium can be several times larger than the Si counterparts [5], and the enhanced carrier transport properties enable higher current drive and lower supply voltage. Therefore, the combination of InGaAs-n/Ge-p is considered as a candidate to replace Si CMOS and further extend Moore's law. However, the fabrication process of heterogeneous integration of co-planar III-V and Ge MOSFETs is complex and difficult to achieve optimized NFETs and PFETs. Therefore, 3D heterogeneous integration of InGaAs and Ge MOSFETs has been proposed and demonstrated [6]–[8].

In this work, with the aid of TCAD mixed-mode simulations, we comprehensively evaluate monolithic 3D ultra-thin-body (UTB) InGaAs-n/Ge-p logic circuits and 6T SRAMs. The paper is organized as follows. Section II describes the monolithic 3D structure and device design used in this work. In Section III, we investigate and compare the leakage and delay performance of InGaAs/Ge inverter and

2-way NAND. In Section IV, the stability, cell leakage, and cell read/write performance of InGaAs/Ge 6T SRAM cells are investigated. In addition, two 3D SRAM layouts for high performance and low power applications are suggested, respectively. Finally, the conclusions are drawn in Section V.

II. MONOLITHIC 3-D STRUCTURE AND DEVICE DESIGN

For monolithic 3D structure, two-tier layer design, one for NMOSFET and the other for PMOSFET, is adopted and connected using dense nano-scale inter-tier vias (Fig. 1(a)). Using low-temperature processes, the bottom-tier device can preserve its characteristics after the fabrication of the upper-tier device [6]–[8]. Compared with monolithic 3D structure with thick interlayer dielectric (ILD), the thin ILD structure possesses better subthreshold swing and lower leakage due to its superior electrostatic integrity. Moreover, monolithic 3D structure with thin ILD shows the interlayer electrical coupling in transistor-level design [9]. The front-gate of the bottom-tier device can serve as the back-gate of the upper-tier device. Thus, exploiting interlayer coupling for back-gating offers another degree of design freedom without area penalty. In our analysis, 3D logic circuits and 6T SRAMs composed of InGaAs NMOSFET and Ge PMOSFET are investigated. Four possible scenarios with different channel materials (InGaAs/Ge and Si) and tier combinations ((Upper/Bottom) tier for (P/N) and (N/P) MOSFET) are shown in Fig. 1(b).

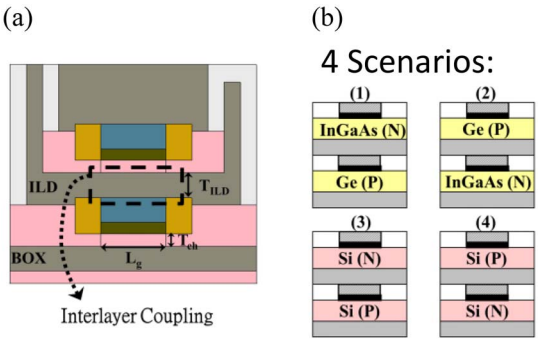


FIGURE 1. (a) Two-tier monolithic stacking showing the interlayer coupling between tiers, and (b) scenarios with different channel materials (InGaAs/Ge and Si) and various tier combinations evaluated in this work.

With interlayer coupling, the gate of bottom-tier transistor provides a dynamic or fixed back-gate bias (V_{bg}) of upper-tier device. For comparison, we use two back-gate biases ($V_{bg} = 0V$ and $V_{bg} = V_{DD}$ for NMOSFET and PMOSFET, respectively) for the base 2D circuits and the V_{bg} of the 3D bottom-tier devices. In other words, the MOSFETs of 2D circuits have zero body-to-source bias. It should be noted that the body-to-source bias of the upper-tier devices is either zero-biased or forward-biased.

In this work, TCAD mixed-mode simulations [10] are performed considering the interlayer coupling of monolithic 3D logic circuits and 6T SRAMs. The calibrated SOI and InGaAs-OI/GeOI UTB devices are designed with $L_g = W = 25nm$, $T_{ch} = 5nm$, EOT = 0.7nm,

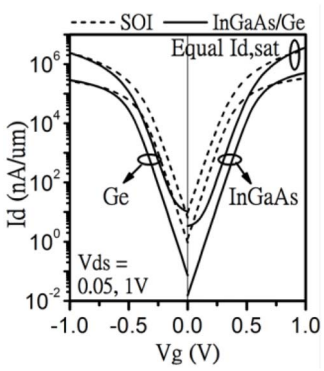


FIGURE 2. (a) Id-Vg characteristics of CMOS with different channel materials (InGaAs-n/Ge-p and Si-n/Si-p) designed under equal $I_{d,sat}$.

$T_{BOX} = T_{ILD} = 10nm$ with equal $I_{d,sat}$ [11], [12]. Fig. 2 shows that the InGaAs-OI MOSFET, with higher mobility, possesses the highest threshold voltage ($|V_T|$) whereas the SOI device has the lowest $|V_T|$. MOSFETs with higher $|V_T|$ exhibit larger back-gate bias efficiency, which refers to the I_d modulation with back-gate bias. Besides, the GeOI devices have the highest I_{off} (due to band-to-band tunneling leakage, I_{BTBT}) at high drain bias, while the SOI counterpart shows the highest I_{off} (due to subthreshold leakage) at low drain bias.

III. LEAKAGE-DELAY ANALYSIS OF LOGIC CIRCUITS

The leakage of inverter is dominated by the off-state MOSFET. Fig. 3(a) shows the leakage comparison of 2D Si/Si and InGaAs/Ge CMOS inverters versus V_{DD} with input signal at "High" and "Low" ("1" and "0"). It shows that InGaAs/Ge inverters exhibit smaller leakage compared with Si/Si counterparts for both inputs except for high V_{DD} with "1" input signal. The rising leakage of InGaAs/Ge inverter with increasing V_{DD} is due to the presence of I_{BTBT} at high drain bias. In Fig. 3(b), monolithic 3D inverters stacked in (P/N) and (N/P) tier are compared with the 2D counterparts. As can be seen, identical leakage is found for 2D and 3D inverters due to the identical V_{bg} configuration of the

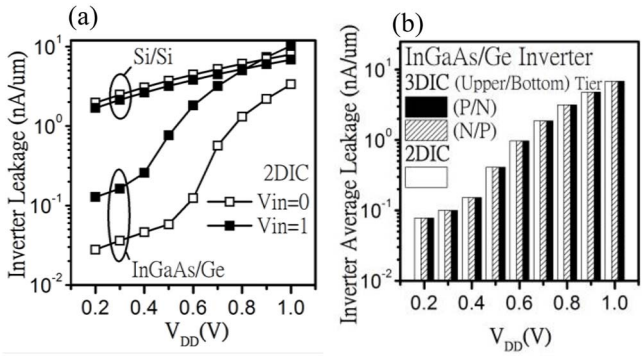


FIGURE 3. (a) Leakage comparison of 2D Si/Si and InGaAs/Ge inverters versus V_{DD} with input signal at "0" and "1", and (b) average leakage comparison of 2D and 3D InGaAs/Ge inverters versus V_{DD}.

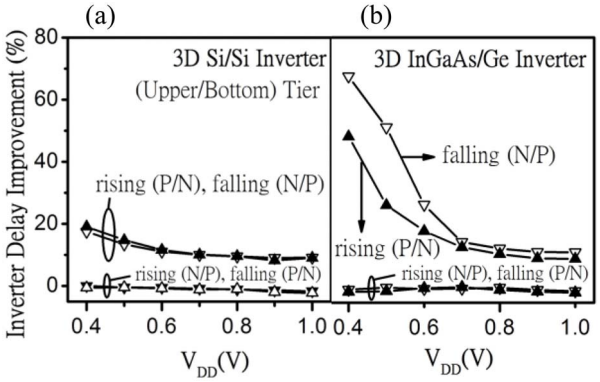


FIGURE 4. **Performance enhancement of (a) Si/Si and (b) InGaAs/Ge 3D 1-stage inverters over the 2D counterparts under different tier combinations and output rising and falling signals.**

leaky device. Note that compared with the planar 2D design using two back-gate biases, monolithic 3D structure offers minimum leakage without extra area overhead.

The delay time is defined as the time from input signal reaches 50% V_{DD} to when the output signal reaches 50% V_{DD}. Fan-out of 1 is considered and the input signal slew rate is derived from multi-stage inverter chains. Fig. 4 compares the delay improvements of various 3D 1-stage inverters over the 2D counterparts. For output falling (rising) delay, the delay time is determined by the strength of the pull-down NMOSFET (pull-up PMOSFET). Due to the strength enhancement of the upper-tier transistors, it can be seen that more than 10% improvement is achievable for the output falling delay with (N/P) tier combination and output rising delay with (P/N) combination. Moreover, the improvement over 2D design becomes more significant at lower V_{DD} due to the enhanced back-gate bias efficiency at lower V_{DD}. Compared with Si/Si counterparts, the InGaAs/Ge 3D inverters with larger back-gate bias efficiency exhibit higher performance enhancements. Fig. 5 shows the delay advantages of 3D Si/Si and InGaAs/Ge 5-stage inverters over the 2D cases. For InGaAs/Ge 5-stage inverters, 3D design with

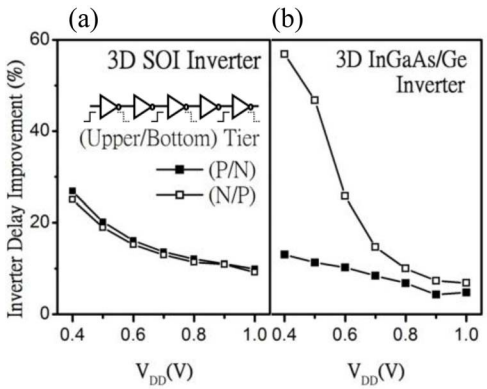


FIGURE 5. **Performance enhancement of (a) Si/Si and (b) InGaAs/Ge 3D 5-stage inverters over the 2D counterparts under different tier combinations.**

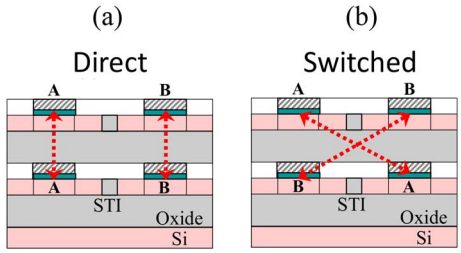


FIGURE 6. **Illustration of monolithic 3D 2-way NAND with (a) direct and (b) switched layouts.**

(N/P) tier combination exhibits more performance enhancement over the (P/N) design and Si/Si counterparts. It shows that monolithic 3D structure of both (N/P) and (P/N) tier combinations can reduce the inverter delay time without increasing leakage while considering interlayer coupling.

For monolithic 3D 2-way NAND, two possible layouts, namely direct and switched 3D layouts depending on the alignment of input gate at different layer, are shown in Fig. 6. Fig. 7 shows the leakage comparison of both InGaAs/Ge and Si/Si 2-way NANDs considering different tier combinations and layouts under different input signals (A,B). Most of the 3D cases show comparable leakage as 2D counterparts except for the (N/P) tier with switched layout design (Fig. 7(a)). Significantly larger leakage is found in 3D 2-way NANDs with (N/P) switched layout under (A,B) = (0,1) and (1,0). In such cases, the off-state NMOSFETs experience forward back-gate biases from the "1" input signal of the bottom-tier PMOSFETs, resulting in leakage increase. For InGaAs/Ge NANDs (Fig. 7(b)), lower leakage than the Si/Si counterparts are observed except for (A,B) = (1,1). Fig. 8 shows the worst-case leakage of InGaAs/Ge and Si/Si NANDs. It is observed that 3D InGaAs/Ge NANDs exhibit smaller leakage than that in the Si/Si counterparts even with I_{BTBT}.

Fig. 9 compares the bottom switching delays for 2D/3D InGaAs/Ge and Si/Si NANDs. As can be seen, 3D NANDs stacked in (N/P) tier combination lead to more than 10% delay improvement due to the strength enhancement of the upper-tier transistors. Moreover, the benefit in InGaAs/Ge 3D

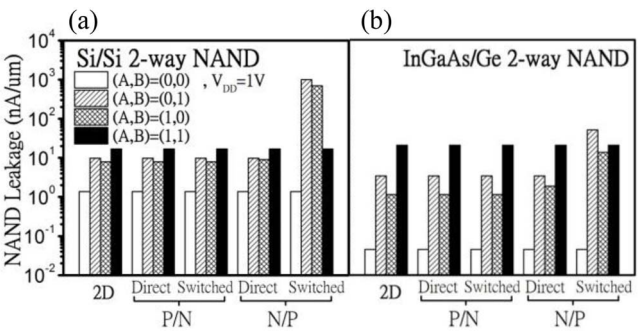


FIGURE 7. **Leakage comparison of (a) Si/Si and (b) InGaAs/Ge 2D and 3D 2-way NANDs with various layout designs, tier combinations and input signals.**

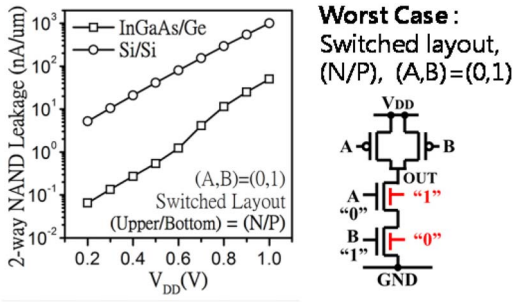


FIGURE 8. **Comparison of worst-case leakage for InGaAs/Ge and Si/Si 3D NANDs versus V_{DD}.**

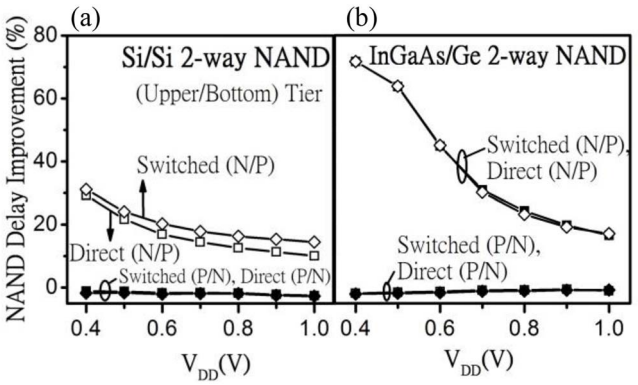


FIGURE 9. **Performance enhancement of (a) Si/Si and (b) InGaAs/Ge 3D 2-way NANDs over the 2D counterparts under different tier combinations and layout designs.**

NAND reaches 70% at lower V_{DD} due to its significant back-gate bias efficiency. It shows that monolithic 3D structure of (N/P) tier with switched layout can reduce the NAND delay time without increasing leakage while considering interlayer coupling.

IV. STABILITY AND PERFORMANCE OF 6T SRAM CELLS

Fig. 10 shows the definitions of read static noise margin (RSNM), V_{trip}, $V_{read,0}$, write static noise margin (WSNM) and $V_{write,0}$. Fig. 11(a) shows the static noise margin (SNM) of 2D InGaAs/Ge and Si/Si SRAM cells. RSNM of Si/Si SRAM is always critical for all V_{DD}. However, for InGaAs/Ge SRAM at low V_{DD}, the WSNM becomes more critical than RSNM due to the asymmetric V_T. The asymmetric V_T of InGaAs-n/Ge-p leads to larger $V_{write,0}$, causing the degradation in WSNM (Fig. 11(b)).

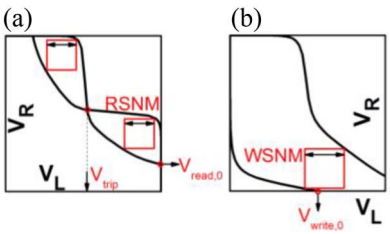


FIGURE 10. **Definitions of RSNM, V_{trip}, $V_{read,0}$, WSNM and $V_{write,0}$.**

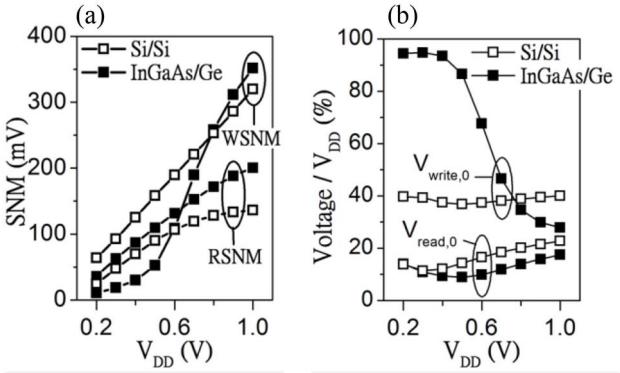


FIGURE 11. **(a) SNM of InGaAs/Ge and Si/Si 2D SRAM cells. (b) $V_{read,0}$ and $V_{write,0}$ verses V_{DD} for both InGaAs/Ge and Si/Si 2D SRAMs.**

Three possible 3D layouts depending on the gate alignment are listed below: (1) PG-PU (PU-PG), (2) PD-PU (PU-PD), (3) PD-PU, PG-$V_{L(R)}$, where PU, PD and PG represent pull-up, pull-down and pass-gate device in 6T SRAM cell, respectively [13]. The physical layouts are given in the APPENDIX. It should be noted that (P/N) PU-PD, $V_{L(R)}$-PG is not included in the following comparisons, because the back-gate bias condition is exactly the same as the (P/N) PU-PD layout but only with different footprint. Monolithic 3D layouts show up to 32% area reduction from 2D design; the reduction is not 50% due to the asymmetric NFET/PFET transistor number.

Fig. 12 compares the RSNM of InGaAs/Ge and Si/Si 2D and various 3D SRAM cells. For both InGaAs/Ge and Si/Si 3D SRAMs, the (N/P) PD-PU layout has the largest RSNM improvement over 2D design due to the smaller $V_{read,0}$. In addition, we can apply an adaptive global bottom-tier V_{bg} for 3D 6T SRAM for better stability and performance. The black bars in Fig. 12(a) and (b) show the larger RSNM improvement. (N/P) PD-PU with $V_{bg\_PMOS} = 0$, however, shows degradation in WSNM due to the increasing $V_{write,0}$ (Figs. 13(a), (b)). At low V_{DD}, where WSNM is critical for InGaAs/Ge SRAM, the (P/N) PU-PG layout with $V_{bg\_NMOS} = V_{DD}$ has the largest WSNM improvement over 2D design due to the smaller $V_{write,0}$ (Fig. 13 (c)). For both InGaAs/Ge and Si/Si SRAMs in standby mode, most of the 3D cases have equal leakage as 2D design except for PU-PG layout with (N/P) and (P/N) tier. The cell leakage of 3D (N/P) PG-PU and (P/N) PU-PG exhibit larger cell leakage since one side of the upper-tier off state PG and PU suffer from the dynamic forward-bias from the bottom-tier device, respectively (Fig. 14). Besides, InGaAs/Ge SRAMs exhibits lower leakage compares with the Si counterparts even with I_{BTBT}.

For SRAM cell performance analysis, the bit-line loading is estimated based on actual layouts with 64 cells per bit-line. The SRAM cell read access time (defined as the time from activation of the word-line to when the bit-line differential voltage reaches 10% V_{DD}) improves for the 3D cases with strengthened PG or PD transistors (Fig. 15). Besides, InGaAs/Ge 3D SRAMs exhibit more improvement

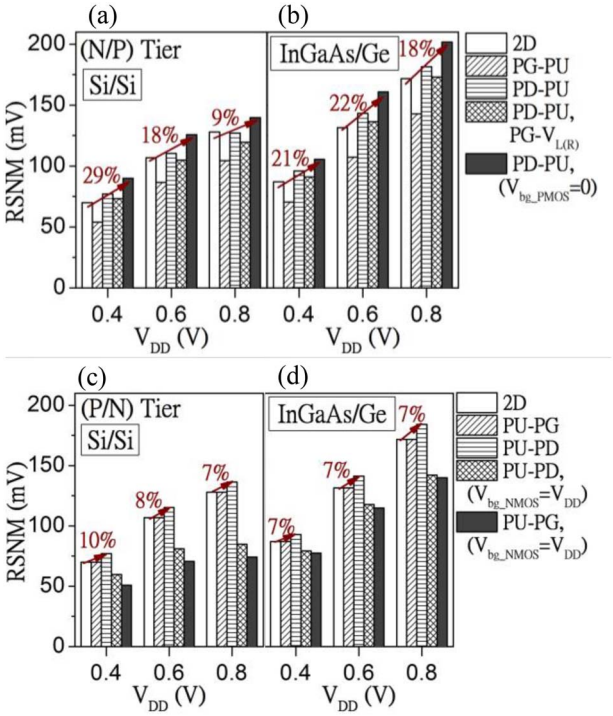


FIGURE 12. RSNM comparison of Si/Si and InGaAs/Ge 6T SRAMs with (Upper/Bottom) tier as (a)(b) (N/P) tier and (c)(d) (P/N) tier for 2D and various 3D layouts.

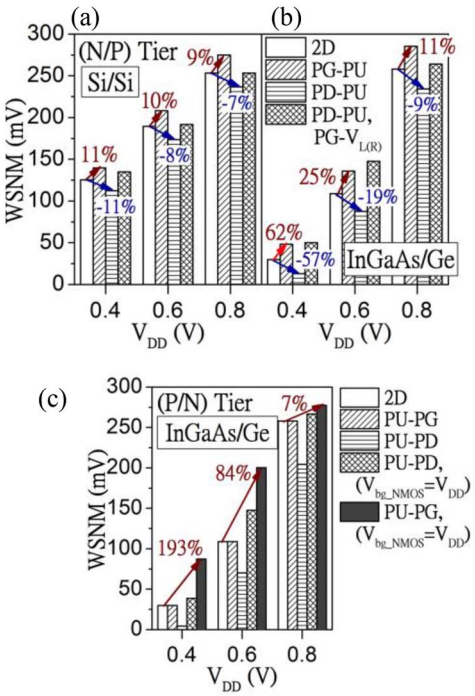


FIGURE 13. WSNM comparison of Si/Si and InGaAs/Ge 6T SRAMs with (Upper/Bottom) tier as (a)(b) (N/P) tier and (c) (P/N) tier for 2D and various 3D layouts.

over 2D design compared with the Si counterparts due to the larger back-gate bias efficiency, and the improvement increases with decreasing V_{DD}. For (P/N) PU-PG with

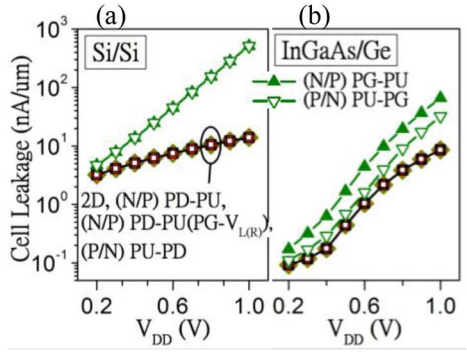


FIGURE 14. Leakage comparison of 2D and 3D (a) Si/Si and (b) InGaAs/Ge 6T SRAM cells under different tier combinations and layouts.

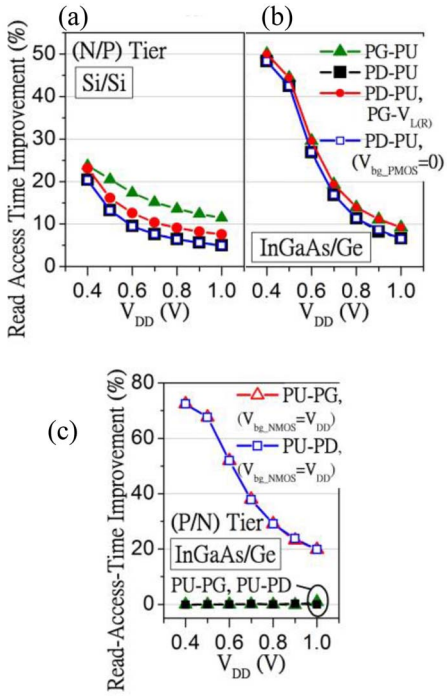


FIGURE 15. Read access time improvement comparison of 3D Si/Si and InGaAs/Ge 6T SRAMs with (Upper/Bottom) tier as (a)(b) (N/P) tier and (c) (P/N) tier under various 3D layouts.

V_{bg_NMOS} = V_{DD}, which has the largest WSNM improvement at low V_{DD}, the read access time has significant improvement due to the fixed forward body-to-source bias of the PG transistor.

The cell time-to-write (defined as the time from activation of the word-line to when the cell storage node voltages crossover) of 3D SRAM cells improves when PG transistors are strengthened (Fig. 16). Time-to-write will degrade while PU or PD is strengthened. Similar to read access time, InGaAs/Ge 3D SRAMs exhibit larger time-to-write improvement over 2D design compared with the Si counterparts due to the larger back-gate bias efficiency, and the improvement increases with decreasing V_{DD}.

For InGaAs/Ge 3D 6T SRAM with adaptive global V_{bg} considering interlayer coupling, we suggest the (N/P) tier

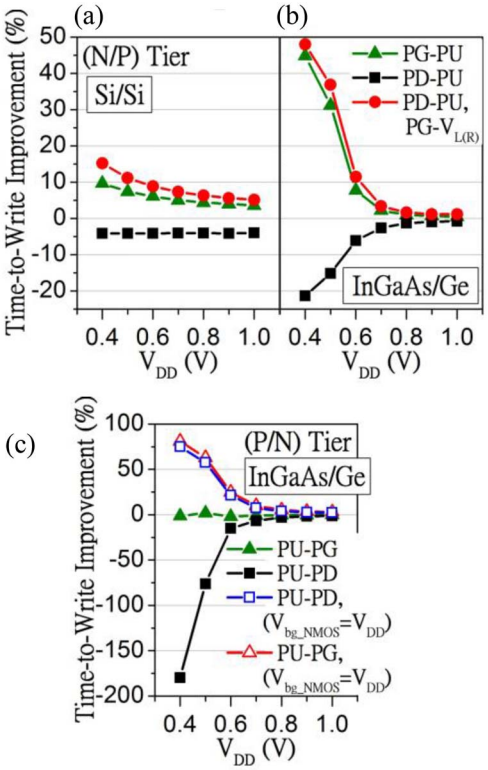


FIGURE 16. **Time-to-write improvement comparison of 3D Si/Si and InGaAs/Ge 6T SRAMs with (Upper/Bottom) tier as (a)(b) (N/P) tier and (c) (P/N) tier under various 3D layouts.**

TABLE 1. **Summary of cell stability and performance for 2D and monolithic 3D InGaAs/Ge 6T SRAMs under high performance operation (V_{DD} = 0.8V) and low power operation (V_{DD} = 0.4V).**

InGaAs/Ge 6T SRAM	RSNM (mV)	WSNM (mV)	Read Access Time (s)	Time-to -Write (s)	Cell Leakage (nA/um)
2D SRAM @V_{DD}=0.8V	172	258	7.57E-11	9.30E-12	3.82
(N/P) Tier, PD-PU @V_{DD}=0.8V	202 (V_{bg_PMOS}=0V)	234	6.71E-11 (V_{bg_PMOS}=0V)	9.43E-12	3.82
2D SRAM @V_{DD}=0.4V	87	30	2.24E-8	8.85E-10	0.175
(P/N) Tier, PU-PG @V_{DD}=0.4V	77	87 (V_{bg_NMOS}=V_{DD})	2.24E-8	1.68E-10 (V_{bg_NMOS}=V_{DD})	0.287

combination with PD-PU layout for high performance operation (e.g., V_{DD}= 0.8V), which has the least cell leakage and provides 18% RSNM improvement and about 11% improvement of read access time. For low power operation (e.g., V_{DD} = 0.4V), where the WSNM is more critical than RSNM, we suggest the (P/N) PU-PG layout that has slightly larger cell leakage but provides 193% WSNM improvement and more than 80% improvement of time-to-write (Table 1).

V. CONCLUSION

We have investigated the monolithic 3D logic circuits and 6T SRAMs composed of InGaAs-n/Ge-p MOSFETs while considering interlayer coupling. TCAD mixed-mode simulation results indicate that monolithic 3D InGaAs/Ge inverter and 2-way NAND stacked in (N/P) tier can improve the performance while maintaining equal leakage with 2D counterparts. Monolithic 3D InGaAs/Ge 6T SRAM can simultaneously improve the cell stability and performance while maintaining equal leakage with 2D counterparts through optimized layouts. We suggest (N/P) PD-PU for 3D SRAM high performance operation, which has the least cell leakage and provides 18% RSNM improvement and about 11% improvement of read access time. We suggest (P/N) PU-PG for 3D SRAM low power operation to improve WSNM significantly. Compared with the Si counterparts, 3D InGaAs/Ge logic circuits and 6T SRAM cells exhibit larger performance enhancement over 2D designs. Finally, it should be noted that the process induced variation (e.g., misalignment between the NMOS and PMOS layers) deserves further investigation in the future.

VI. APPENDIX

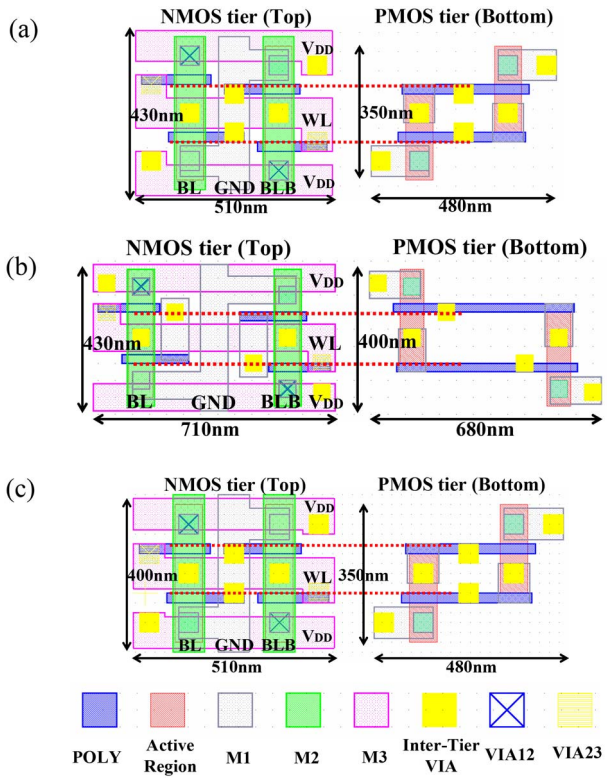


FIGURE 17. **Layouts of 6T SRAM cells for 3D designs with different gate alignments of transistors at distinct layers: (a) PD-PU (PU-PD), (b) PG-PU (PU-PG), and (c) PD-PU, PG-$V_{L(R)}$.**

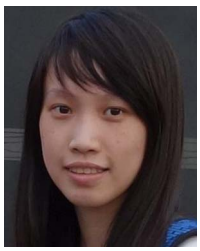
Fig. 17 shows the layouts of 6T SRAM cells for 3D designs with different gate alignments of transistors at distinct layers: (a) PD-PU (PU-PD), (b) PG-PU (PU-PG), and (c) PD-PU, PG-$V_{L(R)}$. The layouts are based on published design rules for 22nm technology node [14] and the applicable aspect ratio and size of interlayer vias for monolithic 3D integration [9] (Table 2). It can be seen that monolithic 3D SRAM with the PG-PU (PU-PG) layout consumes about 40% more footprint than the other two layouts.

TABLE 2. Summary of the pertinent design rules used in this work.

Parameter	Value (nm)
L_g	25
Minimum space between poly	100
M1, M2 Pitch	80
Minimum Space Between M1	35
Minimum Space Between M2	35
Minimum Width of VIA	50

REFERENCES

[1] C.-H. Shen *et al.*, "Monolithic 3D chip integrated with 500ns NVM, 3ps logic circuits and SRAM," in *IEDM Tech. Dig.*, Washington, DC, USA, 2013, pp. 232–235.
[2] C. Liu and S. K. Lim, "A design tradeoff study with monolithic 3D integration," in *Proc. Int. Soc. Qual. Electron. Design (ISQED)*, 2012, pp. 529–536.
[3] Y.-J. Lee, P. Morrow, and S. K. Lim, "Ultra high density logic designs using transistor-level monolithic 3D integration," in *Proc. Int. Conf. Comput.-Aidded Design (ICCAD)*, Austin, TX, USA, 2012, pp. 539–546.
[4] P. Batude *et al.*, "3-D sequential integration: A key enabling technology for heterogeneous co-integration of new function with CMOS," *IEEE J. Emerg. Sel. Topic Circuits Syst.*, vol. 2, no. 4, pp. 714–722, Dec. 2012.
[5] A. Lubow, I.-B. Sohrab, and T. P. Ma, "Comparison of drive currents in metal-oxide-semiconductor field-effect transistors made od Si, Ga, GaAs, InGaAs, and InAs channels," *Appl. Phys. Lett.*, vol. 96, no. 12, 2010, Art. ID 122105.
[6] T. Irisawa *et al.*, "Demonstration of InGaAs/Ge dual channel CMOS inverters with high electron and hole mobility using staked 3D integration," in *VLSI Symp. Tech. Dig.*, Kyoto, Japan, 2013, pp. T56–T57.
[7] T. Irisawa *et al.*, "Demonstration of ultimate CMOS based on 3D stacked InGaAs-OI/SGOI wire channel MOSFETs with independent back gate," in *VLSI Symp. Tech. Dig.*, Honolulu, HI, USA, 2014, pp. 1–2.
[8] P. Batude *et al.*, "3DVLSI with CoolCube process: An alternative path to scaling," in *VLSI Symp. Tech. Dig.*, Kyoto, Japan, 2015, pp. T48–T49.
[9] P. Batude *et al.*, "Advances in 3D CMOS sequential integration," in *IEDM Tech. Dig.*, Baltimore, MD, USA, Dec. 2009, pp. 1–4.
[10] *Sentaurus TCAD, C2009-06 Manual*, Synopsys, Mountain View, CA, USA, 2009.
[11] V. P.-H. Hu, M.-L. Fan, P. Su, and C.-T. Chuang, "Stability and performance optimization of InGaAs-OI and GeOI hetero-channel SRAM Cells," in *Proc. Eur. Solid-State Device Res. Conf. (ESSDERC)*, Bordeaux, France, 2012, pp. 77–80.
[12] Q. Liu *et al.*, "Impact of back bias on ultra-thin body and BOX (UTBB) devices," in *VLSI Symp. Tech. Dig.*, Honolulu, HI, USA, 2011, pp. 160–161.
[13] M.-L. Fan, V. P.-H. Hu, Y.-N. Chen, P. Su, and C.-T. Chuang, "Stability and performance optimization of heterochannel monolithic 3-D SRAM cells considering interlayer coupling," *IEEE Trans. Electron Devices*, vol. 61, no. 10, pp. 3448–3455, Oct. 2014.
[14] S. Narasimha *et al.*, "22nm high-performance SOI technology featuring dual-embedded stressors, epi-plate high-K deep-trench embedded DRAM and self-aligned via 15LM BEOL," in *IEDM Tech. Dig.*, San Francisco, CA, USA, 2012, pp. 3.3.1–3.3.4.



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