A Shield-Based Three-Port De-Embedding Method for Microwave On-Wafer Characterization of Deep-Submicrometer Silicon MOSFETs

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***Abstract*—A general three-port S-parameter de-embedding method using shield-based test structures for microwave on-wafer characterization is presented in this paper. This method does not require any physical equivalent-circuit assumption for the surrounding parasitics of a device-under-test. We use one open and three thru dummy devices to remove the parasitic components connected to the gate, drain, and source terminals of a MOSFET. By shielding the lossy silicon substrate, the cross-coupling from port to port can be significantly mitigated, and thus, the parasitics of probe pads and interconnects at each port can be separately subtracted. The MOS transistor and its corresponding dummy structures fabricated in a 0.18-μm CMOS process were characterized up to 20 GHz. Compared with the two-port cascade-based de-embedding method, the proposed three-port de-embedding procedure can further eliminate the parasitics associated with the dangling leg in the source terminal. The impacts of the accuracy of the de-embedding technique on device modeling and simulation are also discussed.**

***Index Terms*—De-embedding, MOSFET, parasitics, scattering parameters.**

I. Introduction

WITH the downscaling of device channel length in the deep-submicrometer technology, the accuracy of the on-wafer calibration and parasitic de-embedding techniques has become an extremely important issue for the device characterization and modeling in the radio frequency (RF)/ microwave regime. Since the fabrication of the precise 50-Ω load or well-defined 50-Ω transmission lines is still difficult with the current integrated circuit (IC) technologies [1], the classical calibration procedures, such as *short-open-load-thru* (SOLT), *line-reflect-match* (LRM), etc., are impractical for the wafer-level measurements conducted on silicon substrates. For this reason, the de-embedding techniques have been frequently used in conjunction with the on-wafer calibration procedure to remove the unwanted parasitics. In general, the parasitic components of a device-under-test (DUT) fabricated on silicon substrate mainly come from the probe pads, metallic interconnects, and semiconducting substrate. In order to obtain the intrinsic device performance from the raw measurement data, the dummy patterns should be carefully designed to reproduce and subtract the extrinsic parasitics of a fixtured device. In previous research [2]–[7], several de-embedding techniques based on lumped equivalent-circuit models have been developed and extensively used over the past years. These physical equivalent-circuit models consist of probe-pad and interconnect parasitics connected in parallel-series configurations. After subtracting the parasitic components in admittance (Y) and impedance (Z) domains, the impacts of unwanted parasitics on device characterization can be substantially reduced. However, as the operation frequency enters the multi-gigahertz regime and/or the interconnects become longer, these equivalent-circuit models may not work well, because they only take the resistive and inductive effects of the interconnects into account. Recently, a de-embedding technique based on cascade configurations [8], [9] has been developed to overcome the difficulties in the physics-based de-embedding methods. This method models the probe pads, interconnects, and intrinsic device in cascade connection, and does not use any equivalent-circuit representation for the parasitics. Although the two-port cascade-based de-embedding method using *ABCD* parameters can accurately calculate and eliminate the pad and interconnect parasitics, which comprise the resistive, inductive, capacitive, and conductive elements in both input (gate) and output (drain) ports, it still neglects the parasitics of the dangling leg. In this paper, we propose a three-port S-parameter de-embedding procedure based on multiport network analysis for on-wafer characterization of MOSFETs. With the application of the substrate-shielded technique [10], [11], the electromagnetic wave is confined in the vicinity of the microstrip-like transmission line, so that each port of the device can be treated as an individual port without mutual coupling from other ports. Consequently, the redundant parasitics in the gate, drain, and source terminals of a MOSFET can be separately subtracted, and the intrinsic device parameters can be calculated. To substantiate the proposed method, the MOS transistor and dummy structures fabricated using a 0.18 μm six-level CMOS technology were characterized up to 20 GHz with a multiport S-parameter measurement system, and the full-wave electromagnetic simulation based on the method of moment (MoM) was also accomplished.

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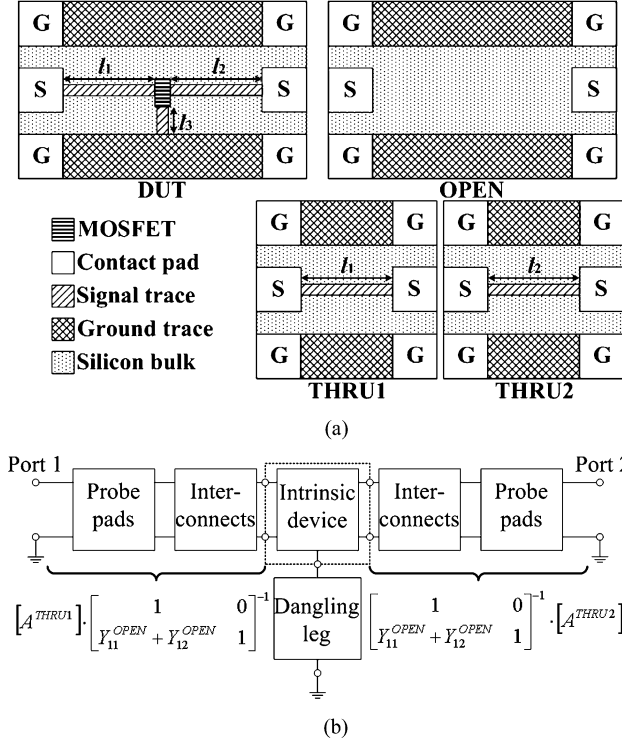

Fig. 1. Conventional two-port cascade-based de-embedding method. (a) DUT and its corresponding dummy structures. (b) Schematic diagram. $[A^{\mathrm{THRU}}]$ and Y^{OPEN} are the $ABCD$ matrix of the thru dummy and the admittance parameter of the open dummy, respectively.

II. Three-Port De-Embedding Theory

A. Substrate-Shielded On-Wafer Test Structures

Fig. 1 illustrates the two-port cascade-based de-embedding method. After subtracting the pad effects of the thru dummies by matrix operation, shown in Fig. 1(b), the distributed parasitic elements in the gate (port 1) and drain (port 2) of a MOSFET can be calculated and then removed. It should be noted that the parasitics of the dangling leg between the device and the ground trace are ignored in this method. For large multifinger MOSFETs, the length of the dangling leg (l_3) is short, and thus its parasitic effects are negligible. For small-sized MOS devices, nevertheless, the parasitic effects of the dangling leg would be considerable, and should be also taken into account. Fig. 2 shows the proposed three-port de-embedding method. The source terminal (port 3) of a MOSFET is connected to probe pads, instead of connecting to a ground. Here we introduce one open and three thru dummies for subtracting the additional parasitics in the gate, drain, and source terminals of a MOSFET. To minimize the substrate interaction and the crosstalk from port to port, the silicon bulk is shielded using the bottom metal (M_1), and the gate, drain, and source ports are placed on the west, east, and south sides, respectively. Then the three-terminal MOSFET can be viewed as an uncoupled system, and each port of it can be de-embedded individually.

B. Microwave Network Analysis

Consider the three-port network depicted in Fig. 2(b), where the primed quantities are referenced to the probing planes, and a_{n}' and b_{n}' are the amplitudes of incident and reflected waves at

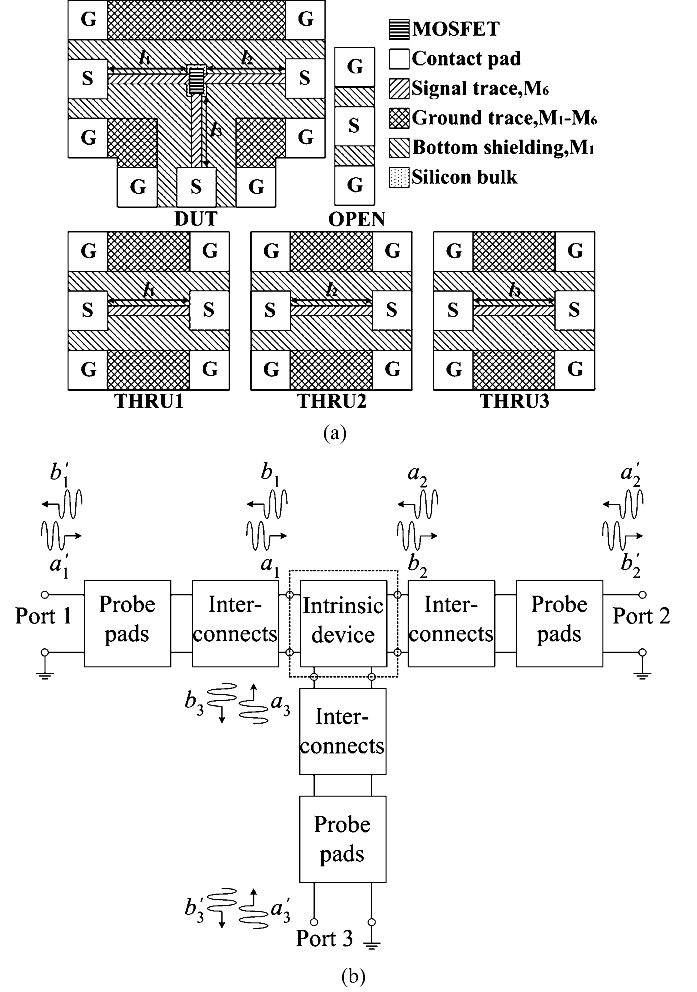

Fig. 2. Proposed three-port de-embedding method. (a) DUT and its corresponding dummy structures. (b) Schematic diagram.

port n, respectively. The 3×3 scattering matrix of the DUT measured at probing planes is denoted by $[S']$. After de-embedding the parasitics associated with the probe pads and interconnects from the measured S-parameters $[S']$, the reference planes are shifted to the terminal planes of the intrinsic device (dotted box), and the de-embedded scattering matrix is denoted by $[S]$. From the definition of the scattering matrix, we then have

$$\begin{bmatrix} b_1' \\ b_2' \\ b_3' \end{bmatrix} = \begin{bmatrix} S_{11}' & S_{12}' & S_{13}' \\ S_{21}' & S_{22}' & S_{23}' \\ S_{31}' & S_{32}' & S_{33}' \end{bmatrix} \begin{bmatrix} a_1' \\ a_2' \\ a_3' \end{bmatrix} \tag{1}$$

$$\begin{bmatrix} b_1 \\ b_2 \\ b_3 \end{bmatrix} = \begin{bmatrix} S_{11} & S_{12} & S_{13} \\ S_{21} & S_{22} & S_{23} \\ S_{31} & S_{32} & S_{33} \end{bmatrix} \begin{bmatrix} a_1 \\ a_2 \\ a_3 \end{bmatrix}. \tag{2}$$

As mentioned in the previous subsection, all three ports of the DUT can be approximately isolated by shielding the silicon substrate. Accordingly, the 2×2 scattering matrices of the networks, composed of probe pads and interconnects between the probing planes and the terminal planes of the intrinsic device, can be written in relation to the incident and reflected waves as

$$\begin{bmatrix} b_1' \\ a_1 \end{bmatrix} = \begin{bmatrix} S_{11}^G & S_{12}^G \\ S_{21}^G & S_{22}^G \end{bmatrix} \begin{bmatrix} a_1' \\ b_1 \end{bmatrix} \tag{3}$$

$$\begin{bmatrix} b_2' \\ a_2 \end{bmatrix} = \begin{bmatrix} S_{11}^D & S_{12}^D \\ S_{21}^D & S_{22}^D \end{bmatrix} \begin{bmatrix} a_2' \\ b_2 \end{bmatrix} \quad (4)$$

$$\begin{bmatrix} b_3' \\ a_3 \end{bmatrix} = \begin{bmatrix} S_{11}^S & S_{12}^S \\ S_{21}^S & S_{22}^S \end{bmatrix} \begin{bmatrix} a_3' \\ b_3 \end{bmatrix} \quad (5)$$

where $[S^{\mathrm{G}}], [S^{\mathrm{D}}]$, and $[S^{\mathrm{S}}]$ represent the scattering matrices of the parasitics in the gate, drain, and source terminals, respectively.

We can calculate the 2×2 chain scattering matrices (T-matrices) $[T^{\mathrm{G}}], [T^{\mathrm{D}}]$, and $[T^{S}]$, which include the parasitics of probe pads and interconnects in cascade at the gate, drain, and source ports, as

$$[T^G] = [T^{\mathrm{THRU1}}][T^{\mathrm{PAD}}]^{-1} \quad (6)$$

$$[T^D] = [T^{\mathrm{THRU2}}][T^{\mathrm{PAD}}]^{-1} \quad (7)$$

$$[T^S] = [T^{\mathrm{THRU3}}][T^{\mathrm{PAD}}]^{-1} \quad (8)$$

where $[T^{\mathrm{THRU1}}], [T^{\mathrm{THRU2}}]$, and $[T^{\mathrm{THRU3}}]$ are, respectively, the T-matrices of the THRU1, THRU2, and THRU3 dummies shown in Fig. 2(a), and $[T^{\mathrm{PAD}}]$ can be calculated from the 2×2 scattering matrices $[S^{\mathrm{PAD}}]$

$$[S^{\mathrm{PAD}}] = \frac{1}{S^{\mathrm{OPEN}} + 3} \begin{bmatrix} S^{\mathrm{OPEN}} - 1 & 2S^{\mathrm{OPEN}} + 2 \\ 2S^{\mathrm{OPEN}} + 2 & S^{\mathrm{OPEN}} - 1 \end{bmatrix} \quad (9)$$

where S^{OPEN} is the one-port S-parameter of the OPEN dummy shown in Fig. 2(a). It should be noted that here we can ignore the coupling effects between the probe pads at ports 1 and 2 of a thru dummy, because of the use of the bottom shielding. And then the T-parameters $[T^{\mathrm{G}}], [T^{\mathrm{D}}]$, and $[T^{S}]$ can be converted to S-parameters $[S^{\mathrm{G}}], [S^{\mathrm{D}}]$, and $[S^{\mathrm{S}}]$. The relationship between the S- and T-parameters is as follows [12]:

$$[S] = \begin{bmatrix} \frac{T_{21}}{T_{11}} & T_{22} - \frac{T_{21}T_{12}}{T_{11}} \\ \frac{1}{T_{11}} & -\frac{T_{12}}{T_{11}} \end{bmatrix} \quad (10)$$

$$[T] = \begin{bmatrix} \frac{1}{S_{21}} & -\frac{S_{22}}{S_{21}} \\ \frac{S_{11}}{S_{21}} & S_{12} - \frac{S_{11}S_{22}}{S_{21}} \end{bmatrix}. \quad (11)$$

Once the $[S'], [S^{\mathrm{G}}], [S^{\mathrm{D}}]$, and $[S^{\mathrm{S}}]$ are measured and calculated, (3)–(5) can be rewritten as

$$\begin{bmatrix} b_1' \\ b_2' \\ b_3' \end{bmatrix} = \begin{bmatrix} S_{11}^G a_1' \\ S_{11}^D a_2' \\ S_{11}^S a_3' \end{bmatrix} + \begin{bmatrix} S_{12}^G b_1 \\ S_{12}^D b_2 \\ S_{12}^S b_3 \end{bmatrix} \quad (12)$$

$$\begin{bmatrix} a_1 \\ a_2 \\ a_3 \end{bmatrix} = \begin{bmatrix} S_{21}^G a_1' \\ S_{21}^D a_2' \\ S_{21}^S a_3' \end{bmatrix} + \begin{bmatrix} S_{22}^G b_1 \\ S_{22}^D b_2 \\ S_{22}^S b_3 \end{bmatrix}. \quad (13)$$

Now from (1), (2), (12), and (13), we can relate the de-embedded scattering matrix $[S]$, which is the desired result, to the measured one $[S']$ as

$$[S] = ([G] \cdot ([S'] - [E])^{-1} \cdot [F] + [H])^{-1} \quad (14)$$

where

$$[E] = \begin{bmatrix} S_{11}^G & 0 & 0 \\ 0 & S_{11}^D & 0 \\ 0 & 0 & S_{11}^S \end{bmatrix} \quad (15)$$

$$[F] = \begin{bmatrix} S_{12}^G & 0 & 0 \\ 0 & S_{12}^D & 0 \\ 0 & 0 & S_{12}^S \end{bmatrix} \quad (16)$$

$$[G] = \begin{bmatrix} S_{21}^G & 0 & 0 \\ 0 & S_{21}^D & 0 \\ 0 & 0 & S_{21}^S \end{bmatrix} \quad (17)$$

$$[H] = \begin{bmatrix} S_{22}^G & 0 & 0 \\ 0 & S_{22}^D & 0 \\ 0 & 0 & S_{22}^S \end{bmatrix}. \quad (18)$$

C. *De-Embedding Procedure*

The proposed parasitic de-embedding procedure for three-port S-parameter characterization of MOSFETs is summarized as follows.

1) Measure the scattering matrices $[S'], [S^{\mathrm{OPEN}}], [S^{\mathrm{THRU1}}], [S^{\mathrm{THRU2}}]$, and $[S^{\mathrm{THRU3}}]$ of the DUT, OPEN, THRU1, THRU2, and THRU3 shown in Fig. 2(a), respectively.
2) Calculate the S-matrix $[S^{\mathrm{PAD}}]$ from (9) and convert $[S^{\mathrm{PAD}}]$ to its T-matrix $[T^{\mathrm{PAD}}]$ using (11).
3) Convert $[S^{\mathrm{THRU1}}], [S^{\mathrm{THRU2}}]$, and $[S^{\mathrm{THRU3}}]$ to their T-matrices $[T^{\mathrm{THRU1}}], [T^{\mathrm{THRU2}}]$, and $[T^{\mathrm{THRU3}}]$, respectively.
4) Calculate T-matrices $[T^{\mathrm{G}}], [T^{\mathrm{D}}]$, and $[T^{\mathrm{S}}]$, which include the pad and interconnect parasitics at the gate, drain, and source ports, using (6)–(8).
5) Convert $[T^{\mathrm{G}}], [T^{\mathrm{D}}]$, and $[T^{\mathrm{S}}]$ to their scattering parameters $[S^{\mathrm{G}}], [S^{\mathrm{D}}]$, and $[S^{\mathrm{S}}]$ using (10).
6) Calculate the intrinsic scattering parameters of the DUT using (14)–(18).

III. Results and Discussion

A standard 0.18 μm six-metal-layer CMOS process was used to fabricate the DUT and its corresponding dummy open and thru devices. An 800-nm-thick oxide was deposited on a 10–20 Ω·cm p-type silicon substrate, and the top metal (M_6) and the other metal layers $(\mathrm{M}_1 - \mathrm{M}_5)$ were respectively fabricated using 2 μm-thick and 0.6 μm-thick aluminum alloys. The thickness of each intermetal dielectric (IMD) is 1.4 μm, and the distance from top metal to silicon substrate is 7.8 μm. As shown in Fig. 2(a), the NMOS transistor with the dimensions of channel length $(L) = 0.18$ μm and channel width $(W) = 110$ μm (5 μm $\times$ 22 fingers) was connected in a three-port ground-signal-ground (GSG) configuration. And the dimensions of the interconnects between pads and transistor are: THRU1 ($W_1 = 10$ μm, $l_1 = 150$ μm); THRU2 ($W_2 = 10$ μm, $l_2 = 150$ μm); and THRU3 ($W_3 = 10$ μm, $l_3 = 160$ μm). The on-wafer three-port S-parameter measurements were performed with Agilent N1953B Physical Layer Test System (PLTS), which includes the E8362B Performance Network Analyzer (PNA) and the N4419B test set. Before S-parameter measurements, the measurement system was calibrated using the four-port SOLT calibration procedure with Cascade Microtech HPC GSG probes and a ceramic impedance standard substrate (ISS). It should be noted that here we ignore the effects of direct coupling between the RF probes, since the distance between any two signal tips of them is at least 200 μm. However, if the dimensions of the RF probes can be decreased so that the distance between them can be shortened, the impacts of the direct coupling between the RF probes on on-wafer measurements should be also taken into account [13].

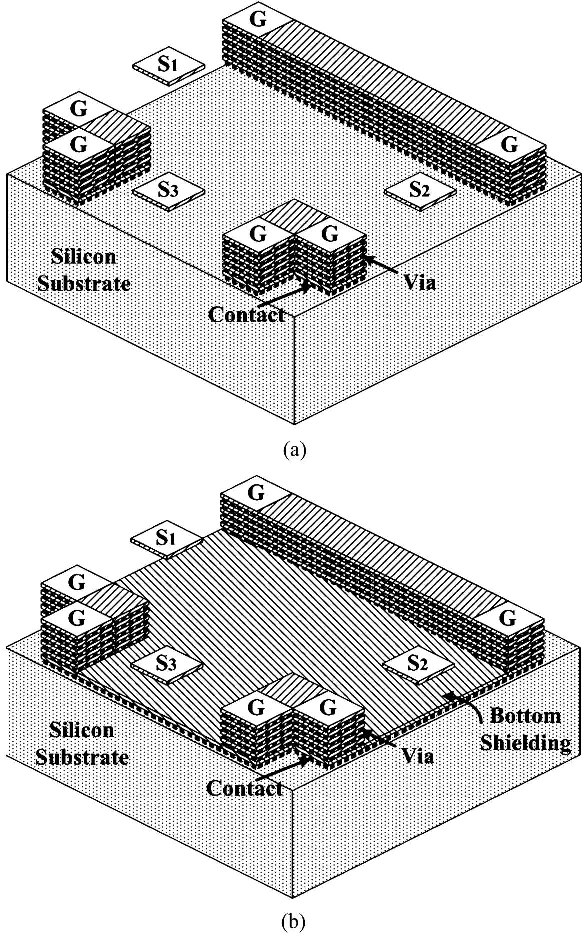

Fig. 3. Illustration of (a) conventional nonshielded and (b) substrate-shielded three-port open devices (not in scale).

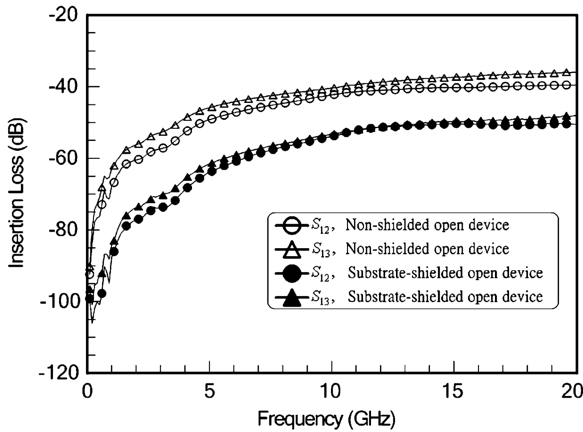

Fig. 4. Insertion losses of nonshielded and substrate-shielded three-port open devices.

A. Characteristics of Substrate-Shielded Test Structures

As has been discussed in the previous literature [14], [15], the forward coupling is mainly owing to the lossy silicon substrate. Therefore, here we adopt the bottom metal (M_1) to isolate the semiconducting substrate. As shown in Fig. 3, the conventional nonshielded and substrate-shielded three-port open devices have been fabricated and characterized. The shield was connected to the ground plates, which were composed of six shunting metal layers with dense via arrays, to ensure an accurate ground reference. Fig. 4 demonstrates the insertion

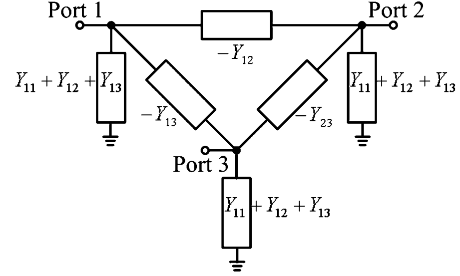

Fig. 5. Equivalent-circuit representation of a reciprocal three-port network.

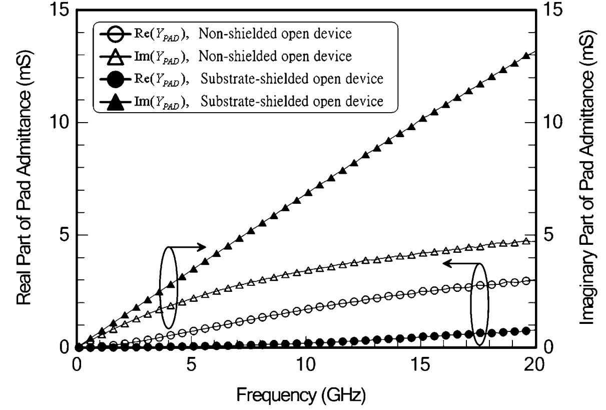

Fig. 6. Real and imaginary parts of pad admittances for nonshielded and substrate-shielded three-port open devices.

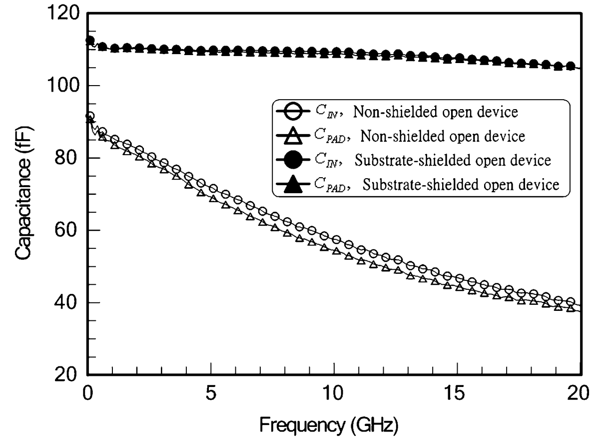

Fig. 7. Pad capacitances C_{PAD} and input capacitances C_{IN} of nonshielded and substrate-shielded three-port open devices.

losses S_{12} and S_{13} of the two structures (S_{23} is not shown for symmetry). We find that the forward coupling between each two-ports is significantly reduced by isolating the probe pads from the silicon substrate. The coupling from port 2 to port 1 is slightly lower than that from port 3 to port 1, due to the larger distance between them. For a reciprocal three-port open device, its admittance elements can be described using the equivalent circuit shown in Fig. 5, in which $Y_{11}+Y_{12}+Y_{13}$ is the pad admittance (Y_{PAD}) of the GSG pads at each port, and $-Y_{12}, -Y_{13}$, and $-Y_{23}$ are the coupling admittances among the three ports. Fig. 6 exhibits the conductive and capacitive behavior of the probe pads, i.e., $\Re(Y_{\mathrm{PAD}})$ and $\Im(Y_{\mathrm{PAD}})$. For the nonshielded open device, the pad admittances mainly consist of the oxide capacitance, substrate parasitics at each port, and substrate leakage between each two-ports, and hence, show a strongly lossy behavior. For the substrate-shielded open device,

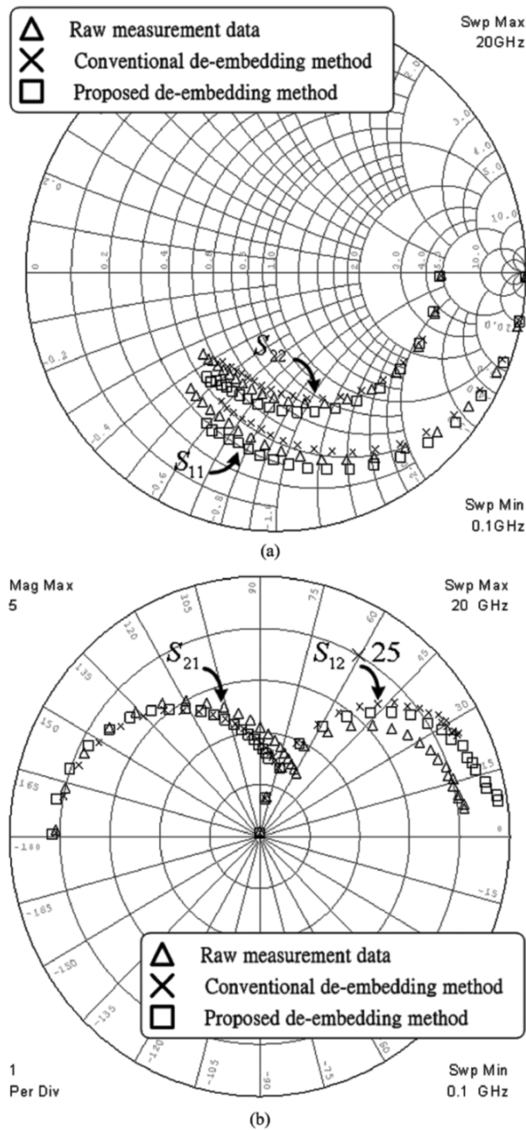

Fig. 8. Measured and de-embedded S-parameters of the fixtured MOSFET biased at $\mathrm{V_G} = \mathrm{V_D} = 1$ V and $\mathrm{V_S} = 0$ V ($\mathrm{I_{DS}} = 18.77$ mA). (a) S_{11} and S_{22}. (b) S_{12} and S_{21}.

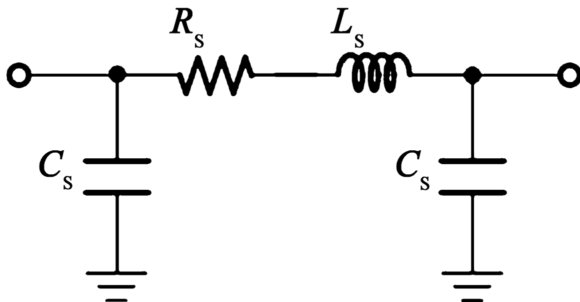

Fig. 9. TLM for the parasitics of the dangling leg. $R_{\rm s} = 0.595\ \Omega, L_{\rm s} = 48.2$ pH, $C_{\rm s} = 49.7$ fF.

however, the pad admittances only comprise the capacitive components distributed in the air and the oxide layer, and hence, exhibit a low-loss dielectric property. Fig. 7 illustrates the influences of forward coupling on the probe-pad capacitance, where the pad capacitance $C_{\rm PAD}$ is $\Im(-Y_{\rm PAD}/\omega)$, input capacitance $C_{\rm IN}$ is $\Im(-Y_{11}/\omega)$, and ω is the angular frequency.

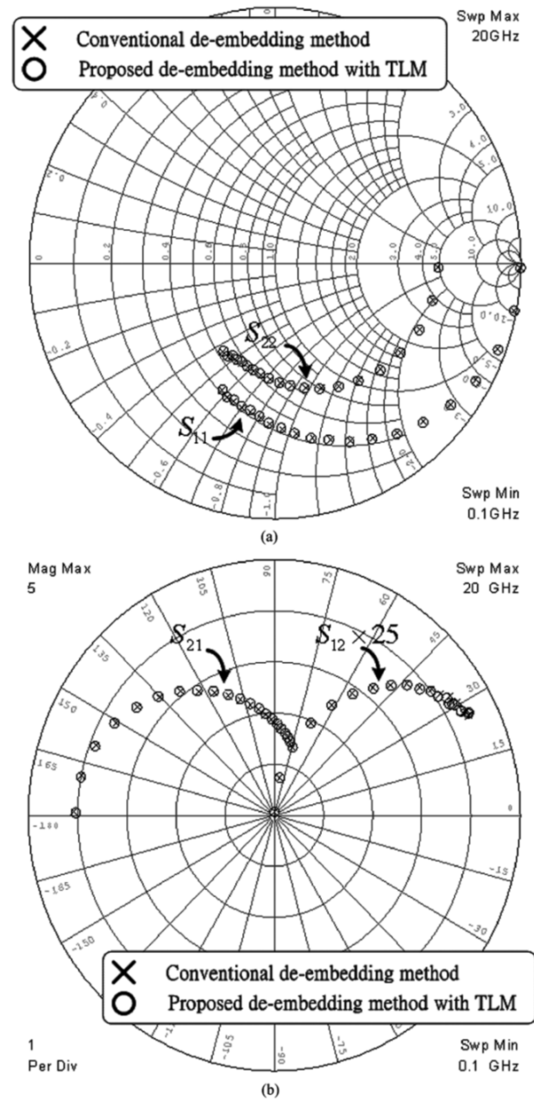

Fig. 10. S-parameters obtained from the proposed de-embedding method with additional TLM to include the parasitics of the dangling leg. The results of the conventional de-embedding method are also shown for comparison. (a) S_{11} and S_{22}. (b) S_{12} and S_{21}. The MOSFET was biased at $\mathrm{V_G} = \mathrm{V_D} = 1$ V and $\mathrm{V_S} = 0$ V ($\mathrm{I_{DS}} = 18.77$ mA).

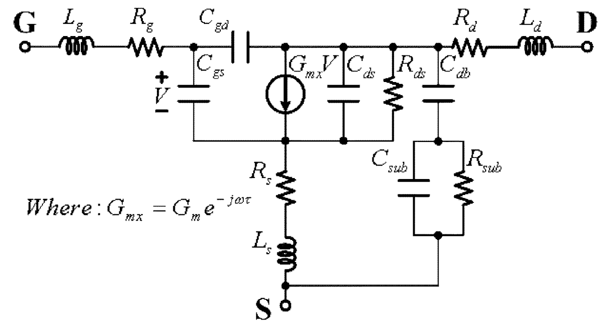

Fig. 11. Comprehensive small-signal equivalent-circuit model for the silicon MOSFET. $R_{\rm g} = 6.2\ \Omega, R_{\rm d} = 8.5\ \Omega, R_{\rm s} = 6.9\ \Omega, L_{\rm g} = 27.8$ pH, $L_{\rm d} = 0$ pH, $L_{\rm s} = 11.9$ pH, $C_{\rm gs} = 47.8$ fF, $C_{\rm gd} = 18.2$ fF, $C_{\rm ds} = 43.9$ fF, $R_{\rm ds} = 568.18\ \Omega, G_{\rm m} = 21.2$ mS, $\tau = 50$ fs, $C_{\rm db} = 26$ fF, $C_{\rm sub} = 0.67$ fF, $R_{\rm sub} = 1271\ \Omega$.

The considerable difference between the frequency-dependent pad capacitance and input capacitance of the nonshielded open device is observed, and it is believed that the coupling via

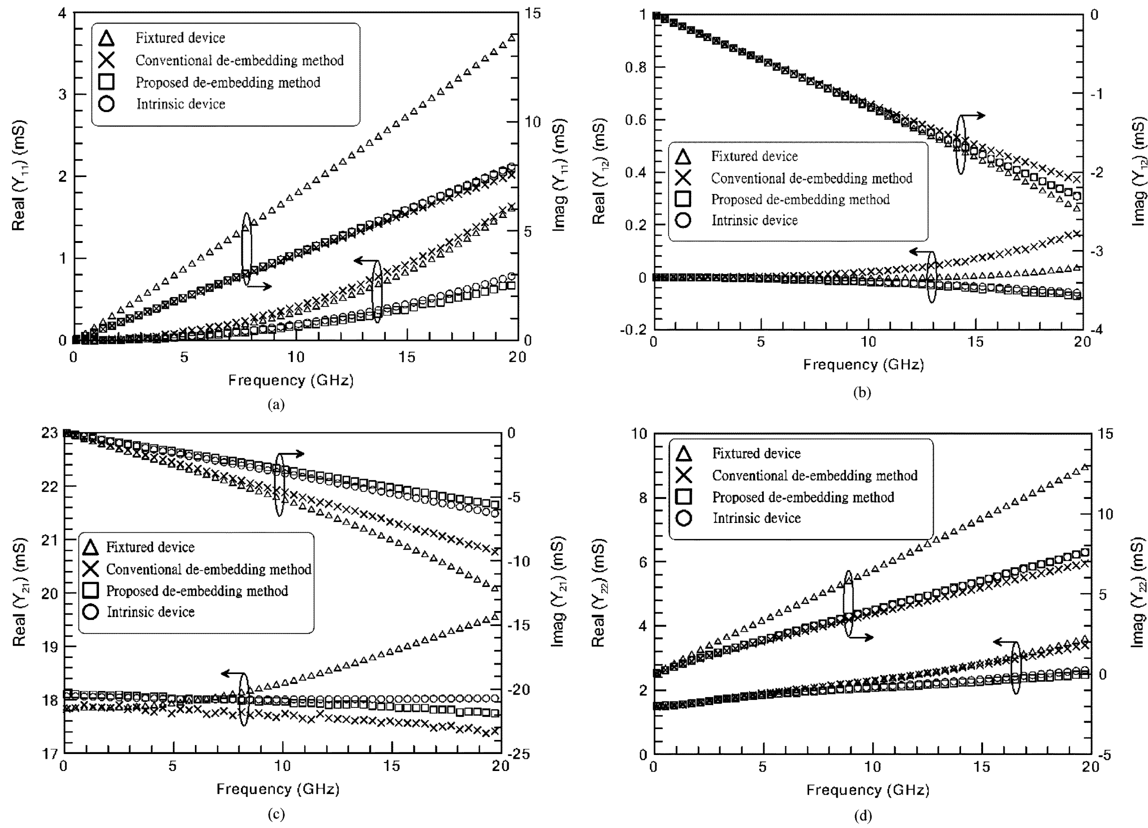

Fig. 12. Real and imaginary parts of the simulated and de-embedded Y-parameters obtained from the fixtured MOS model. The interconnect lengths are $l_1 = 150\ \mu\mathrm{m}, l_2 = 150\ \mu\mathrm{m}, l_3 = 160\ \mu\mathrm{m}$. (a) Y_{11}. (b) Y_{12}. (c) Y_{21}. (d) Y_{22}.

silicon substrate indeed contributes to the input capacitance. By employing the bottom shielding, the pad capacitance and the input capacitance of the substrate-shielded open device are nearly identical, and close to a constant value over the entire frequency range. It implies that the coupling effects among the three ports are efficiently mitigated. Accordingly, for the substrate-shielded open device, we can use the input capacitance instead of the pad capacitance, or, in other words, use the GSG probe pads instead of the multiport open device. These results also support the assumptions mentioned in the proposed three-port de-embedding theory. Based on the above results, it is concluded that the shielding technique can be used to isolate the silicon substrate, and thus, the procedure of parasitic de-embedding can be simplified.

B. Effects of External Parasitics on Device Characteristics

To substantiate the proposed three-port de-embedding method, we measured the S-parameters of the substrate-shielded DUT and dummy structures shown in Fig. 2(a). The surrounding parasitics of the MOSFET biased at $\mathrm{V_G} = 1$ V, $\mathrm{V_D} = 1$ V, and $\mathrm{V_S} = 0$ V ($\mathrm{I_{DS}} = 18.77$ mA) were de-embedded using the conventional two-port and proposed three-port de-embedding methods, respectively. It should be noted that here the conventional two-port de-embedding method uses the same DUT and dummy patterns, except for the THRU3 dummy for the dangling leg, as the proposed three-port one does for measurement consistency. If the parasitics in the source terminal remained, the three-port de-embedding method would degenerate to the conventional two-port de-embedding method. After respectively subtracting the parasitic effects using these two methods, we then converted the de-embedded three-port networks into the common-source MOSFET configurations to investigate the effects of the parasitics of the dangling leg on device characteristics. Fig. 8 compares the measured and de-embedded S-parameters of the MOSFET. The large difference between the measured and de-embedded results is observed. It is because the raw measurement data contain not only the intrinsic device parameters, but also the probe-pad and interconnect parasitics, which are comparable to the intrinsic device parameters. In addition, the difference between the conventional and proposed de-embedding methods due to the parasitics of the dangling leg is also demonstrated. The redundant parasitics of the source terminal will lower the accuracy of the extracted small-signal model parameters for silicon MOSFETs. For instance, the inductive parasitics of the probe pads and interconnects in the source terminal will affect the extracted values of source inductance and intrinsic capacitances of a MOSFET model [16]. The transmission-line model (TLM) illustrated in Fig. 9 was inserted between the source terminal and the ground reference of the de-embedded network using the proposed method, to simulate the additional source parasitics of the de-embedded network using the conventional method. As shown in Fig. 10, the calculated S-parameters obtained from the proposed de-embedding method with additional TLM are in excellent agreement with the conventional de-embedding method over the entire frequency range. It should be noted that the "×" curves used to represent the results of the conventional de-embedding method are the same

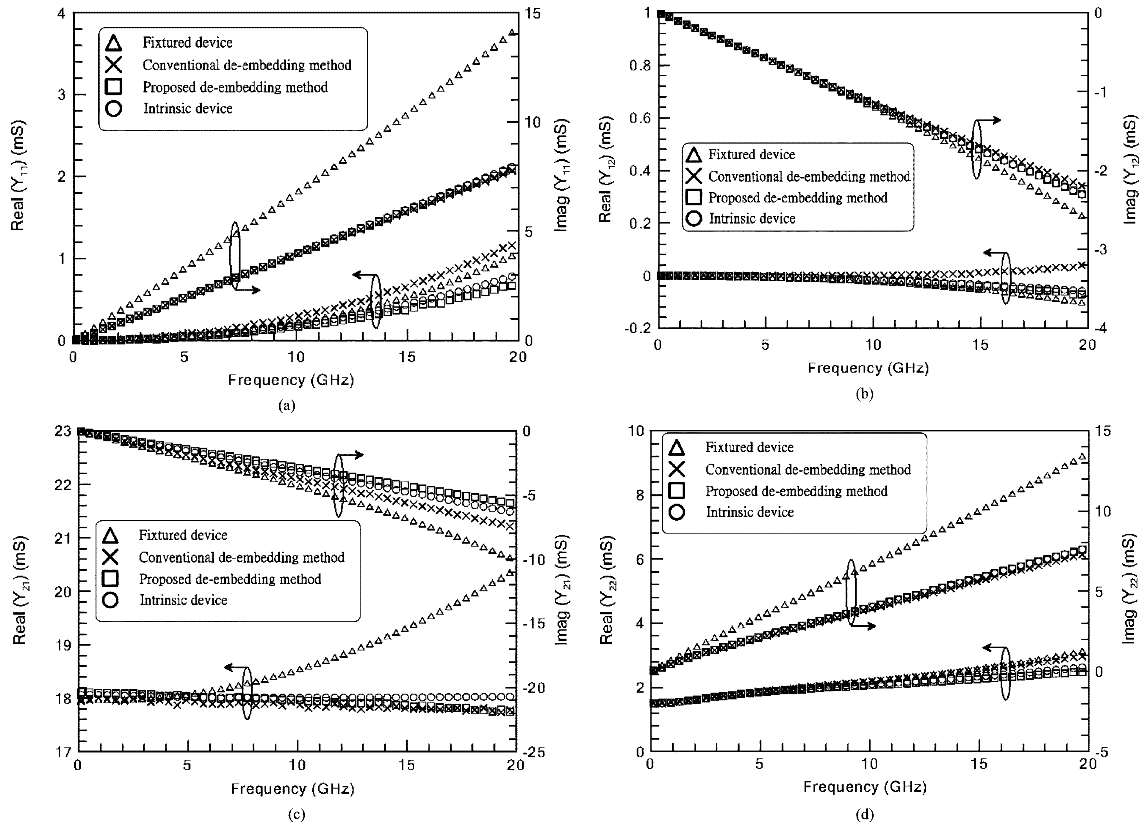

Fig. 13. Real and imaginary parts of the simulated and de-embedded Y-parameters obtained from the fixtured MOS model. The interconnect lengths are $l_1 = 150\ \mu$m, $l_2 = 150\ \mu$m, $l_3 = 60\ \mu$m. (a) Y_{11}. (b) Y_{12}. (c) Y_{21}. (d) Y_{22}.

in Figs. 8 and 10. The circuit parameters of this TLM extracted by curve-fitting techniques are $R_s = 0.595\ \Omega$, $L_s = 48.2$ pH, and $C_s = 49.7$ fF.

C. Verification Using Electromagnetic Simulator

In this subsection, Agilent Momentum, a MoM-based full-wave simulator, was used in conjunction with an intrinsic device of known behavior to adequately check the validity of the proposed three-port de-embedding method, and fairly compare it with the conventional two-port de-embedding method. As shown in Fig. 11, a comprehensive small-signal model was used as the intrinsic device, and its circuit parameters were extracted from a NMOSFET fabricated in a 0.18 μm six-metal-layer CMOS process, with the dimensions of channel length $= 0.18\ \mu$m and channel width $= 8 \times 5\ \mu$m [17]. The substrate-shielded DUT and dummy structures shown in Fig. 2(a) have been simulated by setting the substrate resistivity equal to 20 Ω·cm, and the metal conductivity equal to $3.8 \cdot 10^7$S/m, respectively. To investigate the impacts of the parasitics of the dangling leg on device characteristics, the DUT and dummy structures with two different interconnect dimensions listed below were designed and simulated.

Case 1: $l_1 = 150\ \mu$m, $l_2 = 150\ \mu$m, $l_3 = 160\ \mu$m.
Case 2: $l_1 = 150\ \mu$m, $l_2 = 150\ \mu$m, $l_3 = 60\ \mu$m.

Figs. 12 and 13 show the simulated and de-embedded Y-parameters as functions of frequency obtained from the two different fixtured devices. It is quite obvious that the proposed de-embedding method gives much better consistency between itself and the intrinsic device than the conventional de-embedding method does. These results also indicate that the longer the dangling leg is used for interconnection between the intrinsic device and the ground reference, the more parasitic effects it will have on the high-frequency device characteristics.

IV. Conclusion

In this paper, a three-port parasitic de-embedding theory using a shielding technique for microwave on-wafer characterization has been derived and validated. We introduced the substrate-shielded test structures to prevent the substrate leakage and the forward coupling between each two-ports. For this reason, each port of the DUT can be viewed as an isolated port without cross-coupling from other ports, and thus, the external parasitics in each port can be individually de-embedded to calculate the intrinsic device parameters. Compared with the conventional two-port cascade-based de-embedding method, the proposed method, using one open and three thru dummy structures, can further subtract the additional parasitics of the source terminal of a fixtured MOS transistor. Consequently, the impacts of the surrounding parasitics on device modeling and simulation can be completely removed, and the intrinsic device performance can be obtained.

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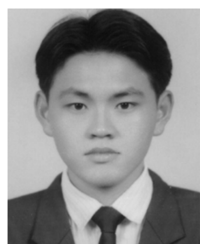

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