ESD Protection Design of Low-Voltage-Triggered p-n-p Devices and Their Failure Modes in Mixed-Voltage I/O Interfaces With Signal Levels Higher Than VDD and Lower Than VSS

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***Abstract*—Electrostatic discharge (ESD) protection design for mixed-voltage I/O interfaces with the low-voltage-triggered p-n-p (LVTp-n-p) device in CMOS technology is proposed. The LVTp-n-p, by inserting N+ or P+ diffusion across the junction between N-well and P-substrate of the p-n-p device, is designed to protect the mixed-voltage I/O interfaces for signals with voltage levels higher than VDD (over-VDD) and lower than VSS (under-VSS). The LVTp-n-p devices with different structures have been investigated and compared in CMOS processes. The experimental results in a 0.35-μm CMOS process have proven that the ESD level of the proposed LVTp-n-p is higher than that of the traditional p-n-p device. Furthermore, layout on LVTp-n-p device for ESD protection in mixed-voltage I/O interfaces is also optimized in this work. The experimental results verified in both 0.35- and 0.25-μm CMOS processes have proven that the ESD levels of the LVTp-n-p drawn in the multifinger layout style are higher than that drawn in the single-finger layout style. Moreover, one of the LVTp-n-p devices drawn with the multifinger layout style has been used to successfully protect the input stage of an asymmetric digital subscriber line (ADSL) IC in a 0.25-μm salicided CMOS process.**

***Index Terms*—Electrostatic discharge (ESD), human body mode (HBM), low-voltage-triggered p-n-p (LVTp-n-p), optical-beam-induced resistance change (OBIRCH), photon emission microscope (EMMI).**

I. Introduction

TO IMPROVE circuit operating speed and performance, device dimensions of MOSFET had been shrunk in advanced CMOS technology. In order to follow the constant-field scaling requirement and to reduce power consumption, the power-supply voltages in CMOS ICs have been also scaled downwards. So, a complex microelectronics system often meets the interfaces of semiconductor chips or subsystems with different internal power-supply voltages. With the different power-supply voltages in an electronic system, the I/O interface circuit and electrostatic discharge (ESD) protection circuit must be designed to avoid electrical overstress across the gate oxide [1], to avoid hot-carrier degradation [2] on the output devices, and to prevent undesirable leakage current paths between the chips [3], [4].

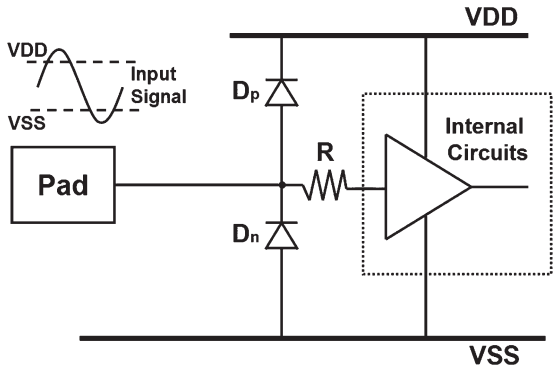

Fig. 1. Input signals with voltage levels higher than VDD and lower than VSS in some mixed-voltage I/O interfaces.

One of the mixed-voltage circuit applications, such as the interface in asymmetric digital subscriber line (ADSL), which has input signals with voltage levels higher than VDD and lower than VSS, is shown in Fig. 1. The traditional on-chip ESD protection circuits are not suitable for such mixed-voltage interfaces. The ESD diode $\mathrm{D_p}(\mathrm{D_n})$ will be forward biased when the input-signal levels are higher than VDD (lower than VSS). This ESD protection circuit will cause current leakage between the chips of the mixed-voltage I/O interface. Moreover, traditional on-chip ESD protection with NMOS/PMOS will also cause the same leakage issue and suffer the gate-oxide reliability issue when the over-VDD or under-VSS external signals reach the input pad. To meet such mixed-voltage I/O interface, the SCR device with floating P-well structure in an N-substrate CMOS process had been used as on-chip ESD protection device [5]. However, the SCR device with a floating-well structure is very sensitive to latchup [6], [7]. The mixed-voltage I/O interfaces in the system applications often have serious overshooting or undershooting signal transition, which could trigger on the SCR device in the ESD protection circuit of the I/O pad to induce latchup troubles to the chip [5].

In this work, a new ESD protection design with the low-voltage-triggered p-n-p (LVTp-n-p) device has been developed

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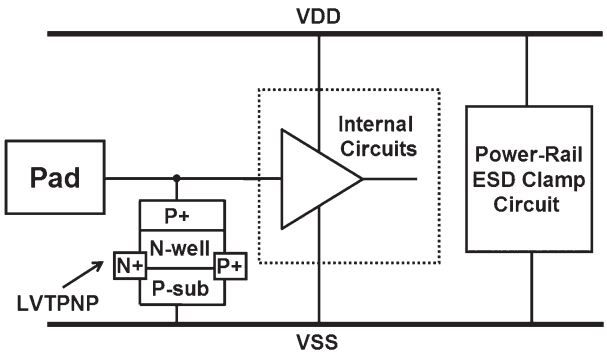


Fig. 2. New proposed ESD protection design with LVTp-n-p device for the mixed-voltage I/O interface with input voltage levels higher than VDD and lower than VSS.

to protect the I/O interfaces with input voltage levels higher than VDD or lower than VSS [8]. Comparing to the traditional p-n-p device in a CMOS process, the new proposed LVTp-n-p with a low breakdown voltage, by avalanche breakdown across the P+/N-well or N+/P-substrate junctions, provides an effective discharging path to protect the mixed-voltage I/O interfaces against ESD stresses. Under normal circuit operation conditions, the LVTp-n-p device is kept OFF without causing current leakage between the chips. Furthermore, layout optimization on the LVTp-n-p device to increase its ESD robustness per silicon area has been also studied [9]. The multifinger layout style is used to improve ESD robustness of the LVTp-n-p device. Moreover, the input stage of ADSL protected by the LVTp-n-p device has been practically implemented in a 0.25-μm salicided CMOS process to achieve a better ESD robustness.

II. ESD Protection Design With LVTp-n-p Devices and Their Layout Optimization

Due to the limitation on placing the ESD diode between the input pad and VDD/VSS power lines for the mixed-voltage I/O interface with over-VDD and under-VSS signal levels, a new ESD protection design with the LVTp-n-p device is shown in Fig. 2. The LVTp-n-p device is connected between the input pad and VSS power line, which provides ESD protection for such mixed-voltage I/O interface. With the help of a power-rail ESD clamp circuit [10], the positive-to-VSS (PS-mode), negative-to-VSS (NS-mode), positive-to-VDD (PD-mode), and negative-to-VDD (ND-mode) ESD stresses [11], [12] on the input pin can be discharged through the LVTp-n-p to VSS or VDD with the cooperation of the power-rail ESD clamp circuit.

A. Device Structures and Transmission Line Pulsing (TLP)-Measured I–V Characteristics

The cross-sectional view of the traditional p-n-p device in an N-well/P-substrate CMOS process is shown in Fig. 3(a), where the N-well is floating in this structure to avoid the leakage path from the pad to grounded P-substrate. The P+ diffusion (emitter) in the floating N-well is connected to the I/O pad for ESD protection. By inserting N+ or P+ diffusion across the junction between the N-well and P-substrate of the traditional p-n-p device, five new different structures of LVTp-n-p devices in Fig. 3(b)–(f) are proposed and investigated in this work to find the optimized design for ESD protection [8].

With the same device dimension of 30 μm $\times$ 30 μm (the width is defined as 30 μm) for all devices, the corresponding TLP-measured *I–V* curves among those devices under PS-mode and NS-mode stress conditions are shown in Fig. 4(a) and (b), respectively. The secondary breakdown currents (It2) among these devices are somewhat different, which could be caused by the different current distribution along the devices of different structures during ESD stress. Basically, the device with the more effective device width will present a higher ESD robustness. To further improve ESD level of such LVTp-n-p devices, the layout to increase effective device width will be studied and optimized in the next section.

B. Layout Parameters of LVTp-n-p Devices on Human Body Mode (HBM) ESD Levels

Under the 0.35-μm CMOS process without any extra mask layer, the ESD levels among the proposed LVTp-n-p devices with different layout parameters are compared in Fig. 5(a)–(g). The layout parameters include the width or spacing, $L_{\rm E}$, $L_{\rm C}$, X, Y, S, L_1, and L_2, which have been indicated in Fig. 3(a)–(f). For the gated2 LVTp-n-p device, the L_1 and L_2 are changed simultaneously in the layout.

In Fig. 5(a) and (b), as the width of the LVTp-n-p devices is increasing, the HBM ESD levels are improved under both positive-to-VSS and negative-to-VSS ESD-stress conditions. This confirms that when the area of effective ESD current flow from emitter to collector is increased, the heat will be dissipated through the larger region. Therefore, the device can sustain a higher ESD level.

In Fig. 5(c), as the spacing X of the type1 LVTp-n-p or the spacing Y of the type2 LVTp-n-p is increasing, the HBM ESD level is improved under the positive-to-VSS ESD-stress condition. Here, the LVTp-n-p devices, with the increase of X or Y, will have a wider field oxide region in the device structures, but the N+ or P+ diffusion across the N-well/P-substrate junction is kept to have the same diffusion layout spacing of 1.2 μm. The TLP-measured *I–V* curves of the type1 LVTp-n-p with different X spacings and the type2 LVTp-n-p with different Y spacings are shown in Fig. 6(a) and (b), respectively. As these spacings increase, the clamped voltage across the devices will be increased due to the increased turn-on resistances. The voltage drop across the base–collector (B–C) junction will increase to cause the emitter–base (E–B) potential barrier to be lowered. The lowering potential barrier at the E–B junction produces a large increase in current with a very small increase in B–C voltage. This effect is the so-called punchthrough breakdown phenomenon [13], which will occur before the avalanche breakdown. In Fig. 5(d), as the spacing S of the LVTp-n-p is increasing, the HBM ESD level is improved under the negative-to-VSS ESD-stress condition. In this ESD-stress condition, however, the parameter S plays the same role as parameters X and Y in the positive-to-VSS ESD-stress condition. Because these spacings increase, the voltage drop across the base–emitter (B–E) junction will increase to

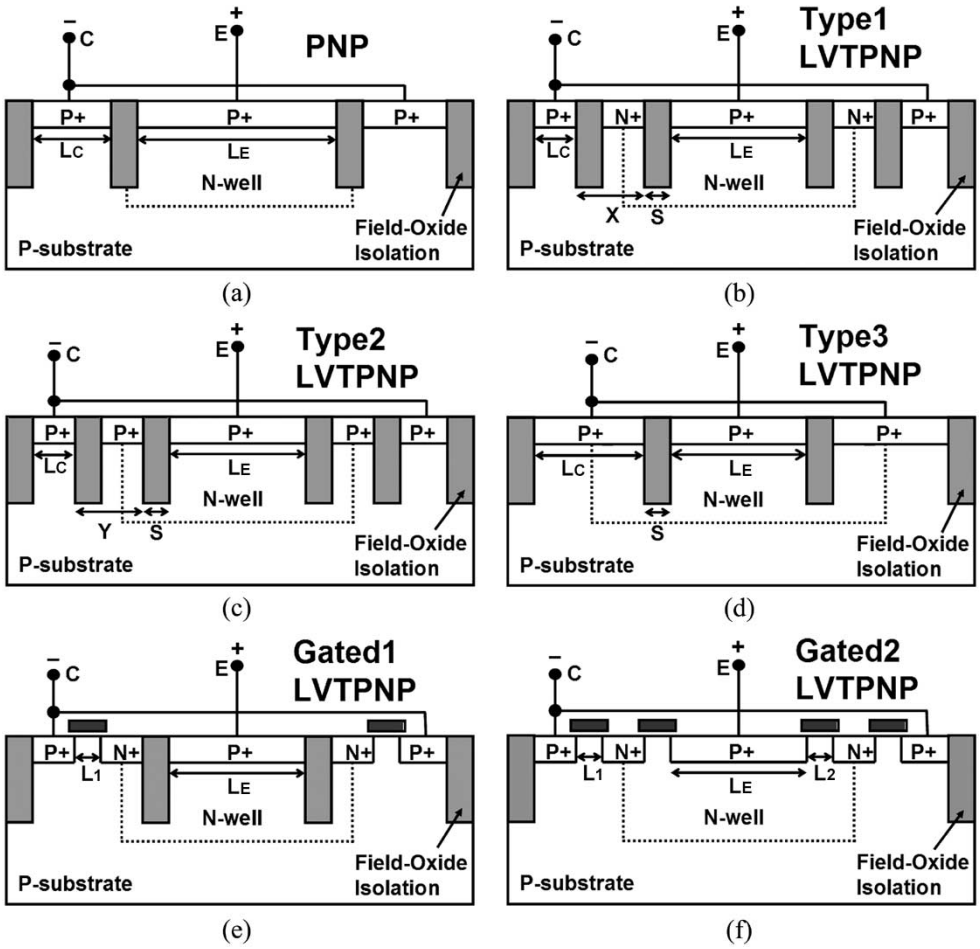


Fig. 3. Device structures of (a) the traditional p-n-p, (b) the type1 LVTp-n-p, (c) the type2 LVTp-n-p, (d) the type3 LVTp-n-p, (e) the gated1 LVTp-n-p, and (f) the gated2 LVTp-n-p.

cause the collector–base (C–B) potential barrier to be lowered. Therefore, the lowering potential barrier at the C–B junction produces a large increase in current, but with a very small increase in B–E voltage. From such results, these spacings in LVTp-n-p devices can be further optimized in layout to improve ESD robustness for applications in such mixed-voltage I/O interfaces.

In Fig. 5(e), as the L_{E} of the LVTp-n-p devices is increasing, the HBM ESD level is improved under the negative-to-VSS ESD-stress condition. Because the heat will be located around the B–E junction, as the emitter junction area is increased, the heat will be dissipated through the larger region. However, under the positive-to-VSS ESD-stress condition, this parameter has no influence on the ESD level, because the heat will be located around the B–C junction with the same area in the test chips.

The parameter L_{C} of the LVTp-n-p devices almost has no influences on the HBM ESD level. Under both positive-to-VSS and negative-to-VSS ESD-stress conditions, the heat will be located around B–C and B–E junctions, respectively. However, the heat will not be located around the P+ diffusion in the P-substrate.

In Fig. 5(f), as L_1 of the gated1 LVTp-n-p (L_1 and L_2 of the gated2 LVTp-n-p) is increasing, the ESD level is improved under the positive-to-VSS ESD-stress condition. In Fig. 5(g), as L_1 and L_2 of the gated2 LVTp-n-p is increasing, the ESD level is improved under the negative-to-VSS ESD-stress condition. However, in such ESD-stress mode, L_1 has no influence to the ESD level of both gated1 LVTp-n-p and gated2 LVTp-n-p. Such layout parameters L_1 (L_2) in the gated LVTp-n-p play the same role as that of the parameters $X(S)$ in the type1 LVTp-n-p, as well as the parameters $Y(S)$ in the type2 LVTp-n-p. By correctly adjusting the layout parameters, the desired ESD level of the mixed-voltage I/O interface can be achieved by the proposed LVTp-n-p devices with the optimized layout parameters.

C. Multifinger Layout Style for LVTp-n-p to Improve ESD Robustness

The ESD robustness of the LVTp-n-p device with the single-finger layout style, which is shown in Fig. 7(a), and its cross-sectional view shown in Fig. 7(b), cannot meet the ESD specification of 2-kV HBM ESD level in a limited silicon area. Therefore, based on the dependence of ESD levels on the layout parameters (including the width, L_{E}, L_{C}, X, Y, and S) of LVTp-n-p devices, the ESD level mainly depends on the effective device width from its emitter to its collector in both PS- and NS-mode ESD stresses. On the other hand, L_{E} affects only the NS-mode ESD level and L_{C} does not affect the ESD

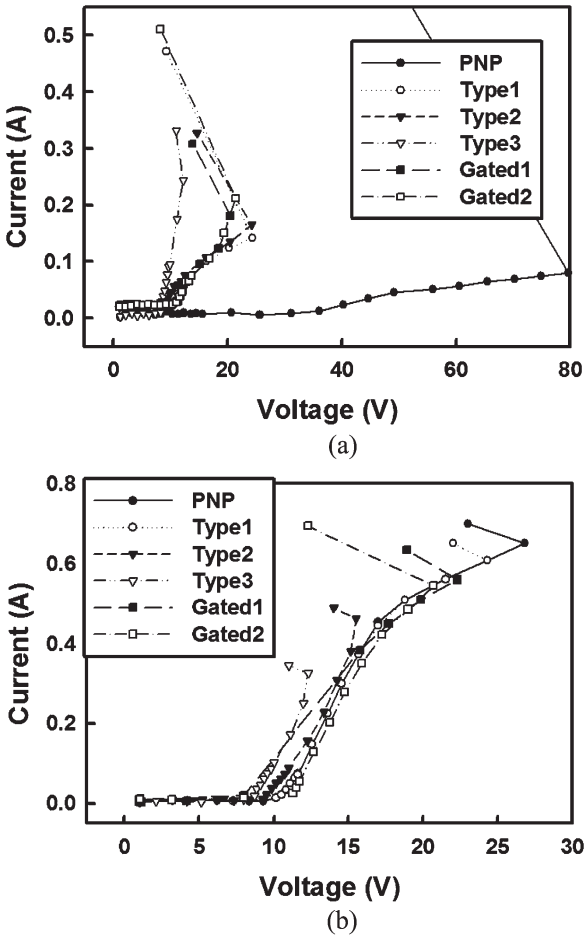


Fig. 4. TLP-measured *I–V* curves among traditional p-n-p and different LVTp-n-p devices under (a) the positive-to-VSS (PS-mode), and (b) the negative-to-VSS (NS-mode) stress conditions.

level. However, comparing the PS- and NS-mode ESD levels, the PS-mode ESD level is critical. Considering the parameters of effective device width, $L_{\rm E}$ and $L_{\rm C}$ are less sensitive to the ESD level than the effective device width. Therefore, a more compact realization of the LVTp-n-p can be implemented by using the minimum spacing of the design rules for $L_{\rm E}$ and $L_{\rm C}$ in each finger layout. The LVTp-n-p realized by the multifinger layout style is shown in Fig. 8(a), and its cross-sectional view is shown in Fig. 8(b), which will have more effective current flow for ESD protection.

The LVTp-n-p devices drawn with the single-finger layout style and the new proposed multifinger layout style have been fabricated in both 0.35-μm polycided and 0.25-μm salicided CMOS processes without any extra additional mask layer. Under the positive-to-VSS ESD-stress condition, the HBM ESD levels of the LVTp-n-p devices with the single-finger and multifinger layout styles are compared in Table I. In almost the same layout area (36 μm $\times$ 32 μm versus 33.6 μm $\times$ 36.5 μm), the LVTp-n-p devices with the multifinger layout style have much higher ESD robustness than those with the single-finger layout style in both 0.35-μm polycided and 0.25-μm salicided CMOS processes. Specifically, the type3 LVTp-n-p with multifinger layout has the highest ESD robustness, which can sustain an HBM ESD stress of 3.6 kV in the 0.35-μm polycided CMOS process and 1.4 kV in the 0.25-μm salicided CMOS process. Furthermore, within unit layout area, the ESD robustness of type3 LVTp-n-p is increased from 0.5 to 2.94 V/μm^2 in the 0.35-μm polycided CMOS process and from 0.68 to 1.14 V/μm^2 in the 0.25-μm salicided CMOS process.

Under the negative-to-VSS ESD-stress condition, the HBM ESD levels of the LVTp-n-p devices with the single-finger layout style and the new multifinger layout style are compared in Table II. In almost the same layout area, the LVTp-n-p devices with the multifinger layout style have much higher ESD robustness than those with the single-finger layout style in both 0.35-μm polycided and 0.25-μm salicided CMOS processes. Specifically, the type3 LVTp-n-p with multifinger layout has the highest ESD robustness, which can sustain an HBM ESD stress of 3.3 kV in the 0.35-μm polycided CMOS process and 3.8 kV in the 0.25-μm salicided CMOS process. Furthermore, within unit layout area, the ESD robustness of type3 LVTp-n-p is increased from 0.59 to 2.69 V/μm^2 in the 0.35-μm polycided CMOS process and from 1.71 to 3.10 V/μm^2 in the salicided 0.25-μm CMOS process. With suitable selection on the LVTp-n-p devices and layout style, the overall ESD robustness of the mixed-voltage I/O interfaces can be designed to meet the ESD specification of 2-kV HBM ESD level within a smaller silicon area. Specifically, the LVTp-n-p in the type3 device structure with multifinger layout style has excellent ESD performance.

Because the doping concentration in the 0.25-μm salicided CMOS process is higher than that in the 0.35-μm polycided CMOS process, the junctions have slightly lower breakdown voltages in the 0.25-μm CMOS process than that in the 0.35-μm CMOS process. With the single-finger layout style, HBM ESD levels of the LVTp-n-p devices in the 0.25-μm CMOS process are higher than those of the LVTp-n-p devices in the 0.35-μm CMOS process under both positive-to-VSS and negative-to-VSS ESD-stress conditions. Moreover, HBM ESD levels of the LVTp-n-p devices in the 0.25-μm CMOS process are higher than those of the LVTp-n-p devices in the 0.35-μm CMOS process under negative-to-VSS ESD-stress condition, when they are drawn with the multifinger layout style. However, HBM ESD levels of the LVTp-n-p devices in the 0.25-μm salicided CMOS process are lower than those of the LVTp-n-p devices in the 0.35-μm polycided CMOS process under positive-to-VSS ESD-stress condition for the multifinger layout style. The silicided diffusion in the 0.25-μm salicided CMOS process causes degradation on ESD robustness of the LVTp-n-p device drawn in multifinger layout style [14]. Under ESD-stress condition, the silicide diffusion on the device will cause the current to be crowded on the surface of the device and the heat will be located in the local area. To further increase the ESD level of the LVTp-n-p device in the 0.25-μm salicided CMOS process, the optional silicide-blocking mask layer can be used to block the silicide formation around the perimeter of the emitter region of the LVTp-n-p device.

Moreover, the TLP-measured *I–V* curves of LVTp-n-p devices with the single-finger layout style and the multifinger layout style in the 0.25-μm salicided CMOS process under PS-mode and NS-mode stress conditions are compared in Fig. 9(a) and (b), respectively. Due to the increase of total effective device width and the decrease of the length from

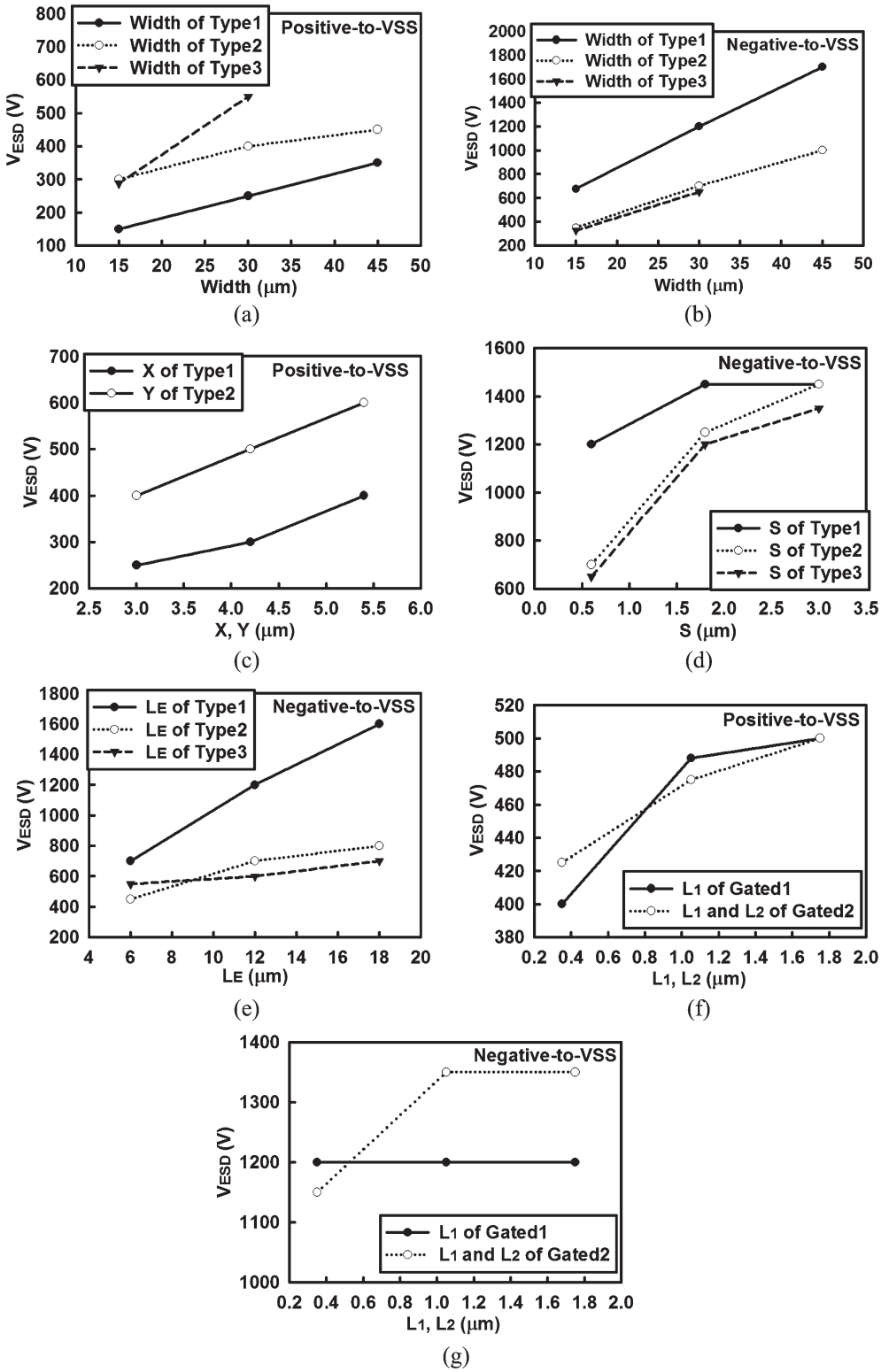


Fig. 5. (a) ESD level versus device width under the positive-to-VSS ESD-stress condition. (b) ESD level versus device width under the negative-to-VSS ESD-stress condition. (c) ESD level versus the spacing X of the type1 LVTp-n-p or the spacing Y of the type2 LVTp-n-p under the positive-to-VSS ESD-stress condition. (d) ESD level versus the spacing S under the negative-to-VSS ESD-stress condition. (e) ESD level versus device L_{E} under the negative-to-VSS ESD-stress condition. (f) ESD level versus L_1 or L_2 of the gated1 LVTp-n-p and the gated2 LVTp-n-p under the positive-to-VSS ESD-stress condition. (g) ESD level versus L_1 or L_2 of the gated1 LVTp-n-p and the gated2 LVTp-n-p under the negative-to-VSS ESD-stress condition.

its emitter to its collector, the LVTp-n-p devices with the multifinger layout style have lower turn-on resistances than those with the single-finger layout style in the same layout area. Hence, the It2 of LVTp-n-p devices with the multifinger layout style is higher than those with the single-finger layout style. For the single-finger layout style, however, because the turn-on resistance of the type3 LVTp-n-p is lower than those of the type1 and type2 LVTp-n-p, there will be factor differences

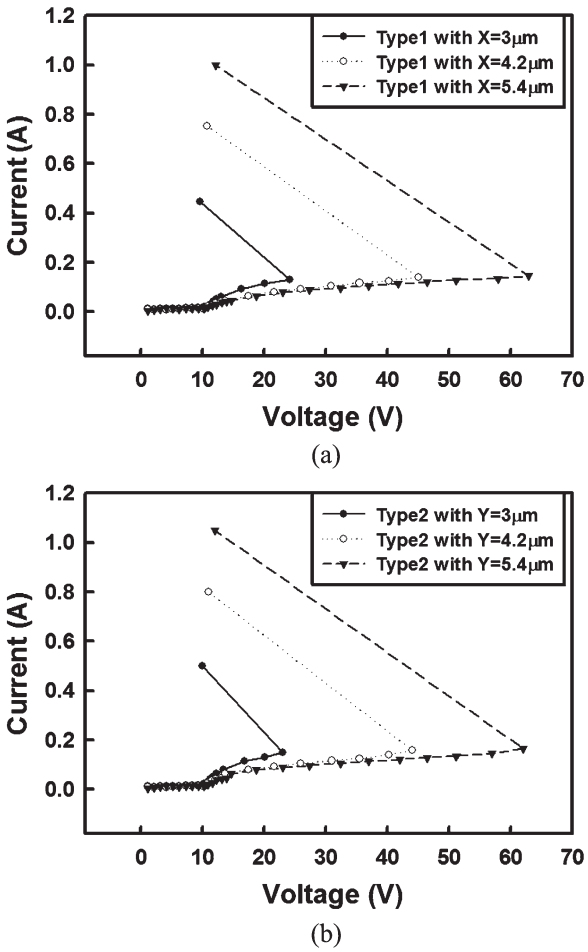


Fig. 6. TLP-measured *I–V* curves of (a) the type1 LVTp-n-p with different X spacings, and (b) the type2 LVTp-n-p with different Y spacings, under the positive-to-VSS stress condition.

in the improved ESD levels of different types of LVTp-n-p in the multifinger layout. Hence, correlating with the same increase of effective device fingers will result in different increase factors of It2 of the type1 (type2) LVTp-n-p and type3 LVTp-n-p.

III. Application in ADSL Interface

A. ESD Protection Design With the LVTp-n-p for the Input Stage of ADSL

The LVTp-n-p devices are used in the input ESD protection circuit for the ADSL interface, which has a high-voltage signal level of 5 V and a low-voltage signal level of -1 V. The ESD protection design for such ADSL input stage is shown in Fig. 10(a), where the single-ended operational amplifier (opamp) with divider resistors is the input stage of ADSL. The schematic of the single-ended opamp is shown in Fig. 10(b), which is composed of the input differential stage ($M_1 \sim M_4$), the output stage (M_6, M_7, R_C, and C_C), and the bias circuit ($M_8 \sim M_{10}$ and R_{bias}). In the 0.25-μm CMOS process with VDD of 2.5 V, the voltage divider (R and R_f), with a ratio of 30 to 1, is used to scale down the ADSL input signals, when the input signals (between 5 and -1 V) are transmitted into the ADSL IC. The V_{i2} is biased at the common reference

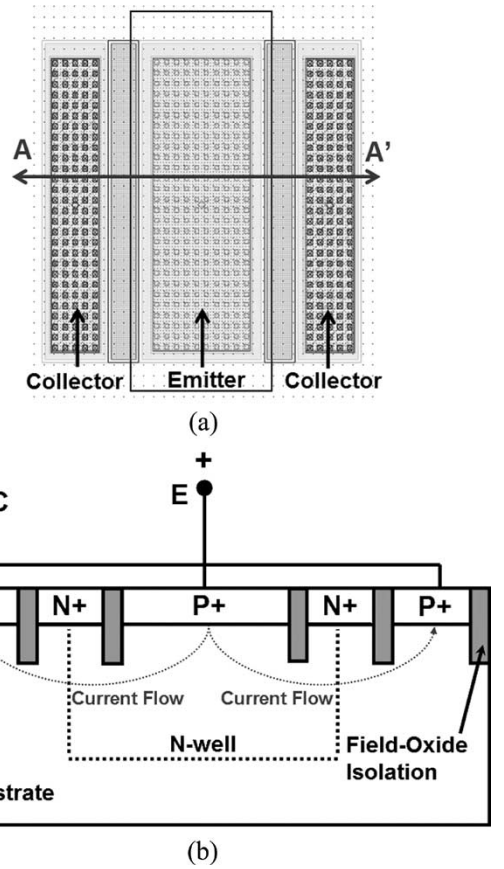


Fig. 7. (a) Single-finger layout style of the LVTp-n-p, and (b) cross-sectional view along the line AA′ in the single-finger layout of LVTp-n-p.

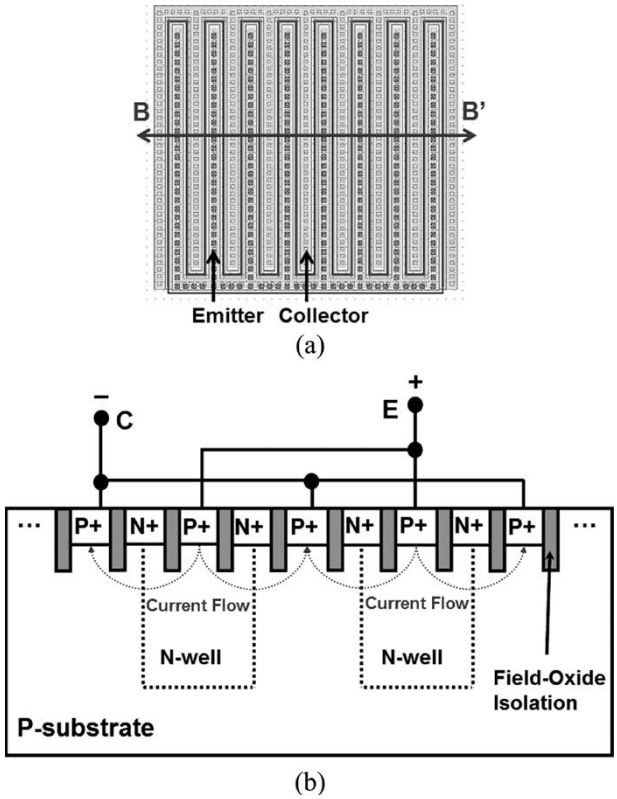


Fig. 8. (a) Multifinger layout style of the LVTp-n-p, and (b) cross-sectional view along the line BB′ in the multifinger layout of LVTp-n-p.

TABLE I
HBM ESD LEVELS OF THE LVTp-n-p DEVICES WITH DIFFERENT LAYOUT STYLES UNDER POSITIVE-TO-VSS ESD-STRESS CONDITION

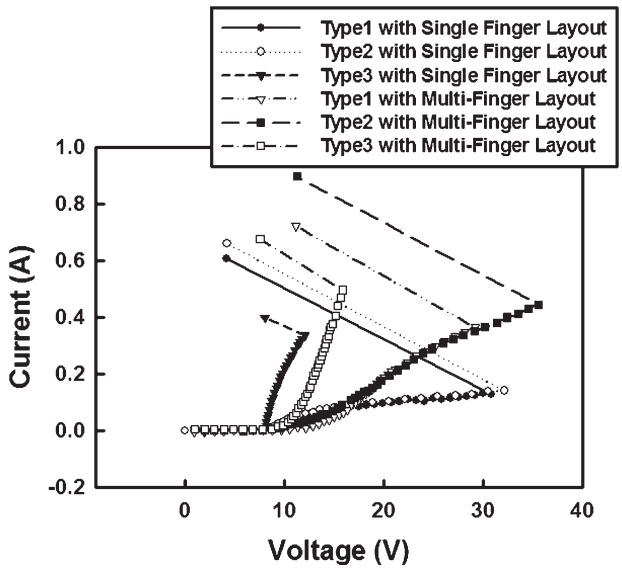
Device Layout Style	Type1 Single Finger Layout	Type2 Single Finger Layout	Type3 Single Finger Layout	Type1 Multi-Finger Layout	Type2 Multi-Finger Layout	Type3 Multi-Finger Layout
Layout Area (μm×μm)	36×32	36×32	36×32	33.6×36.5	33.6×36.5	33.6×36.5
HBM ESD Level (V) in a 0.35-μm CMOS Process	250	350	550	950	1050	3.6k
HBM ESD Level (V) in a 0.25-μm CMOS Process	350	350	750	850	900	1.4k
$V_{ESD/Area}$ (V/μm^2) in a 0.35-μm CMOS Process	0.22	0.3	0.5	0.77	0.86	2.94
$V_{ESD/Area}$ (V/μm^2) in a 0.25-μm CMOS Process	0.3	0.3	0.68	0.69	0.73	1.14

TABLE II
HBM ESD LEVELS OF THE LVTp-n-p DEVICES WITH DIFFERENT LAYOUT STYLES UNDER NEGATIVE-TO-VSS ESD-STRESS CONDITION

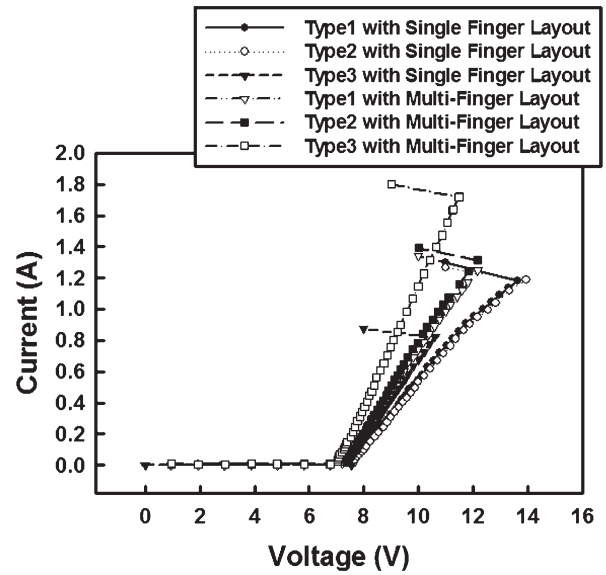
Device Layout Style	Type1 Single Finger Layout	Type2 Single Finger Layout	Type3 Single Finger Layout	Type1 Multi-Finger Layout	Type2 Multi-Finger Layout	Type3 Multi-Finger Layout
Layout Area (μm×μm)	36×32	36×32	36×32	33.6×36.5	33.6×36.5	33.6×36.5
HBM ESD Level (V) in a 0.35-μm CMOS Process	1.2k	700	650	2.6k	2.4k	3.3k
HBM ESD Level (V) in a 0.25-μm CMOS Process	2.4k	2.2k	1.9k	2.7k	2.8k	3.8k
$V_{ESD/Area}$ (V/μm^2) in a 0.35-μm CMOS Process	1.04	0.61	0.59	2.12	1.96	2.69
$V_{ESD/Area}$ (V/μm^2) in a 0.25-μm CMOS Process	2.08	1.91	1.71	2.20	2.28	3.10

voltage of 1.25 V, which is half of VDD. The voltage divider is formed by R and $R_{\rm f}$, which are designed to keep $V_{\rm i1}$ at the scaled-down voltage level and to make the single-ended opamp correct operation.

The TLP measurement of gate-oxide breakdown voltage of NMOS is about 13 V in the 0.25-μm CMOS process. On the other hand, for LVTp-n-p devices, the breakdown voltages are about 7–9 V. During TLP testing, no snapback characteristics



(a)



(b)

Fig. 9. TLP-measured *I–V* curves of the LVTp-n-p devices realized with the single-finger layout style or the multifinger layout style in a 0.25-μm salicided CMOS process under (a) the positive-to-VSS, and (b) the negative-to-VSS stress conditions.

are found due to the inefficient parasitic p-n-p bipolar gain, and the Vt2 will be higher than the gate-oxide breakdown voltage, especially the type1 and type2 LVTp-n-p, shown in Fig. 9. In Fig. 10, for the ADSL input stage, because the input signal will flow from R and $R_{\rm f}$ to $V_{\rm o}$, the voltage level at the differential input will be divided by R and $R_{\rm f}$. During ESD stress, if the divided voltage level on the differential input is larger than the gate-oxide breakdown voltage of the input NMOS, the ESD stress will damage the gate oxide of the input NMOS. By using the proposed ESD protection design with LVTp-n-p, the ESD current will discharge through the LVTp-n-p device to VSS. Because the Vt2 of the LVTp-n-p is lower than the voltage drop on R pulsing the gate-oxide breakdown voltage of NMOS, the gate oxide of the input NMOS can be successfully protected in this ADSL interface. By the way, the input node $(V_{\rm i1})$ of the opamp in Fig. 10(a) is also connected to its output $(V_{\rm o})$ through the feedback resistor $R_{\rm f}$, which will also help to clamp the overshooting voltage on the gate oxide of the input stage. To reduce the Vt2 at a given current level, the device width should be further increased to have a lower turn-on resistance. Among the LVTp-n-p devices, the type3 LVTp-n-p is selected for input ESD protection design in ADSL interface due to its highest HBM ESD level. In Fig. 10, the type3 LVTp-n-p device is connected between the input pad and VSS power line, and the power-rail ESD clamp circuit is realized by the *RC*-inverter-NMOS circuit [10]. The layout views of the ADSL input stage without and with ESD protection circuit are shown in Fig. 11(a) and (b), respectively. When ESD stress occurs at the input pin, the type3 LVTp-n-p will break down with a lower trigger voltage to discharge ESD current. With the power-rail ESD clamp circuit, the PS, NS, PD, and ND ESD stresses can be discharged through the type3 LVTp-n-p to VSS or VDD. Under PS-mode ESD-stress condition, the ESD current will flow from the input pad through LVTp-n-p to VSS. Under NS-mode ESD-stress condition, the ESD current will flow from VSS through LVTp-n-p to the input pad. Under PD-mode ESD-stress condition, the ESD current will flow from the input pad through LVTp-n-p to VSS, and then through the power-rail ESD clamp circuit to VDD. Under ND-mode ESD-stress condition, the ESD current will flow from VDD through the power-rail ESD clamp circuit to VSS, and then through LVTp-n-p to the input pad. Therefore, under PS- and PD-mode ESD-stress conditions, HBM ESD levels will mainly be determined by the LVTp-n-p in the PS-mode ESD-stress condition. Under NS- and ND-mode ESD-stress conditions, HBM ESD levels will mainly be determined by the LVTp-n-p in the NS-mode ESD-stress condition.

B. HBM ESD Levels of ADSL With the Type3 LVTp-n-p

When applying a positive bias (with VSS grounded and VDD floating) to the input pad of ADSL, the current will flow from R and $R_{\rm f}$ to $V_{\rm o}$, and then from $V_{\rm o}$ through the parasitic diode (drain–N-well p-n junction) of M_6 in the single-ended opamp to VDD, and finally from the VDD through the path of M_3–M_1–M_5 to VSS or through the bias circuit to VSS. Due to the turn-on bias circuit, M_7 will turn on. Therefore, before ESD stress, there is current flow from input through the internal circuits to VSS when applying a signal to the input pad. Due to the reason of initial current, to compare the ESD protection ability, the input stage of ADSL without and with the ESD protection circuit has been tested in HBM ESD stress with the failure criterion of 30% shifting on the voltage at 1-μA current bias from its original *I–V* curve [15]–[17]. The typical *I–V* curves of the input stage of ADSL with ESD protection circuit before and after the HBM PS-mode ESD stress of 1.5 kV are shown in Fig. 12, which was measured by applying a swept voltage from -1 to 5 V on the input pad with VSS grounded and VDD floating. Before ESD stress, while the input pad is swept from 0 to 5 V with grounded VSS (VDD floating), the signal paths will flow into the opamp circuit. Therefore, the *I–V* curve will become a straight line, with a slope equal to the reciprocal of $R + R_{\rm f}$, which starts at the voltage drop of internal circuits.

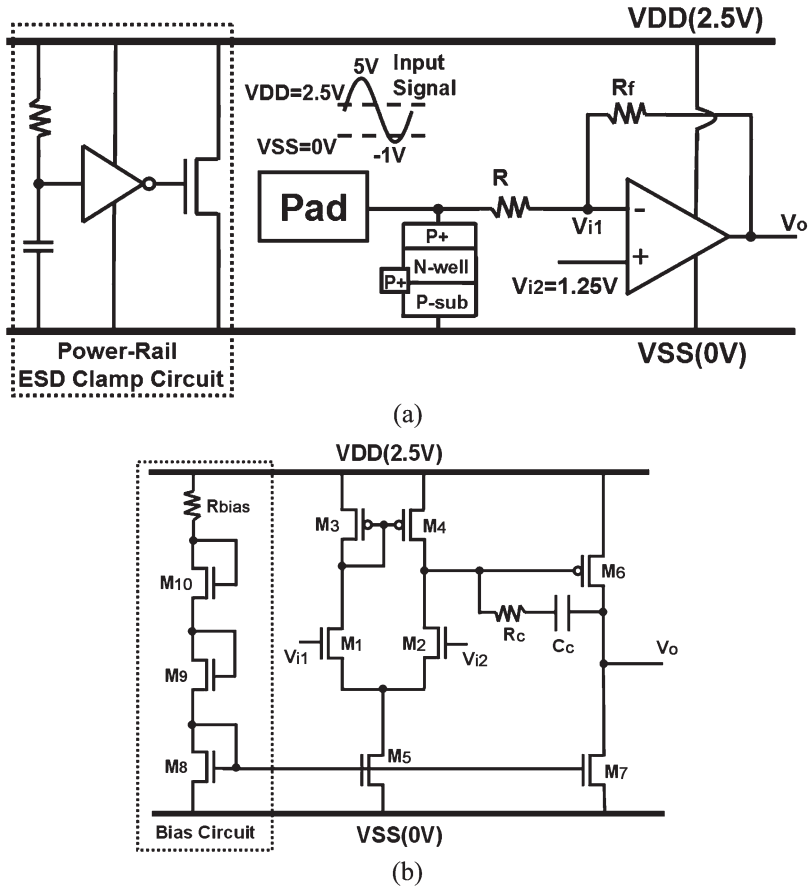


Fig. 10. (a) ESD protection design for the ADSL input stage with single-ended opamp and voltage divider in a 0.25-μm salicided CMOS process. (b) Schematic of the two-stage opamp.

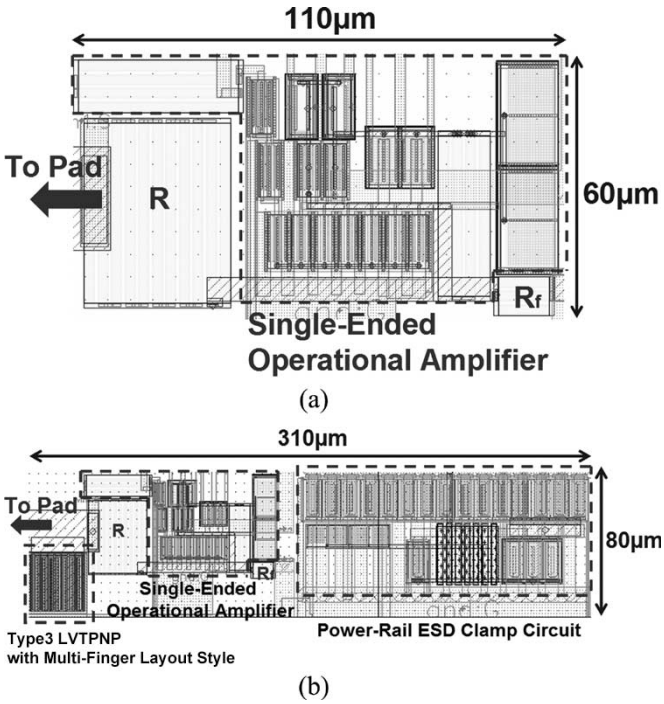


Fig. 11. Layout views of the ADSL input stage (a) without ESD protection, and (b) with ESD protection circuit.

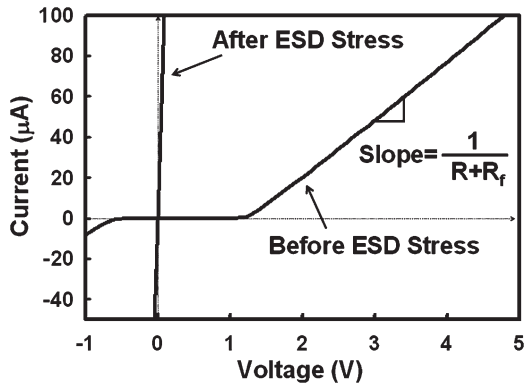


Fig. 12. *I–V* curves of the ADSL input stage with ESD protection circuit before and after PS-mode HBM ESD stress of 1.5 kV, which was measured by applying a swept voltage from -1 to 5 V on the input pad with VSS grounded and VDD floating.

Moreover, before ESD stress, while the input pad is swept from 0 to -1 V with grounded VSS (VDD floating), the input current will flow from VSS through the parasitic diode of M_7 in the single-ended opamp, and then through $R_{\rm f}$ and R to the input pad. Therefore, the *I–V* curve will become a straight line, with a slope equal to the reciprocal of $R + R_{\rm f}$, which starts at the cut-in voltage of the parasitic diode of M_7. However, after an

TABLE III
HBM ESD LEVELS OF THE ADSL INPUT STAGE WITH DIFFERENT ESD PROTECTION DESIGNS UNDER PS-, NS-, PD-, AND ND-MODE ESD-STRESS CONDITIONS

	PS-Mode (Positive-to-VSS)	NS-Mode (Negative-to-VSS)	PD-Mode (Positive-to-VDD)	ND-Mode (Negative-to-VDD)
ADSL Only	450V	350V	450V	400V
ADSL Including the Type3 LVTPNP with Single Finger Layout Style	750V	1.9kV	750V	1.9kV
ADSL Including the Type3 LVTPNP with Multi-Finger Layout Style	1.4kV	3.8kV	1.3kV	3.8kV

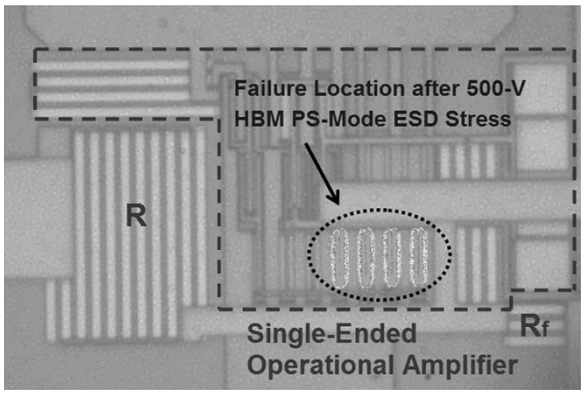


Fig. 13. EMMI picture on the ADSL input stage without ESD protection circuit after HBM PS-mode ESD stress of 500 V.

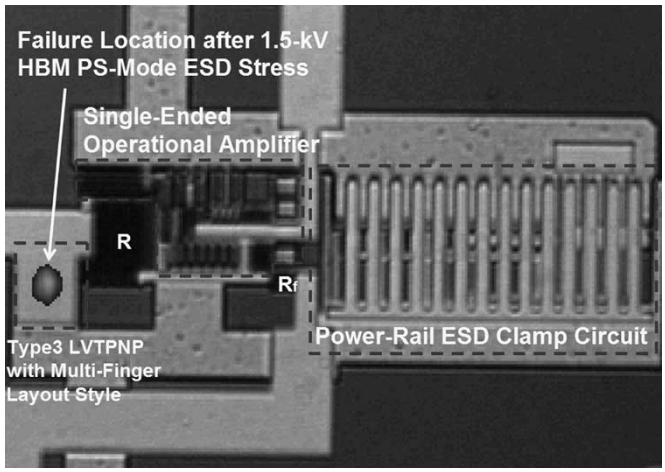


Fig. 14. OBIRCH picture on the ADSL input stage with ESD protection circuit after 1.5-kV HBM PS-mode ESD stress. The failure location is on the type3 LVTp-n-p device of the ESD protection circuit.

HBM ESD stress of 1.5 kV, the type3 LVTp-n-p is burned out to cause a short circuit line in the *I–V* curve.

The input stage of ADSL protected by the type3 LVTp-n-p devices in the single-finger layout style or the multifinger layout style and the power-rail ESD clamp circuit has been fabricated in a 0.25-μm salicided CMOS process. The HBM ESD levels of the ADSL input stage under PS-, NS-, PD-, and ND-mode ESD-stress conditions are shown in Table III. The LVTp-n-p in single-finger layout style is drawn with a device size of 36 μm $\times$ 32 μm, whereas the LVTp-n-p in the multifinger layout style is drawn with a device size of 33.6 μm $\times$ 36.5 μm. As seen in Table III, with the type3 LVTp-n-p and the power-rail ESD clamp circuit, the input stage of ADSL indeed can be protected from ESD stress. Moreover, HBM ESD levels of the input stage of ADSL protected by the LVTp-n-p in multifinger layout style are higher than those of the input stage of ADSL protected by the LVTp-n-p in single-finger layout style. To further increase ESD level, the layout area of LVTp-n-p should be increased with the multifinger layout style, or the silicide-blocking mask layer should be used to block the silicide formation around the perimeter of emitter region of the LVTp-n-p device.

C. Failure Analysis

The photon emission microscope (EMMI) picture of the ADSL input stage without ESD protection circuit after HBM PS-mode ESD stress of 500 V is shown in Fig. 13. The ESD damage, indicated by the arrow, is located on the opamp of the ADSL input stage.

In the layout of the ADSL input stage protected by LVTp-n-p, the type3 LVTp-n-p is fully covered by the metal layers on the top. The ESD damage on the device junction cannot be observed by the EMMI picture. Here, the optical-beam-induced resistance change (OBIRCH) [18], [19] is used to find the ESD-damage location on the input stage of ADSL with ESD protection circuit after HBM PS-mode ESD stress. The OBIRCH picture shown in Fig. 14 indicates the ESD damage located on the type3 LVTp-n-p device after 1.5-kV HBM PS-mode ESD stress. From the failure location in Fig. 14, the type3 LVTp-n-p indeed is triggered ON to conduct ESD current to effectively protect the mixed-voltage I/O interface of the ADSL input stage.

IV. Conclusion

ESD protection design for the mixed-voltage I/O interfaces with new proposed LVTp-n-p devices has been successfully verified to achieve a good ESD protection in a 0.35-μm CMOS process. The proposed LVTp-n-p devices have a higher ESD level than that of the traditional p-n-p device. Moreover, the multifinger layout style has been used to increase the effective device width among the LVTp-n-p device for improving ESD robustness in both 0.35- and 0.25-μm CMOS processes. Comparing among these LVTp-n-p devices, the type3 LVTp-n-p in the multifinger layout style can sustain the highest ESD stress for application in the mixed-voltage I/O interfaces. ESD protection codesigned with the LVTp-n-p device and the power-rail ESD clamp circuit has been successfully implemented to protect the ADSL input stage in a 0.25-μm salicided CMOS process.

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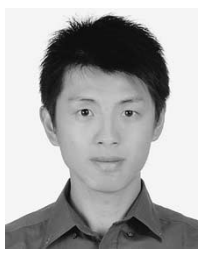

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