Int J Adv Manuf Technol (2005) 26: 585–590
DOI 10.1007/s00170-003-2031-1

ORIGINAL ARTICLE

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Downgrade decision for control/dummy wafers in a fab

Received: 22 August 2003 / Accepted: 10 November 2003 / Published online: 1 December 2004

Abstract Control and dummy (C/D) wafers are indispensable materials used in a semiconductor fab. C/D wafers stored in a high-grade buffer can be downgraded to several low-grade buffers. The downgrade decision is to determine the amount to downgrade for each of these low-grade buffers. Previous literature solves the downgrade decision by considering only the instantaneous WIP information, which is a short-term approach and may not yield the optimum solution in the long run. This paper presents an LP model to solve the downgrade decision problem, which aims to minimize the long-term daily usage of brand-new C/D wafers in a fab. The formulated problem assumes that the storage cost of C/D wafers is much less than the usage cost. This assumption has been justified by analyzing the cost structure of C/D wafers in a typical fab site.

Keywords Control wafers · Downgrade decision · Dummy wafers · Monitor wafers · Semiconductor fab · Test wafers

Notation

Designation and sets

c_i: Designation of C/D buffer i; $0 \leqq i \leqq r+1$, c_0 is the releasing buffer; c_r is the reclaiming buffer, c_{r+1} is the scrapping buffer, and c_i ($1 \leqq i \leqq r-1$) is a working buffer.
$P(i)$: The set of ancestor buffers of c_i in diagraph G, excluding c_0; i.e., $c_0 \notin P(i)$
$S(i)$: The set of descendant buffers for c_i in diagraph G

Parameters

D_i: Average daily demand of C/D wafers in c_i, $1 \leqq i \leqq r-1$
$m(i)$: Maximum number of cleaning recycle in c_i, $1 \leqq i \leqq r-1$
$r_i^{[k]}$: The yield of the kth cleaning recycle in c_i, $1 \leqq k \leqq m(i)$
n: Maximum number of grinding reclaim in c_r
$h^{[k]}$: The yield of the kth grinding reclaim in c_r, $1 \leqq k \leqq n$

Variables

O_{ij}: Daily quantity of C/D wafers downgraded from c_i to c_j in diagraph G
N_i: Daily quantity of brand-new C/D wafers downgraded to c_i from c_0
N: Daily quantity of brand-new C/D wafers downgraded from c_0; $N = \sum_{i=1}^{r-1} N_i$
Y_i: Daily quantity of reclaimed C/D wafers downgraded to c_i from c_0
$Z^{[k]}$: Daily quantity of C/D wafers, with k times of reclaim, sent to c_0 from c_r
Z: Daily quantity of reclaimed C/D wafers sent to c_0 from c_r, $Z = \sum_{k=1}^{n} Z^{[k]}$
$X_i^{[k]}$: Daily quantity of C/D wafers in c_i with kth cleaning recycle

1 Introduction

In semiconductor manufacturing, control wafers and dummy wafers are indispensable materials, used in ensuring the production quality. Control wafers, also called test wafers or monitor wafers, are used to monitor the wellness of tools and processes. To validate a tool/process, control wafers may be run before or concurrently with product wafers. Output parameters are then taken from control wafers to make adjustments on the tool/process, if necessary. Control wafers are often categorized into two types: particle wafers and thickness wafers. Particle wafers are for measuring the particle number to know the cleanliness of a tool. Thickness wafers are for measuring the deposition rate, etching rate or grinding rate of a particular process. Dummy wafers, generally lower in grade than control wafers, are often used in tools such as oxidation furnaces to provide a uniform temperature environment for better quality. In this paper, C/D wafers refer to either control or dummy wafers.

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A semiconductor fab keeps many types of C/D wafers with different specifications. C/D wafers of a particular specification are stored in a dedicated buffer, which supplies the C/D wafers to one or many tools. A C/D wafer, after being used in a tool, is sent to a cleaning recycle process within the fab for possible reuse. The recycled C/D wafers, if they meet the original specification, are kept in the present buffer. Those becoming lower in grade are downgraded to some other buffers. C/D wafers in a buffer can be repeatedly recycled up to a limited number of times. A buffer therefore stores various categories of C/D wafers, featuring in having received different times of recycles.

The process flow of using C/D wafers typically involves the following five steps: preprocessing, in-use, cleaning recycle, downgrade, and grinding reclaim. A thickness wafer for measuring the etching rate of a process is used to explain each step. The preprocessing step is to deposit a film on the control wafer. The in-use step measures the thickness of the film before and after the etching process to monitor the process quality. The cleaning recycle step, as mentioned, is an "in-house" operation, used to remove the film and clean the control wafer for reuse. The downgrade step is to deliver the C/D wafer to buffers that require lower grade. The grinding reclaim, often carried out by vendors, is to grind off some 20–30 um silicon materials from the C/D wafer. A reclaimed C/D wafer, becoming higher in grade, is functionally like a brand-new C/D wafer. The number of grinding reclaims for a C/D wafer is limited.

For a downgrade procedure, the buffer that delivers C/D wafers is called an ancestor buffer, and that which receives is called its descendant buffer. The C/D wafers in an ancestor buffer always have higher grade than those of its descendant buffers. The downgrade relationship among the C/D buffers is a directed graph as shown in Fig. 1. A buffer may have several descendant buffers. Taking C_1 as an example, C_2, C_3, C_4, C_5 and C_6 are its descendant buffers.

Much literature on C/D wafers has been published. Wong and Hood [1] study the impact on cycle time and throughput caused by increasing the number of process monitoring, which consequently increases the demand of C/D wafers. Wu [2] studied the dispatching policy of C/D wafers in the preprocessing stage, where C/D wafers share the tool capacity with product wafers. Popovich et al. [3] developed an automated ordering process to maximize the reuse of test wafers. Chu [4] investigated the policy for setting safety stock level in each C/D buffer. Watanabe et al. [5] studied how to increase the use ratio of reclaimed C/D wafers to reduce the cost.

Some others addressed the problem of downgrading C/D wafers, that is, how many C/D wafers should be delivered to each of its descendant buffers from a particular buffer? Foster et al. [6] established a discrete event simulation program for justifying the effects of various downgrading decisions. Chen and Lee [7] proposed a real-time downgrading policy, called the "push approach". That is, as soon as a particular amount of C/D wafers in a buffer are available for downgrading, they are immediately sent to the descendant buffer, which is heuristically justified as the most needed. Some linear programming models for downgrading C/D wafers, where the desicions are made periodically (e.g., per day), have been developed [8, 9]. In these studies, the developed models consider only the instantaneous WIP level of each buffer at the decision time point, therefore, the obtained solutions may not be optimum in the long run.

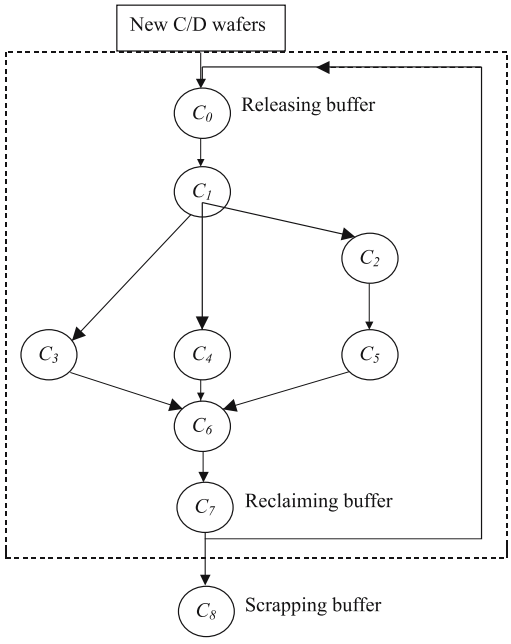

Fig. 1. Downgrade relationships among C/D buffers

By analyzing the cost structure of C/D wafers of several fab sites, the WIP cost only accounts for about 2.4% of the usage cost. Therefore, we assume that the safety stock of C/D wafers at each buffer can be sufficiently prepared in order to absorb the impacts of time-varying properties and unexpected events. Based on this assumption, the downgrade decision problem is simplified. That is, the average daily demand and average daily recycle yield of each buffer are used to characterize the problem. An LP model is accordingly formulated to make the downgrade decision.

The remainder of this paper is organized as follows. Section 2 analyzes the cost structure of C/D wafers and discusses the effects of preparing sufficient safety stocks. Section 3 describes the LP model. An example of the LP model is explained in Sect. 4 and some concluding remarks are stated in Sect. 5.

2 Cost structure of C/D wafers

The cost of C/D wafers in a fab involves three major items: (1) the cost of machine idleness due to lack of C/D wafers, (2) the usage cost of C/D wafers, and (3) the storage cost of C/D wafer (WIP) in shop floor. To analyze the impacts of these three cost items, we interviewed several 8 in fab sites in industry. The relevant cost data of a typical 8 in fab is discussed below.

The throughput of the 8 in fab is 30 000 wafers/month. The C/D wafers released to the fab, which includes both brand-new and reclaimed ones, is about 21 000 wafers/month. The average

WIP of C/D wafers is about 50 000 wafers. The cost of a brand-new C/D wafer is about \$ 70/wafer. The reclaimed cost is about \$ 10/wafer. A C/D wafer in average receives two times the grinding reclaim, that is, a brand new C/D wafer would generate two reclaimed C/D wafers. The brand new C/D wafers released to the fab is therefore $21\,000 \times (1/3) = 7000$ wafers/month. The reclaimed C/D wafers released to the fab is $21\,000 \times (2/3) = 14\,000$ wafers/month. The monthly usage cost of C/D wafers is thus $(7000 \times \$\,70) + (14\,000 \times \$\,10) = \$\,630\,000$/month.

For the WIP, the ratio between brand-new and reclaimed C/D wafers is 1 : 2. Therefore the average cost per C/D wafer WIP is $(\$\,70 \times 1 + \$\,10 \times 2)/3 = \$\,30$. Suppose the monthly interest rate is 1%. The monthly storage cost of C/D wafer WIP is $(\$\,30) \times (50\,000) \times (1\%) = \$\,15\,000$/month, which is about 2.4% of the usage cost.

The cost of machine idleness, due to lack of C/D wafers, is quite high. Therefore, a typical fab requests that the safety stock level of C/D wafers be so high that the machine would not become idle. Taking thickness C/D wafers as an example, the preprocessing for depositing a film takes about 5 h. In the worst case, the lack of thickness C/D wafers would cause an etching machine to be idle for 5 h. The hourly depreciation cost of an etching machine is about \$ 30. Suppose the etching machine is idle for 5 h per month, the idle cost is about \$ 150/month. Yet, the monthly storage cost of keeping a lot (25 pieces) of preprocessed C/D wafers per month is only about $\$\,7.5 = \$\,30$/wafer $\times$ 25 wafers $\times$ (1%). The cost of machine idle is therefore much higher than the WIP cost of C/D wafers.

From the above analysis, we can reasonably assume that the safety stock level of C/D wafers should be so high that the WIP in buffers can always fulfill the time varying demand. Figure 2 shows the profile of a time-varying demand of a C/D buffer, $D(t) = \overline{D} + e(t)$, where $D(t)$ denotes the demand in day t, $\overline{D} = \left(\sum_t D(t) / \sum t\right)$ denotes the average daily demand and $e(t)$ denotes the daily variation from mean. The safety stock level, denoted by s, can then be so prepared, $s = Max_t \{e(t)\}$ to avoid the machine being idle due to lack of C/D wafers. Based on such a safety stock preparation, we can consider the downgrade decision as a static decision problem. That is, the input and output daily flow rates of each C/D buffer are constants and should be balanced.

3 Problem formulation and modeling

3.1 Problem description

In a typical fab, the downgrade relationship among all buffers is a directed graph (Fig. 1). The directed graph involves four types of C/D buffers. Working buffers ($c_1 - c_6$) directly supply C/D wafers to tools. The releasing buffer (c_0) releases brand-new or reclaimed C/D wafers to working buffers. The reclaiming buffer (c_7) reclaims C/D wafers, and sent them to either the releasing buffer or the scrapping buffer. The scrapping buffer (c_8) stores the C/D wafers that cannot be reclaimed further and needs to be scrapped. Working buffers are many in number, while each other type involves only one.

A working buffer stores m categories of C/D wafers, where m denotes the maximum number of cleaning recycles. Category i ($1 \leqslant i \leqslant m$) represents C/D wafers that have received i times of cleaning recycle. A C/D wafer in category i, after receiving one more cleaning recycle, becomes one in category $i + 1$. Any C/D wafer in a particular working buffer, whatever category it belongs to, is regarded as functionally identical or the same in specification. Notice that each cleaning recycle in a certain buffer has a distinct yield rate; the out-of-specification C/D wafers should be forcedly downgraded. Figure 3 shows the various categories of C/D wafers in each working buffer of Fig. 1.

Each working buffer stores C/D wafers with different specification. C/D wafers higher in specification can be downgraded to buffers with lower specification. Downgrade relationships among the working buffers therefore can be established by examining their specifications. The releasing buffer, the highest in specification, can downgrade wafers to any working buffer. The reclaiming buffer, next to the lowest in specification, can receive downgraded wafers from any working buffer. The scrapping buffer, the lowest in specification, only accepts C/D wafers from the reclaiming buffer. A C/D wafer can receive at most n times of grinding reclaim, with a distinct yield rate in each reclaim. Out-of-specification C/D wafers as well as those that cannot be reclaimed further are sent to the scrapping buffer.

Reclaimed C/D wafers, if within specification, are sent back to the releasing buffer. These wafers are regarded as function-

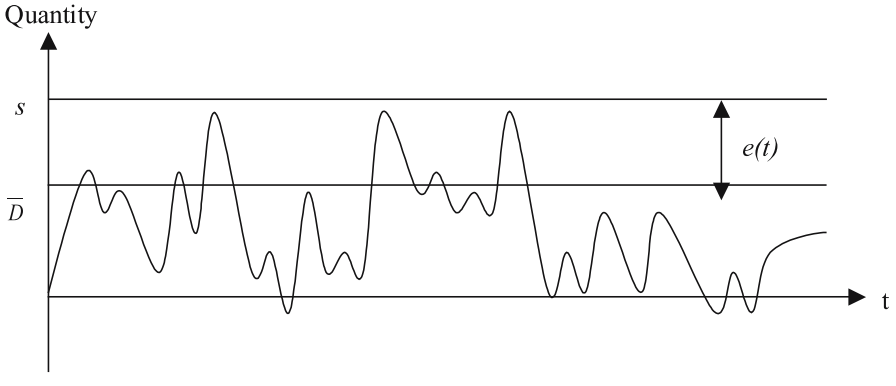

Fig. 2. Time-varying demand and safety stock of a C/D buffer

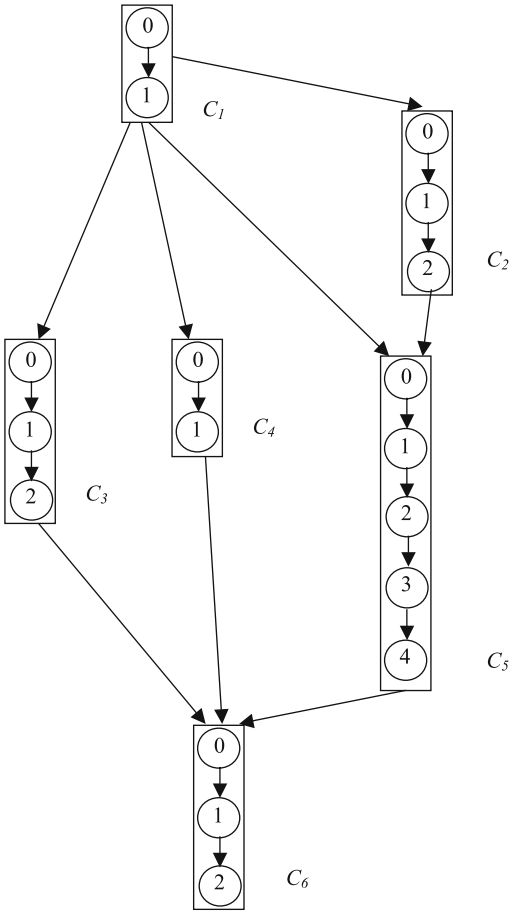

Fig. 3. A working C/D buffer stores several categories of C/D wafers

ally identical to the brand-new buffers. Let the downgrade path between the reclaiming buffer and the releasing buffer be called the feedback path. By eliminating the feedback path, the directed graph becomes one without loop.

The graph without a loop can be denoted by $G = (V, E)$, consisting of a finite set of nodes $V = \{c_0, c_1, \ldots, c_r, c_{r+1}\}$ and a set of arcs E. Herein, a node represents a buffer. An arc represents an ordered pair of two nodes. We denote an arc from c_i to c_j by $c_i \rightarrow c_j$; c_i is the predecessor of c_j and c_j is a successor of c_i. A path from c_i to c_j exists if one can traverse from c_i to c_j through passing k arcs ($k \geqslant 1$). If there is a path from node c_i to node c_j, then c_i is said to be an "ancestor" of c_j, and c_j is said to be a "descendant" of c_i. The diagraph without loop means that any two nodes cannot be ancestor of each other. Node c_0 represents the releasing buffer, c_r the reclaiming buffer, and c_{r+1} the scrapping buffer. Node c_i ($1 \leqslant i \leqslant r-1$) is a working buffer.

Note that the aforementioned diagraph G does not include the feedback path ($c_r \rightarrow c_0$). As a result, the downgrade relationships among all the buffers can be denoted by a diagraph with loop, $S = (G, f)$, where G is the graph without loop and f is the arc $c_r \rightarrow c_0$.

Referring to the diagraph $S = (G, f)$, the downgrade decision problem is to determine the daily flow rate of C/D wafers to be downgraded among buffers so that the brand-new C/D buffers released to the fab is minimized.

3.2 Model

The linear program for the downgrading decision problem can be formulated below:

$$Min \sum_{i=1}^{r-1} N_i$$

s.t.

$$N + Z = \sum_{j=1}^{r-1} N_j + \sum_{j=1}^{r-1} Y_j \tag{1}$$

$$N_j + Y_j + \sum_{i \in P(j)} O_{ij} = X_j^{[0]} \qquad 1 \leqslant j \leqslant r-1 \tag{2}$$

$$X_j^{[k]} = r_j^{[k]} \cdot X_j^{[k-1]} \qquad 1 \leqslant j \leqslant r-1 \tag{3}$$

$$\sum_{k=0}^{m(j)} X_j^{[k]} = D_j \qquad 1 \leqslant j \leqslant r-1 \tag{4}$$

$$\sum_{j \in s(i)} O_{ij} = X_j^{[0]} \qquad 1 \leqslant j \leqslant r-1 \tag{5}$$

$$\sum_{j \in P(r)} O_{jr} = \sum_{k=1}^{n} Z^{[k]} + O_{r,r+1} \qquad 1 \leqslant j \leqslant r-1 \tag{6}$$

$$Z^{[1]} = h^{[1]} \cdot N \tag{7}$$

$$Z^{[k]} = h^{[k]} \cdot Z^{[k-1]} \tag{8}$$

$$O_{r,r+1} = N \tag{9}$$

$$N = \sum_{i=1}^{r-1} N_i \tag{10}$$

$$Z = \sum_{i=1}^{r-1} Z_i \tag{11}$$

$$N_i \geqslant 0; \quad Z_i \geqslant 0; \quad Y_i \geqslant 0; \quad O_{ij} \geqslant 0.$$

In the aforementioned LP model, the decision problem is modeled as a static system. The flow in each buffer or in the fab should be balanced. That is, the input flow rate should equal the output flow rate. Otherwise, the WIP of C/D wafers in the fab will finally increase to infinity or decrease to zero.

The objective function is to minimize the daily usage of brand-new wafers. Constraint Eq. 1 denotes the flow balance relationship in the releasing buffer c_0. The definition of N and Z is given in Eqs. 10 and 11. Constraints Eq. 2 indicate the inputs to a working buffer. Constraints Eq. 3 describe the yield relationship of a cleaning recycle in a working buffer. Constraints Eq. 4 denote that the demand of C/D wafers in a working buffer c_i is supplied by several categories of C/D wafers, with a different number of recycle. Constraints Eq. 5 indicate the output

of a working buffer. The left-hand side describes where the output C/D wafers are downgraded. The right-hand side denotes the sources of the output, which is $X_j^{[0]}$ by considering the flow balance relationship of buffer c_i.

Constraint Eq. 6 denotes the flow balance relationship of the reclaiming buffer c_r. The inputs of c_r are from all working buffers, represented in the left-hand side. The output involves two types of reclaimed C/D wafers, either within specification for reuse or out-of-specification for scrapping. Constraints Eqs. 7 and 8 represent the yield relationships of grinding reclaim. Constraint Eq. 9 denotes that flow balance of the whole fab, that is, all brand-new buffers finally have to go to the scrapping buffer c_{r+1}.

3.3 Model refinement

The aforementioned model can be refined as follows, by reducing the number of constraints.

$$Min \sum_{i=1}^{r-1} N_i$$

s.t.

$$N = \sum_{j=1}^{r-1} N_j \tag{12}$$

$$\left(\sum_{k=1}^{n}\prod_{i=1}^{k} h^{[i]}\right)\cdot N = \sum_{j=1}^{r-1} Y_j \tag{13}$$

$$N_j + Y_j + \sum_{i\in P(j)} O_{ij} = \frac{D_j}{\left(1+\sum_{k=1}^{m(j)}\prod_{i=1}^{k} r_j^{[i]}\right)} \quad 1 \leqslant j \leqslant r-1 \tag{14}$$

$$\sum_{j\in s(i)} O_{ij} = \frac{D_j}{\left(1+\sum_{k=1}^{m(j)}\prod_{i=1}^{k} r_j^{[i]}\right)} \quad 1 \leqslant j \leqslant r-1 \tag{15}$$

$$\sum_{j\in P(r)} O_{jr} = \left(\sum_{k=1}^{n}\prod_{i=1}^{k} h^{[i]}+1\right)\cdot N \quad 1 \leqslant j \leqslant r-1 \tag{16}$$

$$O_{r,r+1} = N. \tag{17}$$

Considering constraints Eqs. 7 and 8, we can derive $Z^{[K]} = \prod_{i=1}^{k} h^{[i]} \cdot N$ and then $Z = \sum_{k=1}^{n}\prod_{i=1}^{k} h^{[i]} \cdot N$. Constraint Eq. 1 can therefore be decomposed into constraints Eqs. 10 and 11, which respectively models the brand-new wafers and reclaimed wafers released from c_0.

Likewise, by considering constraints Eqs. 3 and 4, we can derive $X_i^{[k]} = \prod_{i=1}^{k} r_j^{[i]} \cdot X_j^{[0]}$, subsequently $\left(1+\sum_{k=1}^{m(j)}\prod_{i=1}^{k} r_j^{[i]}\right)\cdot X_j^{[0]} = D_j$, and finally $X_i^{[0]} = \frac{D_j}{\left(1+\sum_{k=1}^{m(j)}\prod_{i=1}^{k} r_j^{[i]}\right)}$. Constraint Eq. 2 can then be replaced by constraints Eq. 14, and constraint Eq. 5 by Eq. 15. Notice that the right-hand side of constraint Eq. 5 equals $X_i^{[0]}$, due to the flow balance relationship. Constraint Eq. 6 can be replaced by constraint Eq. 16 by considering constraint Eq. 9 as well as $Z = \sum_{k=1}^{n}\prod_{i=1}^{k} h^{[i]} \cdot N$.

4 Example

The refined LP model is explained by the example as shown in Fig. 1, which involves nine buffers, one releasing buffer (c_0), six working buffers (c_1–c_6), one reclaiming buffer (c_7), and one scrapping buffer (c_8). The daily demand and the yield of recycle of each working buffer are shown in Table 1. The yield information of the reclaiming buffer is $n = 2$, $h^{[1]} = 0.9$, and $h^{[2]} = 0.8$.

The LP model of the example is described below.

$$\begin{aligned}
&Min\ N_1+N_2+N_3+N_4+N_5+N_6\\
&N-N_1-N_2-N_3-N_4-N_5-N_6=0\\
&(0.9+0.9\times0.8)N-Y_1-Y_2-Y_3-Y_4-Y_5-Y_6=0\\
&N_1+Y_1=65/(1+0.9)\\
&N_2+Y_2+O_{12}=38/(1+0.9+0.9\times0.8)\\
&N_3+Y_3+O_{13}=26/(1+0.9+0.9\times0.8)\\
&N_4+Y_4+O_{14}=36/(1+0.9)\\
&N_5+Y_5+O_{15}+O_{25}\\
&\quad=110/(1+0.9+0.9\times0.8+0.9\times0.8\times0.7\\
&\qquad+0.9\times0.8\times0.7\times0.6)\\
&N_6+Y_6+O_{16}+O_{26}+O_{36}+O_{46}+O_{56}\\
&\quad=48/(1+0.9+0.9\times0.8)\\
&O_{12}+O_{13}+O_{14}+O_{15}+O_{16}+O_{17}=65/(1+0.9)\\
&O_{25}+O_{26}+O_{27}=38/(1+0.9+0.9\times0.8)\\
&O_{36}+O_{37}=26/(1+0.9+0.9\times0.8)\\
&O_{46}+O_{47}=36/(1+0.9)\\
&O_{56}+O_{57}=110/(1+0.9+0.9\times0.8+0.9\times0.8\times0.7\\
&\qquad+0.9\times0.8\times0.7\times0.6)\\
&O_{67}=48/(1+0.9+0.9\times0.8)\\
&O_{17}+O_{27}+O_{37}+O_{47}+O_{57}+O_{67}=(1+0.9+0.9\times0.8)N\\
&O_{78}=N\\
&N_j\geqslant0,\quad Y_j\geqslant0,\quad O_{ij}\geqslant0
\end{aligned}$$

We use software package CPLEX to solve the problem. The optimum solution of the LP model is multiple. The minimum daily flow rate of C/D wafers (N) is 23.3 wafers/d. Table 2 presents one of the optimum solutions, which is provided by CPLEX.

Table 1. Demand and yield of recycle at working buffer c_j

Buffer	c_1	c_2	c_3	c_4	c_5	c_6
D_j	65	38	26	36	110	48
$m(j)$	1	2	2	1	4	2
$r_i^{[1]}$	90%	90%	90%	90%	90%	90%
$r_i^{[2]}$	–	80%	80%	–	80%	80%
$r_i^{[3]}$	–	–	–	–	70%	–
$r_i^{[4]}$	–	–	–	–	60%	–

Table 2. Downgrade decision of an optimum solution

From \ To	C_1	C_2	C_3	C_4	C_5	C_6	C_7
C_0	100%						
C_1		42.4%	29%	28.6%			
C_2					100%		
C_3							100%
C_4							100%
C_5						57%	43%
C_6							100%
C_7	29%			24.3%	46.7%		

Table 2 shows that the releasing buffer c_0 downgrades the C/D wafers only to c_1. Buffer c_1 downgrades a certain percentage of C/D wafers to c_2 (42.4%), c_3 (29%) and c_4 (28.6%) but downgrades nothing to c_5, c_6 and c_7. Notice that the last row in Table 2 indicates the output flow of reclaimed wafers (Y_i) from buffer c_0, which is also the output from the reclaiming buffer c_7. The fab can use the downgrade percentage of each buffer, provided by the obtained solution, to control the daily flow of C/D wafers to minimize the long-term usage of C/D wafers.

5 Concluding remarks

An LP model for the decision of downgrading C/D wafers is proposed. The model assumes that the safety stock is so highly prepared that the decision becomes a static flow balance problem. The system addressed in the decision problem is a diagraph, where each node represents a buffer. For each buffer, the input flow rate should-use-dialog-box-p equal the output flow rate. The assumption of sufficient safety stocks has been reasonably justified by analyzing the cost structure of C/D wafers through the interview of several fab sites in industry.

The LP model may provide multiple optimum solutions, which are infinite in number and can be characterized by a solution space. Future work of this research involves identifying the best one from the solution space, by additionally considering the safety stock costs, transportation costs, and fab space constraints.

Acknowledgement The authors would like to thank the Taiwan Semiconductor Manufacturing Corp. for characterizing this research problem.

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