Foreword
Special Issue on Advanced Technology for Ultra-Low Power Electronic Devices

ELECTRONIC devices consume a large amount of energy globally, and this is projected to accelerate in the near future with greater societal connectivity and cloud storage. To meet power saving goals, both the DC leakage power (P_{DC}) and switching AC power (P_{AC}) consumption of future electronics must be lowered. Electronic materials play a central role for ultra-low power electronics. To lower the transistor's gate and source-drain leakage current, high-κ dielectric plus metal gate technologies and FinFET structures have been implemented in CMOS. The scaling of supply voltage (V_{DD}) is an effective way to lower P_{AC}, where the transistor's current degradation can be compensated by using high mobility channel materials, such as p-channel Ge, and n-channel InGaAs; high-mobility metal-oxide semiconductors, or two-dimensional (2D) materials. The ultimate V_{DD} reduction is limited by the transistor's turn-on slope. One proposed solution is the Tunnel FET, where carriers are injected by band-to-band-tunneling directly to the channel. Another method to reach <60 mV/dec turn-on slope is to integrate piezoelectric or ferroelectric materials into MOSFETs. These new electronic materials can also be used for ultra-low power memory application beyond existing DRAM thereby enabling technology for processor-in-memory and brain mimicking chips.

Our intent with this special issue was to consolidate the latest advances on advanced technology for ultra-low power electronic devices. The call for papers invited submissions that address advances in process technologies and materials, devices concepts using new materials, device design, measurements and electrical characterization, and modeling and simulations.

The special issue begins with four invited papers to provide progress and perspective in the development of ultra-low power electronic devices. Jesus A. del Alamo, MIT, and Sorin Cristoloveanu, IMEP-LAHC, summarize recent progress and current directions in III-V FETs and sharp-switching devices, respectively, to lower the switching power in FETs. Tak Ning, IBM, considers SOI lateral bipolar transistors to reach ultra-low power system. Simon Deleonibus, CEA, LETI, discusses the challenge of energy and variability efficient era for ultra-low power system. The contributed papers are focused using material and process technology, device design, and simulation to address the power consumption in logic, memory and display devices. The special issue meets our goal of providing a consolidation of the latest advancements in ultra-low power electronic devices. The papers also show that this field is vital for future electronics.

PAUL R. BERGER, *Guest Editor*
Ohio State University
Columbus, OH, USA

ALBERT CHIN, *Guest Editor*
National Chiao Tung University
Hsinchu, Taiwan

AKIRA NISHIYAMA, *Guest Editor*
Toshiba
Japan

MEIKEI IEONG, *Guest Editor*
ASTRI
Hong Kong

Date of current version 23 August 2016.
Digital Object Identifier 10.1109/JEDS.2016.2597518

Paul R. Berger received the Ph.D. degree in electrical engineering from the University of Michigan, Ann Arbor. He is currently a Professor with Ohio State University. He is also a Distinguished Visiting Professor with the Tampere University of Technology. He was with Bell Laboratories, Murray Hill, NJ, USA, the University of Delaware, the Max-Planck Institute for Polymer Research, Mainz, Germany, Cambridge Display Technology, Ltd., Cambridge, U.K., and Interuniversity Microelectronics Center, Leuven, Belgium. He was a recipient of the NSF CAREER Award, the DARPA ULTRA Sustained Excellence Award, the Lumley Research Awards, the Faculty Diversity Excellence Award, and the Outstanding Engineering Educator, representing the entire State of Ohio and all engineering disciplines as bestowed by the Ohio Society of Professional Engineers. He has been on the Program and Advisory Committees of numerous conferences, including the IEDM, DRC, EMC, ISDRS, CSTIC, CPTIC, and IFSOE meetings. He is currently the Chair of the Columbus IEEE EDS/Photonics Chapter and the Faculty Advisor to Ohio State's IEEE Student Chapter and the IEEE Graduate Student Body, which is the first in the world. He is the Faculty Advisor to the Solar Education and Outreach Club and the Recruitment and Retention Initiative for Successful Engineers for minority engineers. He is currently the IEEE EDS Distinguished Lecturer. He is a Senior Member of OSA.

Albert Chin received the Ph.D. degree from the University of Michigan. He was with AT&T Bell Labs, General Electric E-Lab, and Texas Instruments SPDC.

He is a Pioneer on low DC-power high-κ CMOS, high-κ planar Flash memory, high mobility Ge-On-Insulator, low AC-power 3D IC, high RF power asymmetric-MOSFET, Si THz devices, and resonant-cavity photo-detector. He has co-authored over 450 papers and seven highly cited papers.

Dr. Chin served as the Subcommittee Chair and the Asian Arrangements Chair of the IEDM Executive Committee. He is an IEEE Fellow, Optical Society of America Fellow and Asia-Pacific Academy of Materials Academician. He has served as an Editor of the IEEE ELECTRON DEVICE LETTERS and the IEEE ED Society Technical Committee Chairs on Electronic Materials from 2014 to 2015 and Compound Semiconductor Devices & Circuits since 2016.

Akira Nishiyama received the Ph.D. degree from Waseda University. In 1985, he joined the Research and Development Center, Toshiba Corporation. Since then, he has been engaging in research on high speed CMOS devices such as high-k gate dielectrics, metal gate electrodes as well as low power consumption Ge MOS transistors. He was a Visiting Scientist with the FOM Institute for Atomic and Molecular Physics, Amsterdam, from 1993 to 1994. He worked as a Visiting Professor with the Tokyo Institute of Technology from 2009 to 2015. He is currently a Chief Fellow and an Assistant Director of the LSI & Storage field of corporate R&D Center, Toshiba Corporation.

He was an Editor of the *Japanese Journal of Applied Physics* from 2006 to 2008. He has been serving as a member of organizing committee as well as technical program committee of several international conferences. He is a fellow of the Japan Society of Applied Physics and currently the Vice Chair of the IEEE EDS Japan chapter.

Meikei Ieong (SM'01) received the B.S. degree in electrical engineering from National Taiwan University, Taipei, Taiwan, in 1991, the M.S. and Ph.D. degrees in electrical and computer engineering from the University of Massachusetts, Amherst, in 1993 and 1996, respectively, and the M.B.A. degree from the Sloan Fellows Program, Massachusetts Institute of Technology in 2013.

He is currently a Chief Technology Officer with Hong Kong Applied Science and Technology Research Institute. He was the Vice-President of TSMC Europe and the Program Director with TSMC Research, Taiwan. He held various engineering and management positions with IBM, including a Senior Manager with IBM T. J. Watson Research Center, Yorktown, NY, USA. He was a recipient of the IBM Technical Achievement and Corporate awards. He was elected as a Master Inventor with IBM Research.

Mr. Ieong held an Adjunct Associate Professor position with the Department of Electrical Engineering, Columbia University, NY, USA, in 2001. He was the General Chairman of the IEEE International Electron Devices Meeting. He has been serving as an Editor for the IEEE TRANSACTIONS ON ELECTRON DEVICES since 2010 and the Chair of the IEEE EDS Education Award Committee since 2013. He has published over 100 papers in referred journals and conference proceedings and holds over 80 patents. He also speaks frequently at international conferences and seminars.