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High Performance Metal-Gate/High-κ GaN MOSFET With Good Reliability for Both Logic and Power Applications

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ABSTRACT The gate-recessed GaN MOSFET on a Si substrate is demonstrated to achieve a record highest normalized transistor current (μC_{ox}) of 335 μA/V^2 (410 mA/mm at $L_G = 5$ μm and only $V_G = 4$ V), I_{ON}/I_{OFF} of 9 orders of magnitude, small 79 mV/dec sub-threshold slope, a low oxide/GaN interface trap density of 1.2×10^{10} eV^{-1}/cm^2, a low on-resistance of 17.0 Ω-mm, a high breakdown voltage of 720–970 V, and excellent reliability of only 40 mV ΔV_T after 175 °C 1000 s stress at maximum drive current. Such excellent device integrities are due to the high-κ gate dielectric and the high conduction band offset (ΔE_C) of SiO_2/GaN. From the calculation results of self-consistent Schrödinger and Poisson equations, the good reliability of GaN MOSFET is related to the confined carrier density within the GaN channel, which is in sharp contrast to the strong wave-function penetration into the high-trap density AlGaN barrier in the AlGaN/GaN HEMT.

INDEX TERMS GaN, MOSFET, high-κ, reliability, interface.

I. INTRODUCTION

The ideal transistor requires low off-state current (I_{OFF}) to save power, high on-current (I_{ON}) to increase the circuit speed, small turn-on sub-threshold swing (*SS*) to lower switching power, small supply voltage (V_{DD}) for low power operation, versatile high V_{DD} for power electronics and communication applications, and good reliability. To reach these goals simultaneously, both high mobility and wide energy-bandgap materials are the key solution [1]. Besides, the wide bandgap channel MOSFET has new application for logic CMOS, because it can lower the increased I_{OFF} in the highly scaled deep X-nm FinFET by quantum-mechanical direct tunneling [1].

Among available materials, the GaN is one of the ideal candidates with the merits of high mobility, high saturation velocity, and high breakdown field [1]–[17]. Thus, excellent RF power performance has been realized by AlGaN/GaN HEMT [14]–[17]. Yet the GaN MOSFET [1]–[13] has the positive threshold voltage (V_T) and lower leakage current than HEMT, which is more preferable for system application. Besides, the AlGaN barrier in AlGaN/GaN HEMT is difficult to scale down due to the gate leakage current, which limits further improvement of gate capacitance and transistor's drive current.

Previously, using a high-κ gate dielectric, we reported high I_{ON} and reasonable breakdown voltage (V_{BD}) in gate-recessed GaN MOSFET [11]. However, the very poor I_{OFF} and *SS* are the major drawbacks. In this paper, we report a normally-off gate-recessed GaN MOSFET on Si substrate, using the HfAlO/SiO_2 gate dielectric. In addition to the reached highest normalized drive current ($I_{ON,nor}$) of 335 μA/V^2, 10^9 I_{ON}/I_{OFF}, small *SS* of 79 mV/dec, a low oxide/GaN interface trap density (D_{it}) of 1.2×10^{10} eV^{-1}/cm^2, a positive V_T of 0.55 V, and a high V_{BD} of 720∼970 V were achieved simultaneously. Besides, excellent reliability of only 40 mV ΔV_T was measured after 175°C 1000 sec stress at the maximum drive current. The excellent reliability is further supported by the quantum-mechanical

simulation, where the electron wave-function is confined in GaN channel and quite different from the severe wave-function penetration into the AlGaN barrier in a HEMT. This device has steep *SS* comparable with metal-gate/high-κ Si MOSFET, with much better I_{ON}/I_{OFF} and much higher V_{BD}.

II. EXPERIMENTS

The device structure in Fig. 1 has a low-temperature grown AlGaN buffer on (111) Si wafer, a 1-μm GaN active layer, a 30-nm AlGaN barrier, and a 2-nm GaN. A thin 2.5-nm thick AlN etching stop layer was inserted in AlGaN barrier to improve the etching selectivity [13], [18]. Then mesa isolation and gate region were recess etched by using BCl_3/Cl_2 RIE. A thin 3-nm thick AlGaN layer beneath the AlN layer was used to prevent RIE damage to GaN channel. The gate dielectric of 1-nm SiO_2 and 5-nm high-κ HfAlO were formed by ALD [19]–[23]. Then the gate dielectric was annealed at 400 °C for 5 min under oxygen ambient, to improve the quality of gate oxide and oxide/GaN interface [20]–[23]. In comparison with previous PVD-deposited SiO_2, the *in-situ* formed SiO_2 shows much improved interface trap density. The interfacial SiO_2 not only lowers the interface reaction but also increases the oxide/GaN barrier height [11], [12], [23]. After opening contact window, the ohmic contacts were formed by Ti/Al/Ti/Au deposition and rapid thermal annealing (RTA) at 850 °C for 30 sec in a nitrogen ambient. Then high work-function Pt/Au was deposited and patterned to form the metal-gate with a size of 5-μm × 100-μm. An asymmetric drain and source was used to improve the V_{BD} [11], [24]. For comparison, the control AlGaN/GaN HEMT devices, without the AlN layer, were also made. The $C-V$ data were measured by using Agilent E4980A at a step voltage of 0.2 V and sweep time of 110 to 88 ms.

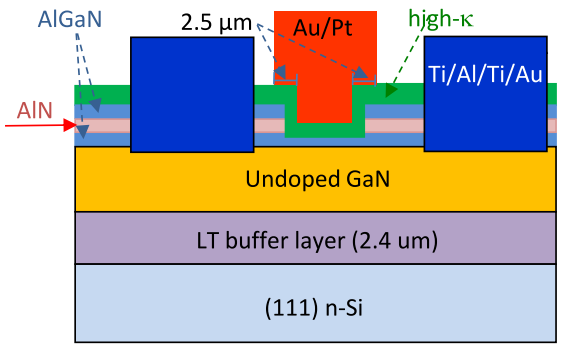

FIGURE 1. The schematic device structure of gate-recessed metal-gate/high-κ GaN MOSFET.

III. RESULTS AND DISCUSSION

The unique feature of GaN MOSFET for logic application is its large bandgap that increases the quantum-mechanical tunneling barrier height from source to drain [1]. As the FinFET scales to deep X-nm region, the I_{OFF} is limited by direct tunneling current density (J_{DT}) under electrical channel length, without considering the drain depletion. The J_{DT} can be approximately expressed as [1], [25]:

$$J_{DT} = \frac{BE^2}{\phi_b\left(1-\sqrt{1-qEt_b/\phi_b}\right)^2} \times \exp\left\{-\frac{C\sqrt{m*}\phi_b^{3/2}}{E}\left[1-\left(1-\frac{qEt_b}{\phi_b}\right)^{3/2}\right]\right\} \quad (1)$$

The B and C are the constant; ϕ_b, E, t_b, and m^* are the tunneling barrier height, electric field, thickness, and effective mass, respectively. The conventional method to lower the J_{DT} is to decrease the tunneling E field, where the lowered drain current (I_D) can be compensated by the high mobility channel. Unfortunately, the high mobility Ge [23] and InGaAs has much smaller bandgap and ϕ_b than Si that increase J_{DT} exponentially. The better method is to increase ϕ_b, decrease E field, and use high mobility channel at the same time, which can be realized by using high-mobility wide-bandgap material such as GaN.

Fig. 2 plots the ϕ_b dependence on J_{DT} for Si and GaN MOSFET with a 7 nm electrical channel length. The J_{DT} can be lowered by increasing the ϕ_b using highly p^+ channel doping, where the maximum ϕ_b is close to bandgap energy. However, the random dopant variation is a severe issue in such small dimension. To avoid this problem, the channel doping can be lowered under the fully depleted condition. Unfortunately, the maximum ϕ_b decreases to half of the bandgap energy that increases the J_{DT} exponentially. Besides, the drain-induced barrier lowering (DIBL) will also lower the ϕ_b. The source-drain dopant diffusion into channel will further decrease the electrical t_b with an exponential dependence on J_{DT}. As shown in Fig. 2, the J_{DT} can be lowered by several orders of magnitude if the Si is replaced by GaN. Nevertheless, the lacking of high performance GaN MOSFET on Si substrate is the major challenge for this technology.

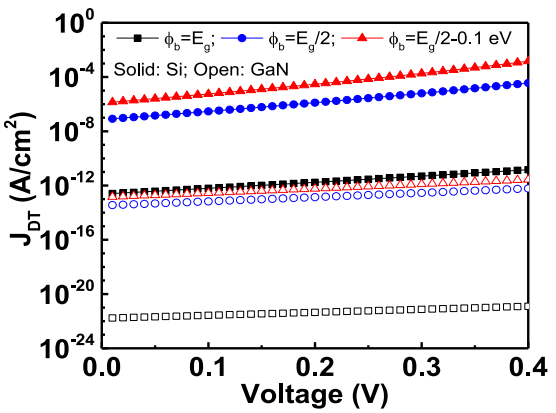

FIGURE 2. J_{DT} versus ϕ_b for Si and GaN MOSFET with a 7-nm electrical channel length. The ϕ_b of E_g, $E_g/2$, and $E_g/2$-0.1 eV is related to highly p^+ channel doping, fully depleted channel, and further 0.1 V DIBL lowering, respectively.

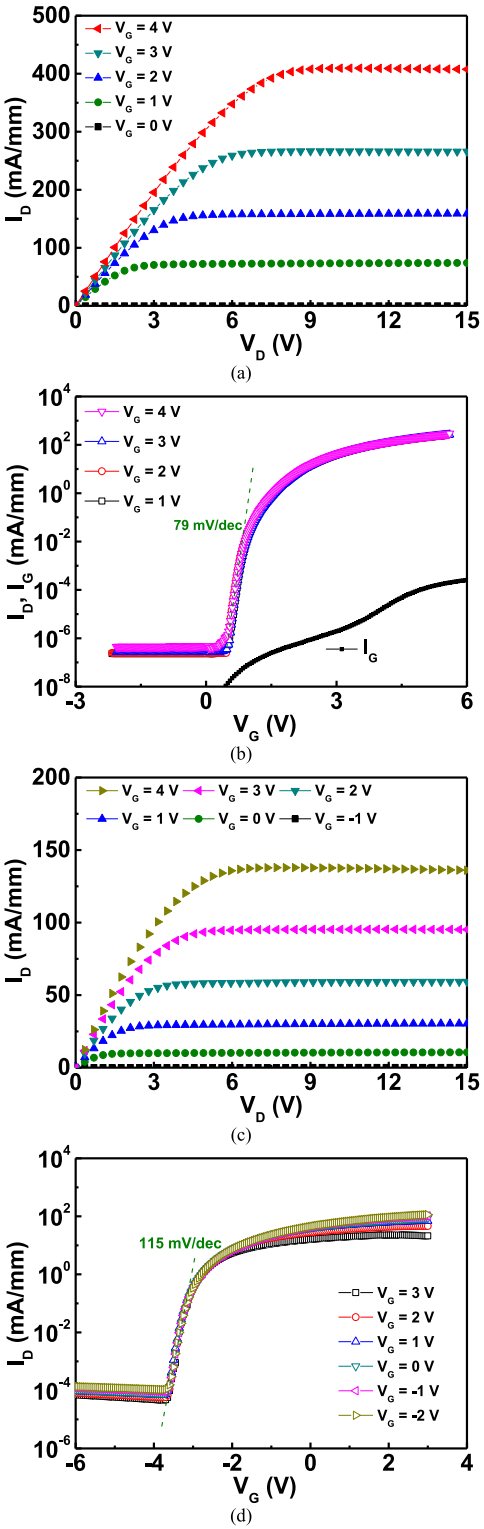

FIGURE 3. **(a) $I_D - V_D$ and (b) $I_D - V_G$ and $I_G - V_G$ characteristics of gate-recessed metal-gate/high-κ GaN MOSFETs; (c) $I_D - V_D$ and (d) $I_D - V_G$ characteristics of AlGaN/GaN HEMT with the similar epitaxial material structure but without the extra AlN layer.**

Figs. 3(a) and 3(b) show the $I_D - V_D$ and $I_D - V_G$ data of gate-recessed metal-gate/high-κ GaN MOSFETs, respectively. The measured gate current (I_G) is orders of magnitude lower than I_D. The high-κ MOSFET has a very high I_{ON} of 410 mA/mm at $L_G = 5$ μm and $V_G = 4$ V, or record highest $I_{ON,nor}$ of 335 μA/V^2, a small R_{on} of 17 Ω-mm, a very low *SS* of only 79 mV/dec, an I_{ON}/I_{OFF} of 10^9, and a positive V_T of 0.55 V. The $I_{ON,nor}$ is normalized by gate size and gate overdrive of $V_G - V_T$:

$$I_{ON,nor} = I_{ON} * (2L_G/W_G) / (V_G - V_T)^2 = \mu C_{ox} \quad (2)$$

The L_G, W_G, V_G, C_{ox}, and μ are the gate length, width, voltage, gate capacitance, and mobility, respectively. For low-power logic CMOS application, the steep *SS*, comparable with metal-gate/high-κ Si MOSFET [19], is essential to turn on the transistor fast; the even better I_{ON}/I_{OFF} or I_{OFF} than Si MOSFET is vital to improve the leakage power consumption. For power application, the high I_{ON} is important to improve the power density, chip size and cost of power module for system application [24]. The low V_T is required to integrate with the low V_{DD} of Si sub-μm CMOS control IC [11].

For comparison, the $I_D - V_D$ and $I_D - V_G$ characteristics of AlGaN/GaN HEMT were also shown in Figs. 3(c) and 3(d), respectively. Here the HEMT has the similar epitaxial material structure with the gate-recessed GaN MOSFET but without the extra AlN layer. The AlGaN/GaN HEMT has a standard device performance of −3 V V_T, 115 mV/dec *SS*, and 10^{-4} mA/mm I_{OFF} but are significantly worse than those of MOSFET. It is important to notice that the $I_{ON,nor}$ of control AlGaN/GaN HEMT is comparable with or slightly better than the published data in [14]–[17]. It is essential to notice that the battery in mobile communication only provides a positive voltage and requires extra circuit to generate the negative V_G bias. Although the high mobility is the merit of HEMT, the gate-recessed MOSFET has 5 times higher $I_{ON,nor}$ than that of HEMT. Thus, both gate capacitance ($C_{ox} = \varepsilon_0\kappa/t$) and mobility at high V_G, or high effective field (E_{eff}), should be considered to reach the high $I_{ON,nor}$. Besides, the mobility in a transistor decreases rapidly with increasing V_G and E_{eff} [19]–[23], and therefore the HEMT mobility operated at high V_G is much lower than the Hall mobility measured at a low electric field. The small C_{ox} of thick AlGaN gate dielectric in HEMT is another limiting factor to cause the low $I_{ON,nor}$.

Figs. 4(a) and 4(b) show the $G_m - V_G$ characteristics of gate-recessed metal-gate/high-κ GaN MOSFETs and AlGaN/GaN HEMT, respectively. The G_m data were obtained from the $I_D - V_G$ curves of Figs. 3(b) and 3(d). For gate-recessed metal-gate/high-κ GaN MOSFET, the G_m increases with increasing V_G that is typical for MOSFET device. In contrast, the G_m of AlGaN/GaN HEMT increases initially with increasing V_G but gradually decreases at higher V_G values, which is due to the small AlGaN/GaN barrier to cause carrier leakage. The peak G_m values are 112 and 25 mS/mm for metal-gate/high-κ GaN MOSFET and AlGaN/GaN HEMT, respectively. The very high G_m is the merit of metal-gate/high-κ MOSFET as compared with HEMT.

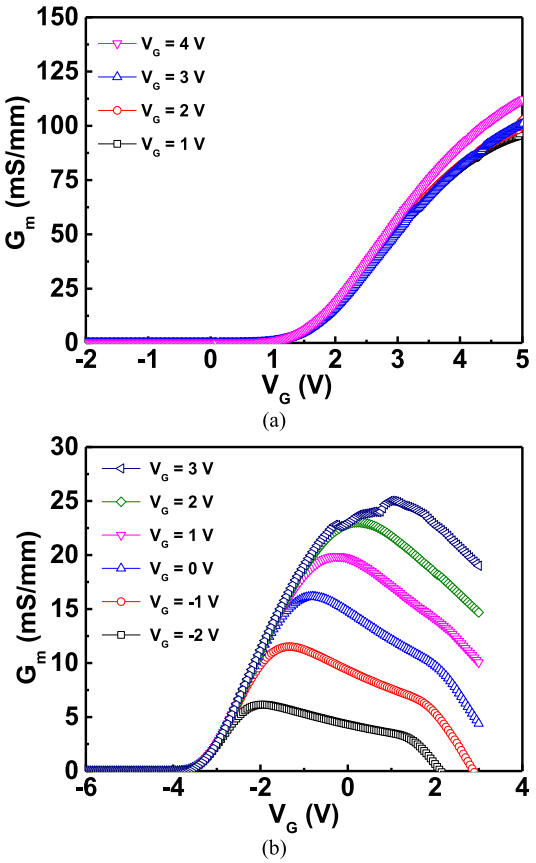

FIGURE 4. $G_m - V_G$ characteristics of (a) gate-recessed metal-gate/high-κ GaN MOSFETs, and (b) AlGaN/GaN HEMT without the extra AlN layer.

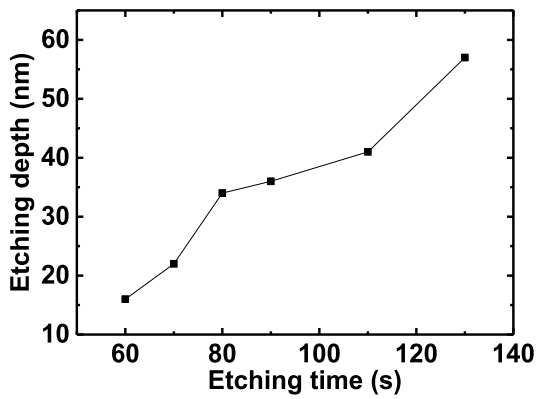

FIGURE 5. The RIE etching depth as a function of etching time of the AlGaN/GaN HEMT structure.

One reason to reach the excellent I_{OFF} compared with previous gate-recessed GaN MOSFET [11] is due to the good RIE etching controllability. The gate over recess can cause device failure, while under recess leads to negative V_T and high I_{OFF}. Fig. 5 shows the etching depth versus time. The etching rate is slower when the AlGaN is etched to AlN. However, the AlN thickness is limited to 3 nm, because the thick AlN will cause the high strain, interface

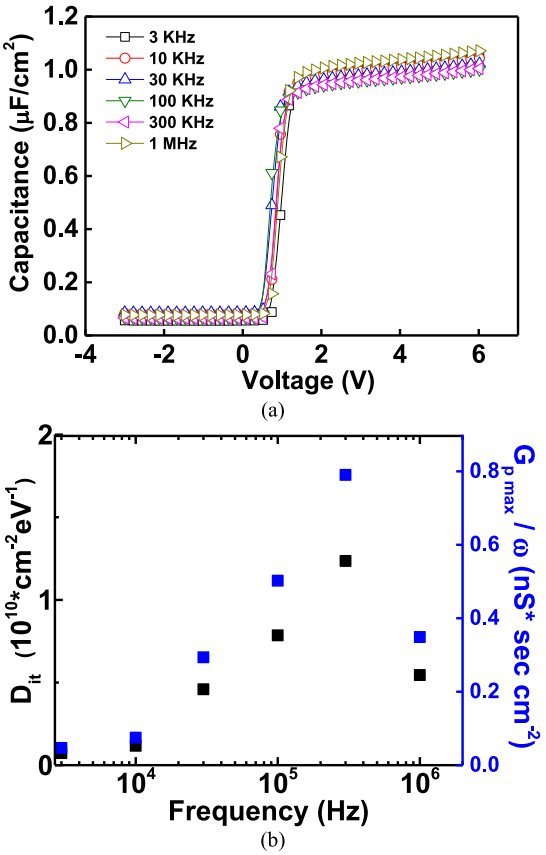

FIGURE 6. Frequency dependent (a) $C_G - V_G$ characteristics and (b) D_{it} and G_p/ω of gate-recessed metal-gate/high-κ GaN MOSFETs.

roughness, and poor mobility. Careful RIE etching control is still needed even with AlN layer.

We further measured the frequency (f)-dependent $C_G - V_G$ characteristics of GaN MOSFET. As shown in Fig. 6(a), little change of $C_G - V_G$ slopes from depletion to accumulation can be found as increasing f from 3 kHz to 1 MHz. These results indicate the good oxide/GaN interface. The $C - V$ curves of metal-gate/high-κ GaN MOSFETs, swept between −4 and 7 V and measured at 3 kHz to 1 MHz, has small hysteresis of 0.25∼0.08 V, indicating the good high-κ dielectric quality. We also used the conductance (G_p) method to extract the D_{it}. Fig. 6(b) shows the D_{it} and G_p/ω as a function of f. The D_{it} is obtained from the G_p/ω peak [26]–[29], where ω is the angular frequency. A low D_{it} of 1.2×10^{10} eV^{-1}/cm^2 is obtained, the lowest reported data among GaN MOSFET [2]–[13]. Because of the large high-κ gate capacitance and the small D_{it}, the D_{it} extraction by conductance method is accurate due to $C_{ox} > qD_{it}$ [29]. Such a low D_{it} value is also consistent with the measured small SS of only 79 mV/dec. In high-κ/Si [22] and high-κ/Ge MOSFETs [23] without interfacial SiO_2, the interface reaction largely degrades the D_{it}. The excellent D_{it} in this work is due to the SiO_2 to lower high-κ and GaN reaction.

The high voltage operation and good reliability are the necessary characteristics for power device. Fig. 7 shows

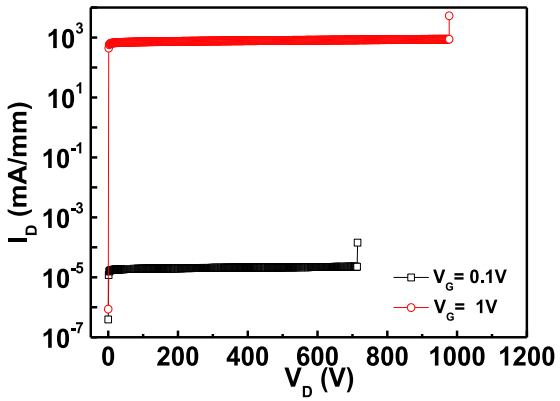

FIGURE 7. The V_{BD} characteristics of gate-recessed high-κ GaN MOSFET.

the $I_D - V_D$ characteristics of gate-recessed high-κ GaN MOSFET. A high V_{BD} of 720 and 970 V are obtained at V_G of 0.1 and 1 V, indicating the breakdown is sensitive to defects in GaN. These V_{BD} values are high enough for 600 V system application.

Fig. 8(a) is the I_D-stress versus time characteristics of gate-recessed metal-gate/high-κ MOSFET during maximum I_{ON} ($I_{ON,max}$) at $V_G = 4$ V, $V_D = 20$ V and elevated 175°C stress. The I_{ON} has only slight variation during stress, but the I_{OFF} becomes better with increasing stress time. The I_{ON}/I_{OFF} improves from initial 10^9 to 10^{10} after stress, which may be related to the electrons trapping/de-trapping inside GaN. Fig. 8(b) shows the $I_D - V_G$ characteristics before and after stress at 175°C and $I_{ON,max}$ for 1000 sec. The ΔV_T after 175°C stress is only 40 mV, which is the best data among reported GaN MOSFET [2]–[13]. This result further supports the excellent gate oxide and MOS interface, consistent with the small *SS* and very low I_{OFF}. For comparison, the $I_D - V_G$ hysteresis of fresh device before bias-temperature stress is also plotted in Fig. 8(c), which has a small ΔV_T of 15 mV.

To further investigate such excellent stress reliability, the self-consistent Schrödinger and Poisson equations were solved for both AlGaN/GaN HEMT and gate-recessed metal-gate/high-κ GaN MOSFET. Figs. 9(a) and 9(b) are the calculated data of electron wave-function and carrier density distributions for AlGaN/GaN HEMT, respectively. The polarization induced a thin layer of charge at the interface [30] with a two-dimensional electron gas (2DEG) density of 1×10^{13} cm^{-2} that agrees with the Hall measurement data well. At this high 2DEG density, electron wave-functions of ground and two excited states were populated, but penetrates into AlGaN.

The wave-function penetration into AlGaN barrier can be observed clearly from the carrier density distribution, which is due to the small conduction band offset (ΔE_C) of 0.34 eV and the elevated quantum energy levels. It is well known the Al-content compound semiconductor such as AlGaAs, InAlAs, and AlGaN have high trap densities. During the

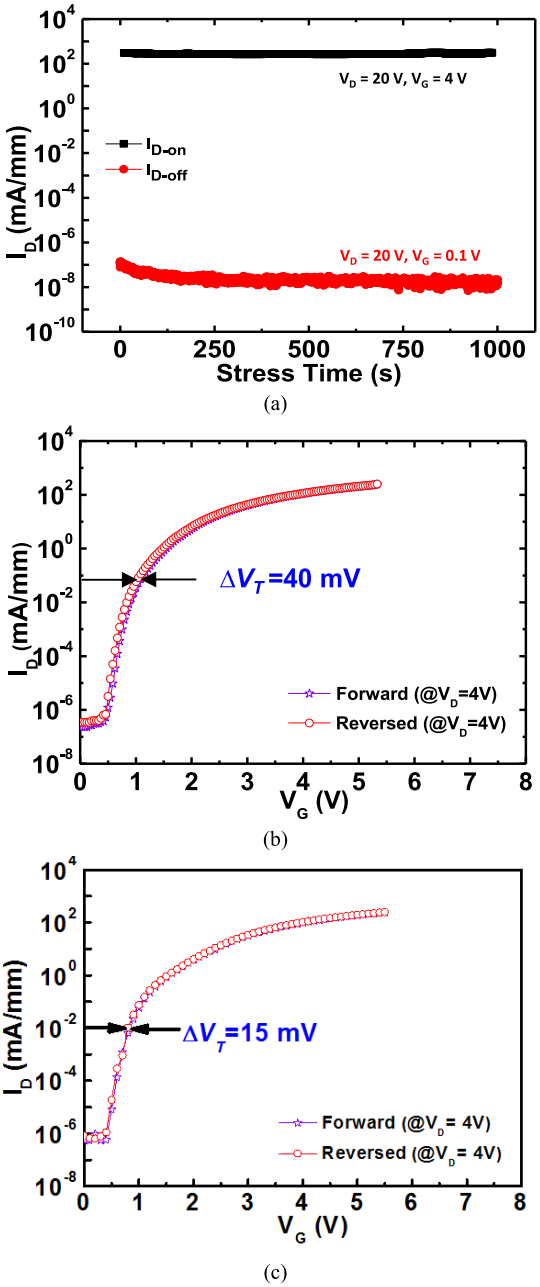

FIGURE 8. (a) The I_D as a function of time during stress at $I_{D,max}$ and 175°C for 1000 sec. (b) Forward and reversed $I_D - V_G$ sweep curves after 1000 sec stress at 175°C and $V_D = 20$ V. (c) The fresh device before bias-temperature stress.

device operation, the energetic channel hot electrons can be easily trapped inside the AlGaN defect centers and cause device performance degradation.

Figs. 9(c) and 9(d) present the calculated data of electron wave-function and carrier density distributions for gate-recessed metal-gate/high-κ GaN MOSFET, respectively. At an inversion density of 1×10^{13} cm^{-2} induced by MOS V_G, the ground and two excited states were also found. Although the quantum confinement lifts the energy levels, the electron wave-functions are still confined within the

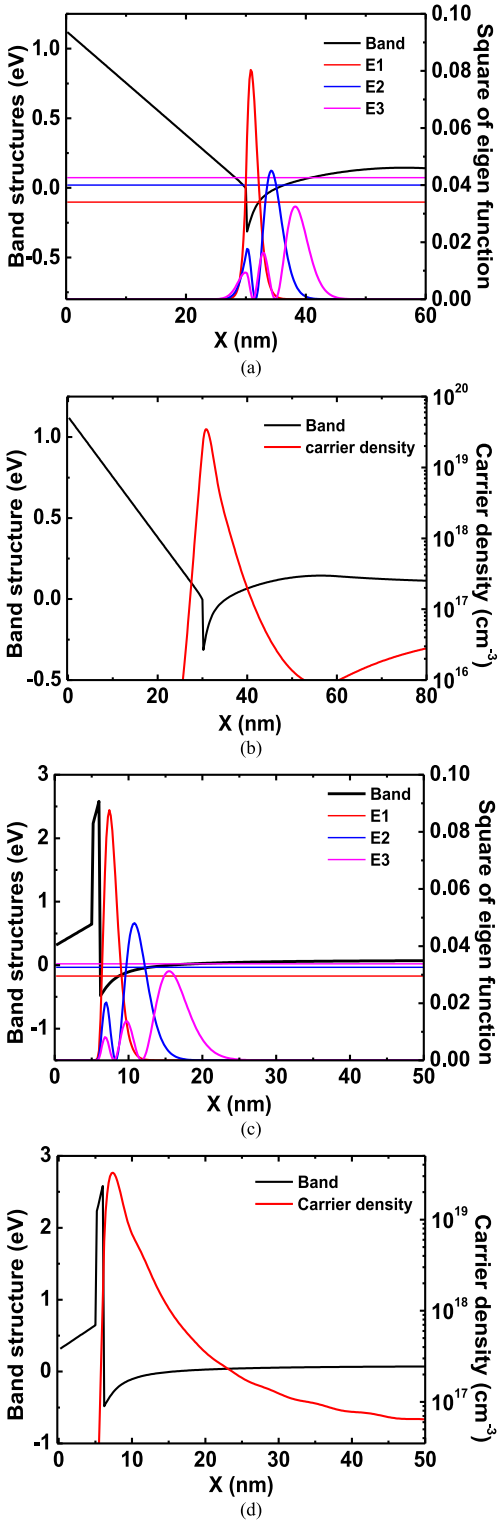

FIGURE 9. (a) The electron wave-function distribution and (b) carrier density distribution of AlGaN/GaN HEMT. (c) The electron wave-function distribution and (d) carrier density distribution of gate-recessed metal-gate/high-κ GaN MOSFET.

GaN well. The interfacial SiO_2 gate dielectric not only lowers the remote phonon scattering and increase the mobility, but also increases ΔE_C. Such large ΔE_C is crucial to confine the energetic channel hot electrons during device operation, which explains the excellent reliability even at $I_{ON,max}$ and 175°C stress. This large bandgap ultra-thin SiO_2 interfacial layer has been implemented in metal-gate/high-κ Si CMOS manufacture to improve the remote phonon scattering and increase the drive current [19], [22]. The oxidized AlGaN under selective-etching process may be the other potential mechanism to passivate the GaN surface and reach good interface compared with previous work [11].

IV. CONCLUSION

Excellent device performance of the highest $I_{ON,nor}$, high V_{BD}, low R_{on}, and the best reliability are achieved in gate-recessed metal-gate/high-κ GaN MOSFET simultaneously. This device has steep *SS* comparable with the metal-gate/high-κ Si MOSFET, but having significantly larger I_{ON}/I_{OFF} and higher V_{BD}. The excellent stress reliability is attributed to the large ΔE_C between the high-κ gate dielectric and GaN channel, which is in sharp contrast to the strong wave-function penetration into AlGaN barrier in the AlGaN/GaN HEMT.

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