This article has been accepted for publication in a future issue of this journal, but has not been fully edited. Content may change prior to final publication. Citation information: DOI 10.1109/JEDS.2016.2594190, IEEE Journal of the Electron Devices Society

Overview of Selector Devices For 3D Stackable Cross Point RRAM Arrays

R. Aluguri, Tseung-Yuen Tseng, *Fellow, IEEE*

Abstract— **Cross point RRAM arrays is the emerging area for future memory devices due to their high density, excellent scalability. Sneak path problem is the main disadvantage of cross point structures which needed to be overcome to produce real devices. Various self-rectifying cells like complementary resistive cell, Hybrid RRAM cell, valence modulated conductive oxide RRAM and non-linear resistive memory with tunneling barrier, etc., are proposed to overcome the sneak path problem and to achieve the high density with good on/off ratio. However it is challenging to fabricate the self-rectifying cells operating at low program/erase voltages with high non-linearity for both read and write operations and exhibiting good retention and endurance characteristics at the same time for a single device. 1S1R devices are more attractive than SRC due to large optimization possibilities to obtain better device performance as they have separate selector cell and memory cell which decouples the control parameters. Various kinds of selector devices like Si based selector, metal-oxide based selector, threshold switch selector, mixed ionic-electronic conduction selector etc., are under intense research to obtain the best performance cross point memory devices. In this article we have briefly discussed about recent progress on various self-rectifying cells and selector devices for obtaining 3D stackable cross point memory arrays.**

Index Terms— **Cross bar RRAM, Self-rectifying cells, Selector devices**

I. Introduction

A simple two-terminal Metal-Insulator-Metal (MIM) structure allows the implementation of resistive memories into high dense cross-point arrays. The concept of "crosspoint" for memory application can be traced back to more than 60 years ago [1]. A cross-point array consists of parallel interconnects (e.g. word lines/bit lines) at upper and lower planes, perpendicular to each other. Two-terminal memory devices are implemented at the crossing points of these wires. Assuming the width of both lines and spaces equals F (the minimal feature size), this leads to an effective cell area being $4F^2$, yielding the smallest single layer cell footprint. It is feasible to stack multiple 2D layers into a 3D configuration. By doing this, the minimal feature size is reduced further to $4F^2/n$, where n is the number of stacking layers. This prompts stacked cross-point arrays to be a promising architecture for high density and large capacity memory arrays. A practical problem associated with stacked 3D cross-point array is that the cost per bit does not always scale with the increasing number of layers, as it requires critical process steps, e.g. lithography and etching of metal lines and via contacts for each additional memory layer. This introduces extra process complexity and increases the fabrication cost. It has been reported that, to be most cost effective, the maximum number of stacking memory layers is about 8 [2]. In contrast, in the 3D vertical NAND (Bit-Cost Scalable) technology [3], a single critical lithography and etching step is used to define memory cells on different layers. Thus, such stacked 3D cross-point can hardly compete with 3D VNAND technology, from the cost point of view. Recently, vertical cross-point arrays for resistive random access memory (VRRAM) [2, 4, 5] were suggested, considering a similar approach BiCS (bit cost scalable) for 3D NAND Flash [3]. In this structure, all vertical cells on different layers are defined by a single critical lithography and etch step, for achieving comparable fabrication cost. On top of that, VRRAM is expected to have better scaling potential compared to VNAND [5]. Firstly, the lateral half-pitch of VRRAM is expected to be smaller than that of VNAND. The former is determined by the thickness of the RRAM device (simple metal-insulator-metal structure), while the latter is determined by the minimal polysilicon vertical channel and charge trapping layer thickness. Secondly, due to the short channel effect, vertical cell-to-cell coupling and change spread issue, a minimal horizontal word line (WL) to word line (WL) distance for VNAND is mandatory. For VRRAM, this distance is determined by the WL-to-WL parasitic leakages, which can be reduced when a good insulator barrier is employed. Considering these two factors, VRRAM is forecasted to consume less than 1⁄3 in lateral and 1⁄2 in vertical dimension compared to the current charge trap based VNAND, which is promising for further reducing the bit per cost. Therefore, 3D VRRAM is clearly a more suitable candidate than stacked 3D RRAM as the successor of VNAND Flash in the future.

Although RRAM cross-point array and VRRAM shows promising potential for high density memory applications, it has not yet been commercialized successfully today. One reason is that, to enable functional memory operation, it is required that each memory cell has good selectivity, which is enabled through a nonlinear electrical behavior. A strong non-linearity is essential to allow access to the specific

"This work was supported by the Ministry of Science and Technology, Taiwan, under Project No. 102-2221-E 009-134-MY3 ".

R. Aluguri is with the National Chiao Tung University, Hsinchu, Taiwan, 30010 (e-mail: aluguri.iitkgp@ gmail.com).

Tseung-Yuen Tseng is with the National Chiao Tung University, Hsinchu, Taiwan, 30010 (e-mail: tseng@cc.nctu.edu.tw).

2168-6734 (c) 2016 IEEE. Translations and content mining are permitted for academic research only. Personal use is also permitted, but republication/redistribution requires IEEE permission. See http://www.ieee.org/publications_standards/publications/rights/index.html for more information.

This article has been accepted for publication in a future issue of this journal, but has not been fully edited. Content may change prior to final publication. Citation information: DOI 10.1109/JEDS.2016.2594190, IEEE Journal of the Electron Devices Society

device(s) in the memory array without affecting or being affected by the others [6]. However, most of the reported resistive memory cells show nearly ohmic behavior in both LRS and HRS. This causes sneak currents through the unselected cells in the cross point array during memory operation. Two approaches are available to overcome these sneak current problems, firstly, using a self-rectifying cell (SRC) that will show non-liner I-V characteristics inherently and secondly, using an additional select device with non-linear I-V characteristics. In this paper, we have given an overview of recent progress on self-rectifying cells and non-linear select devices to achieve the high density and highly selective 3D RRAM cross point array for future memory devices.

II. SNEAK PATH CURRENT PROBLEM

Taking a 2D cross-point array as an example, read error occurs when the detectable difference between readout current of a selected element in LRS and HRS vanishes, as shown in Fig. 1. Due to the presence of the line resistance, the extra leakage induces significant IR voltage drop on the interconnecting lines, thus degrading the accessibility to the target cell, especially during the write operation where high currents are involved. Moreover, the leakage currents raise the total power consumption. With increasing array size, the array performance degradation is getting even worse due to the presence of more leakage paths.

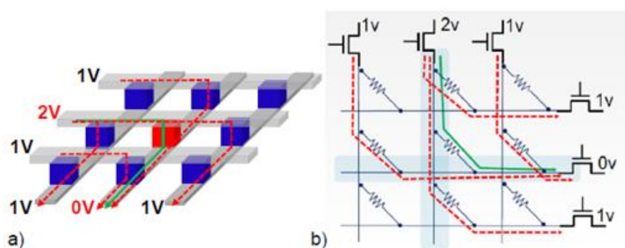


Fig. 1. (a) Illustration of sneak current in cross-point array with (nearly) linear resistive switching memory cells during read operation. (b) Circuit schematic of crosspoint rray. Red dash lines: sneak current paths. Green solid line: actual readout signal from the selected element. Reprinted from [1].

The sneak current issue occurs for vertical RRAM array as well when linear resistive memory elements are used which is observed in Fig. 2. These leakage currents would degrade array performance. For instance, the readout current (collected on the selected bitline pillar) consists of both real read signal and parasitic leakage currents from the unselected cells at different layers. With increasing the number of layers for VRRAM, more cells are connected to the vertical bitline pillar. This leads to more leakage paths, which causes additional read margin degradation. In the ideal case, the memory operation (e.g. read and write) is supposed to take place only on the selected memory cell(s), leaving the rest of the cells unaffected [6]. This, results in zero parasitic leakages and no additional power dissipation. However, this is nearly impossible in reality. An alternative solution is to introduce non-linear I-V characteristics into each memory cell [6, 7].

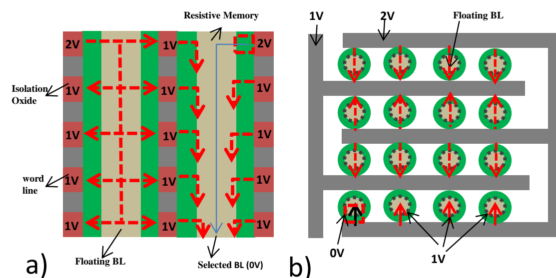


Fig. 2. Illustration of potential sneak currents in VRRAM array with linear resistive switching memory cells. (a) side view of cross-section a-a'. (b) top view. Red dash lines: potential sneak current paths. Green solid line: actual readout signal from the selected element.

To this end, a possibility is to use a separate, non-linear device, such as a diode [7], serially connected with each resistive memory element, in a one-selector one-resistor (1S1R) configuration as shown in Fig. 3. A two-terminal selector structure is required for implementing this in a cross-point array, so as not to cause additional memory array area overhead. In this case, the parasitic leakage is largely suppressed due to the high resistance of a non-linear selector at small bias, which would dominate the full cell characteristics for the unselected memory cells. The advantage of this approach is that each of the elements can be tuned separately to achieve the best full cell characteristics that fulfill the performance targets [6], while the disadvantage is the increasing process complexity required to integrate full stack. Moreover, if a middle electrode is needed between the 1S and 1R components, so as to form a M-O-M-S-M stack, where 'O' refers to oxide for resistive memory, and 'S' refers to material

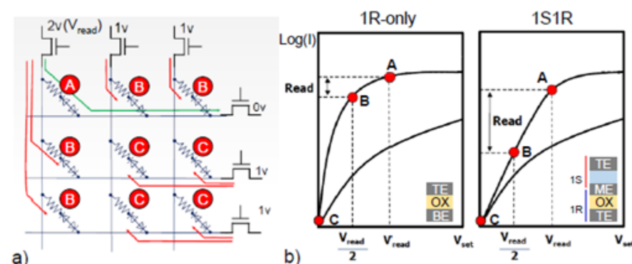


Fig. 3 (a) Schematic of leakage current suppression by introducing non-linear characteristics into each memory cell during read operation. (b) I-V comparison of ohmic 1R and non-linearity '1S +1R' cell configuration. TE: top electrode, ME: middle electrode BE: bottom electrode. Adapted from [1, 5].

for selector.

Fig. 4(a) represents the 1S1R structure which is not compatible with a vertical RRAM architecture. Firstly, it would compromise the lateral scaling. Secondly, it would form a conductive electrode connecting the cells on the same vertical string, thus creating a short between neighboring cells at the adjacent planes. To isolate the cells, this inner electrode must be etched away, which is almost impossible. Thus, a second approach is to directly introduce non-linear I-V behavior into the memory cell itself. Such resistive memory device is also called self-rectifying cell (SRC) or selector less memory

2168-6734 (c) 2016 IEEE. Translations and content mining are permitted for academic research only. Personal use is also permitted, but republication/redistribution requires IEEE permission. See http://www.ieee.org/publications_standards/publications/rights/index.html for more information.

This article has been accepted for publication in a future issue of this journal, but has not been fully edited. Content may change prior to final publication. Citation information: DOI 10.1109/JEDS.2016.2594190, IEEE Journal of the Electron Devices Society

device. In this case, only one memory device is needed to be integrated, without implementing a separate selection device. Fig. 4(b) shows a non-linear SRC structure which is compatible with VRRAM architecture as well as planar cross-point arrays. This approach has an obvious advantage from process point of view, however, finding the proper material systems to achieve performance requirements from all aspects such as stable memory resistance states (LRS/HRS), high non-linearity for both read and write operations, low switching current and voltage, etc, remain big challenges.

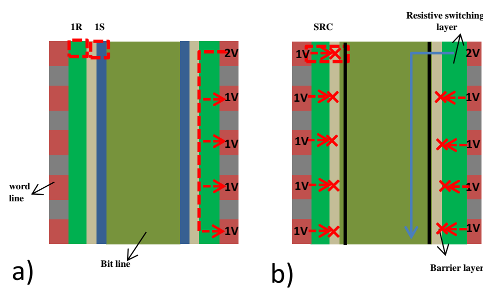


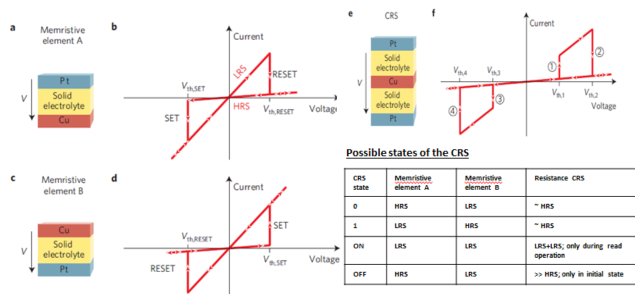
Fig. 4. (a) 1S1R configuration with inner metal electrode is not appropriate in VRRAM since it would form a conductive electrode connecting the cells on the same (vertical) string, creating additional short-circuit paths. (b) A non-linear self-rectifying cell (SRC) is suitable for VRRAM. e.g. to block the leakage currents by build-in tunneling barrier in the device. The arrows indicate the potential leakage paths.

III. SELF-RECTIFYING CELL (SRC)

In general, a resistive memory device which provides selectivity inherently without using an additional selector is called SRC. Recently, several SRC concepts have been reported showing attractive characteristics. In this section, three types of SRCs are briefly introduced.

A. *Complementary resistive switching (CRS)*

CRS was firstly reported by Linn et al [8]. Their CRS cell consists of two back to back connected CBRAM cells in which each single CBRAM cell has similar bipolar switching characteristics to that of oxide-based RRAM. Fig. 5 shows the schematic diagram and switching characteristics of both single CBRAM cell and a CRS cell. A conductive filament of copper-ions is formed (LRS) by applying positive voltage on the Cu electrode and dissolved (HRS) by applying voltage at the negative polarity which is shown in fig. 5(a)-5(d). Two



Possible states of the CRS

CRS state	Memristive element A	Memristive element B	Resistance CRS
0	HRS	LRS	~ HRS
1	LRS	HRS	~ HRS
ON	LRS	LRS	LRS+LRS; only during read operation
OFF	HRS	LRS	>> HRS; only in initial state

Fig. 5. (a)-(d) Schematic of single CBRAM cell and typical switching characteristics. (e) Structure of CRS cell (f) Switching behavior of a CRS and illustration of resistance state distribution between the two CBRAM elements. Reprinted from [8].

stacked CBRAM cells, sharing one common Cu electrode in the middle, forms a CRS device as shown in fig. 5(e).

A "butterfly" shape I-V characteristics is observed, owing to the four combinations of resistance states between the two resistive memory elements. After initializing the HRS/HRS ('OFF') state, the logic state '1' is represented by LRS (top-cell)/HRS(bottom-cell) state and HRS/LRS has the state '0'. The fourth state ('ON', LRS/LRS) is triggered during the read operation. The leakage current can be suppressed at both logic states ('0' and '1'), because at least one of the resistive elements is in the HRS. The logic state is distinguishable by applying a positive read voltage greater than the set voltage (V_{SET}) of the bottom cell. When the cell is in LRS/HRS (logic '1') state, this triggers the formation of a filament in the bottom cell, thus LRS/LRS is achieved, resulting in a high readout current. On the other hand, the cell stays in HRS/LRS (logic '0') at read voltage leading to a low readout current. The read '1' operation in the CRS cell is destructive, so a write-back process is needed to bring the LRS/LRS to the original LRS/HRS state by applying a negative voltage. This will increase the complexity from peripheral circuit design point of view [6]. Moreover, it causes extra power consumption, which makes it less attractive for frequently-read memory applications. Furthermore, this limits the read endurance to be equal to the program endurance. Until now, CRS have been reported not only for CBRAM [8, 9], but also for a variety of oxide-based RRAM [10–12] and amorphous carbon based RRAM cells [13], in a back-to-back connected cell configuration. However, the inner metal electrode makes the device structure less attractive to VRRAM architecture. In contrast to these M-I-M-I-M ('M': metal, 'I': insulator or electrolyte) CRS structure, Nardi et al. [14] reported CRS

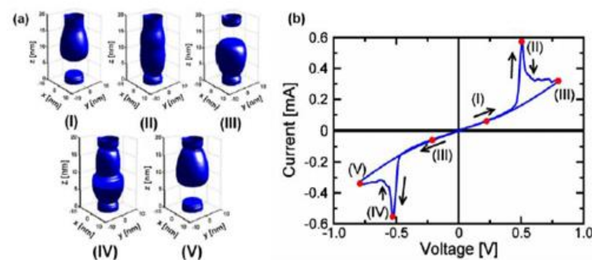


Fig. 6. (a) Simulated filament's shape and (b) corresponding I-V sweeps shows CRS behavior. Reprinted from [14].

operation in single a HfO_x layer M-I-M stack as shown in fig. 6.

The CRS behavior in this case is explained as following [14]: When a strong negative voltage is applied with respect to the top electrode, a depletion gap is created near the bottom electrode due to the lack of oxygen vacancies. Then, upon applying a positive voltage, the oxygen vacancies are drifted from top electrode towards the bottom electrode forming the conductive filament. So, the cell shows a low resistance state in this condition. Further increasing the positive voltage causes depletion of oxygen vacancies near top electrode, leading to a high resistance state again. In this way the conductive filament

2168-6734 (c) 2016 IEEE. Translations and content mining are permitted for academic research only. Personal use is also permitted, but republication/redistribution requires IEEE permission. See http://www.ieee.org/publications_standards/publications/rights/index.html for more information.

can be connected, depleted and reconnected by applying negative voltage. Fig. 6 (a) shows the simulated filament's shape by a numerical model and corresponding I-V characteristics during switching. Beyond simulation analysis, the paper also reported a real oxide-RRAM (TiN/HfO_x(5nm)/TiN) stack showing such CRS behavior, which aligns with the simulation prediction. Thus interests for CRS cells are driven by their non-linear I-V characteristics, which can be achieved using the existing bipolar resistive memory cells. However, several issues are remaining as challenges for practical CRS cell implementation. Firstly, it is hard to control the uniformity of CRS due to the variability inherent to each memory element in the stack. This implies that it could be difficult to achieve low current operation in the CRS, as the variability usually increases with lowering the current for the filamentary resistive elements [15–17]. Secondly, a destructive read requires a write-back process, which increases complexity of circuit design.

B. Hybrid RRAM-selector cell

The W/NbO_x/Pt cell was demonstrated by Kim et al. [18], where Nb_2O_{5-x}/NbO_{2-x} stack layer is formed for a hybrid device with both memory and selector properties as shown in fig. 7. Different properties are obtained due to different atomic ratio (Nb/O) in the NbO_x film. For instance, a NbO_{2-x} film [19, 20] shows a typical metal-insulator transition (MIT) selector behavior, while Nb_2O_{5-x} layer exhibits bipolar filamentary resistive switching. By controlling the oxygen concentration during deposition, Nb_2O_{5-x} and NbO_{2-x} are formed successively to achieve both memory and selector functionalities in the same cell as shown in fig. 7(b). A merit of this structure is that an additional middle electrode is not needed for separating the selector and memory cell. The reported hybrid devices show good DC cycling, high temperature thermal stability and good device-to-device uniformity.

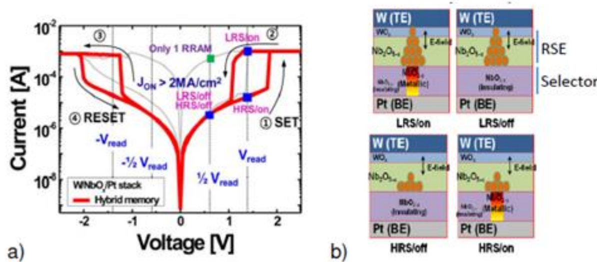


Fig. 7. (a) I-V characteristics of hybrid W/NbOx/Pt device showing both threshold switching and resistive memory behavior. (b) Proposed switching model for hybrid resistive memory device. Reprinted from [18].

C. Non-linear resistive memory with tunneling barrier

A non-linear resistive memory is also achieved by engineering the oxide multi-layers for filamentary resistive memories. For instance, where a thin tunneling barrier is inserted to generate non-linear characteristics [21-23], Chand et al. reported a 5×6 μm^2 HfO_2 cross bar RRAM with inserting a thin Al_2O_3 tunnel layer [21]. The device with tunnel layer has shown an excellent non-linearity factor (37) in comparison to the device without tunnel layer (1.7). Here the non-linearity factor gives the quantitative measure of non-linearity in the low resistance state, and is defined as the ratio of the current at the read voltage (I @ V_{read}) to the current at the half-of- the read voltage (I @ $1/2V_{read}$).The conduction in the HfO_2 layer is dominated by hopping and a direct tunneling through the large band gap Al_2O_3 tunnel layer at high polarity, similar to the conduction mechanism in the metal-insulator-metal diode [21] is observed. This resulted in abrupt increase of the current through the device due to Fowler-Nordheim tunneling effect and has shown a high non-linearity factor and large endurance of 10^4 cycles. Park et al. reported a new memory structure with two tunneling barriers as shown in Fig. 8[22]. In this, the original resistive memory cell consists of two transition metal oxide (TMO) films acting as resistive switching layers. While in the new structure, additional barrier layers are imposed at both bottom and top of the stack as shown in fig. 8(b). Compared to the original cell switching from fig. 8(c), the new device exhibits strong non-linear I-V characteristics in the LRS as shown in fig. 8(d). Moreover, the switching current is reduced to below ~1 μA. Note that low current operation and high non-linearity are both desired for an ideal self-rectifying cell, in order to minimize power dissipation and IR voltage drop during memory operation. Further investigation showed that the two inserted barrier layers play different roles regarding to switching. The bottom barrier acts a tunneling barrier. The initial leakage current for both states can be decreased with increase of this barrier thickness, thus improving the cell non-linearity. The top barrier, on the other hand, provides self-current compliance. This improves pulse endurance by limiting potential current overshoot. As a consequence, excellent pulse stress up to 10^7 cycles at program condition was achieved with limited degradation through the whole I-V voltage range.

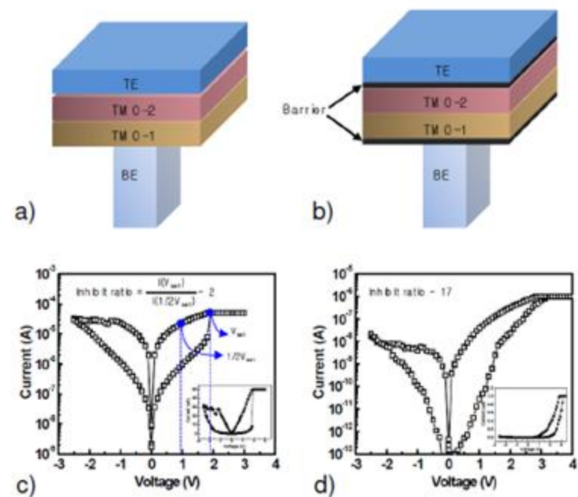


Fig. 8. Schematic of (a) the original resistive memory stack and (b) self-rectifying cell structure. (c) Switching characteristics of (a). (d) Low current and non-linearity is achieved for structure (b). Reprinted from [22].

2168-6734 (c) 2016 IEEE. Translations and content mining are permitted for academic research only. Personal use is also permitted, but republication/redistribution requires IEEE permission. See http://www.ieee.org/publications_standards/publications/rights/index.html for more information.

D. *Vacancy Modulated Conductive Oxide (VMCO)-RRAM*

Govoreanu et al. demonstrated self-rectifying $TiN/Al_2O_3/TiO_2/TiN$ cell as shown in fig. 9 [22]. A post TiO_2 deposition anneal reduces the TiO_2 layer, creating an oxygen vacancy (Vo) profile across the film, hence a vacancy modulated conductive oxide (VMCO) active layer [24]. VMCO cell switches in self-compliance mode.

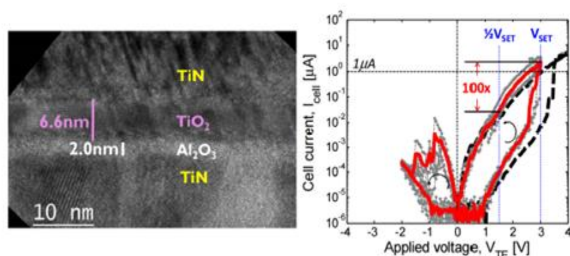


Fig. 9. (a) TEM picture of the proposed device structure.
(b) Switching characteristics of VMCO cell. Reprinted from [24].

Furthermore, the cell exhibits low current operation and strongly non-linear I-V behavior. The switching current scales with cell size, indicating that the switching takes place uniformly over the entire cell area, in contrast to the filamentary resistive memory cells. The oxygen vacancies can move back and forth according to the polarity of the applied electric field [24], resulting in a change of the barrier seen by the tunneling electrons which is schematically demonstrated in fig.10. For instance, in the HRS and initial state, the vacancies are close to TiN/TiO_2 interface, leaving the whole 'defect-free' tunneling barrier (Al_2O_3 + part of TiO_2) layer, thus increasing the cell resistance. When a positive voltage is applied on the top TiN, the oxygen vacancies are pushed through the whole TiO_2 region. Therefore, the LRS cell resistance reduces since it is mostly determined by the Al_2O_3 only.

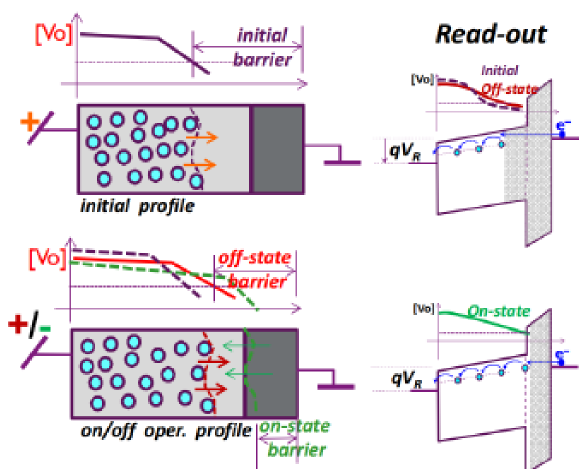


Fig. 10 Schematic of proposed model for VMCO switching. Reprinted from [24].

SRC was also demonstrated by Meyer et al. [25] and Chevallier et al. [26]. A simple Pt/Tunneling oxide (TO)/Conductive metal oxide (CMO)/Pt stack was developed as a resistive memory device. Fig. 11(a) shows that self-compliance, low current switching and non-linearity can be achieved simultaneously. Although this cell structure is similar to that of the self-rectifying cells that was introduced before, the underlying resistance change mechanism is different. A schematic model is shown in fig. 11(b) representing the conduction mechanism in the device under various applied fields. A large electric filed is generated in the tunnel barrier at program and erase voltages due to its small thickness. This high field penetrates through the CMO upto a distance of Debye-length resulting in the exchange of oxygen ions between TO and CMO as shown in fig. 11(b). Thus the oxygen ions exchanges between TO and CMO upon the application of negative and positive voltages.

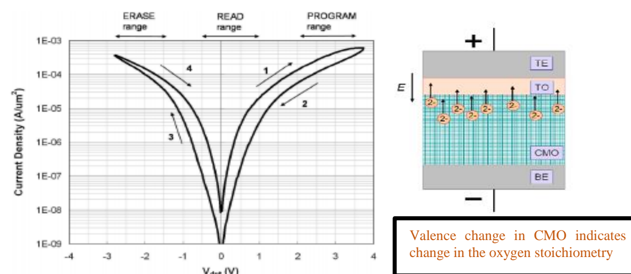


Fig. 11 (a) I-V characteristics of dual-layer resistive memory cell. (b) Proposed model for the resistance switching. Reprinted from [25].

IV. SELECTOR FOR RRAM

Besides SRC, introducing an additional selection device in serially connected with each memory element in a 1S1R configuration is another effective way to inject self-selectivity to the cross-point arrays. Compared to the SRC, using separate memory and selector cell decouples control parameters, allowing optimization individual component separately to reach the overall device performance targets. As a consequence, the 1S1R device appears relatively easier to meet the performance requirements than the SRC. It is believed that the 1S1R RRAM cross-point arrays which are suitable for the potential storage class memory (SCM) applications will pioneer the commercialization of the RRAM technology in the near future, before VRRAM acting as VNAND replacement. Compared to CRS and 1D1R, 1S1R shows the higher non-linearity factor. A sufficient read margin can be obtained using An All-LPU (All line pull up) scheme in all types of devices i.e., CRS, 1D1R, or 1S1R. However, unreliable write is the major obstacle in CRS and 1D1R. The 1S1R crossbar RRAM with excellent read and write margins using high band width parallel schemes has high potential as a new generation SCM.

An ideal selector has several characteristic requirements to enable high density 1S1R cross-point arrays. These requirements are basically derived from circuit performance aspect, device and process compatibility. A two-terminal selector is needed so as not to cause extra memory array area overhead, to enable achieving the minimal single layer cell footprint $4F^2$ (F: feature size). This renders up the usage of a

2168-6734 (c) 2016 IEEE. Translations and content mining are permitted for academic research only. Personal use is also permitted, but republication/redistribution requires IEEE permission. See http://www.ieee.org/publications_standards/publications/rights/index.html for more information.

This article has been accepted for publication in a future issue of this journal, but has not been fully edited. Content may change prior to final publication. Citation information: DOI 10.1109/JEDS.2016.2594190, IEEE Journal of the Electron Devices Society

silicon-based four-terminal transistor as cross-point array selection device, although a transistor acts as a perfect switch for blocking leakage current [27, 28]. A selector should be able to provide enough current as needed for SET and RESET operations of the resistive memory cell. For instance, to enable resistive memory with ~10 A switching current, this translates to current density of ~10 MA/cm^2 for a selector, where targeting 10x10 nm^2 cell size. The maximum achievable cross-point array block size depends on the circuit performance like sufficient read margin, acceptable read/write power, etc, which is strongly affected by the leakage currents from the unselected memory elements. The leakage current needs to be as low as possible for improving the overall memory operation.

Table I: Selector device requirements

Parameter	Ideal value
ON current I_{on}	>10MA/cm^2
Threshold Voltage, V_{th}	~ 0V
ON/OFF ratio	>10^6
Processing temperature	<400 ^{o}C
Operating temperature	85 ^{o}C
Switching speed	<50 ns
Operation polarity	Compatible with memory element
Scalability	Comparable with memory element

Considering that an ideal selector should have high current at high voltage as well as very small current at low voltages simultaneously, this translates into a highly non-linear characteristic [6]. As most of the reported resistive memory cells exhibited better performance in bipolar operation mode, a bidirectional selector, which could provide symmetrical I-V, such as high drive current and highly non-linearity at both polarities is required. Resistive memory elements have various SET and RESET voltages depending on their material system and underlying working mechanisms. It is important that the selector element is compatible with the memory cell, in order to transfer selector non-linearity to the 1S1R full cell, to ensure limited leakage current from the unselected memory elements during both read and write operations. It is difficult to assess the performance of a selection device quantitatively without knowing the resistive memory to be paired [6, 29, 30]. An ideal selector device should be fast enough, imposing no speed limitation on the operation of the memory device. Moreover, the reliability such as cycling endurance, array yield, variability should be as good as or even better than the resistive memory cell [6]. The material utilized by selector fabrication should be CMOS process compatible, which limits the usage of materials such as Pt, Ag, Au, etc in the structure. Moreover, to enable 3D stacked memory arrays, the thermal budget of selector device fabrication should be compatible with the back-end-of-line (BEOL) process. Besides, the selector should be able to withstand 400°C thermal stress for ~2h, considering the processes needed for stacking subsequent memory layers and wiring interconnects [6]. It is also desired that a selector has a simple structure and low aspect ratio, to reduce the process complexity. Some of the important parameters of the ideal selector device are given in the Table I.

The above discussed selector requirements make it very challenging to implement a qualified selector device for cross-point arrays. In the following part, we will survey the main reported selector concepts, and discuss their merits and demerits.

V. KIND OF SELECTOR

A. Silicon-based selectors

Transistors have been used as the selector devices for many decades as they can fulfill the several requirements of the selector. Transistors offers large drive current which provides high ON/OFF ratio, self-compliance, tunable threshold voltage with doping variation and mass production with high reliability which makes them attractive towards the selector devices. In 2013, Panasonic has developed an industry's first new non-volatile memory RRAM. The 1T1R-RRAM memory is fabricated by the CMOS process with 0.18 μm low power consumption RRAM, enabling readout at low-voltage and fast memory cell rewriting at 10 ns. Microcomputer with RRAM reduces power consumption of applications, in particular allowing longer battery life and downsizing for environment infrastructure equipment, such as smart meter, and mobile devices, such as smart phone requiring low power consumption. However, the relatively large size and a complex fabrication process limit the use of transistors as selector devices.

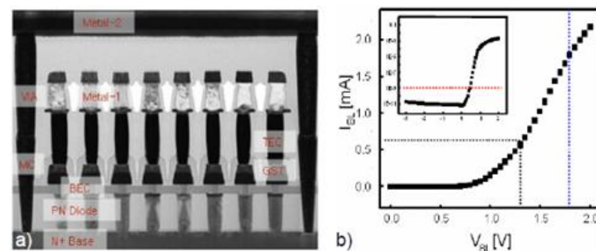


Fig. 12 (a) Vertical Si diode (90nm tech. node) selector for 512Mb PCRAM chip with 5.8F^2 cell size. BEC: bottom electrode contact. GST: $Ge_2Sb_2Te_5$. TEC: top electrode contact. (b) I-V characteristics for PN diode. Reprinted from [31].

Epitaxially grown PN (P-i-N) diodes [31–33] have been reported and demonstrated firstly for the unipolar phase change memories (PCRAM) as selector devices. J.H. Oh et al. fabricated vertical diodes with selective-epitaxial-growth (SEG) on single crystalline Si substrate, to improve the rectifying ability (forward/reversed biased I_{on}/I_{off} current ratio) compared to that of poly-Si case [31]. The selector devices integrated in a 512Mb PRCAM test chip, presented in fig. 12(a), are showing functional memory operations. The demonstrated PN diodes show high on-current density exceeding 25MA/cm^2 with I_{on}/I_{off} ratio of about 10^8. The advantage of using PN diodes as cross-point array selector

2168-6734 (c) 2016 IEEE. Translations and content mining are permitted for academic research only. Personal use is also permitted, but republication/redistribution requires IEEE permission. See http://www.ieee.org/publications_standards/publications/rights/index.html for more information.

devices come from three aspects: firstly, many decades of manufacturing and research experience with Si based device make it relatively easy for performance tunability, enabling PN diodes to be compatible with the memory cell [6]. Secondly, PN diodes provide high on-current, which is able to drive successful SET or RESET operation for the memory cell. Thirdly, parasitic leakage can be largely suppressed due to the extremely small reversed bias current. However, due to the fact that most of the resistive memories operate in bipolar switching mode, a unipolar PN diode is not suitable. Two-terminal Si-based selector being capable of providing symmetrical I-V characteristics have been reported, such as punch through NPN diodes [34–36].

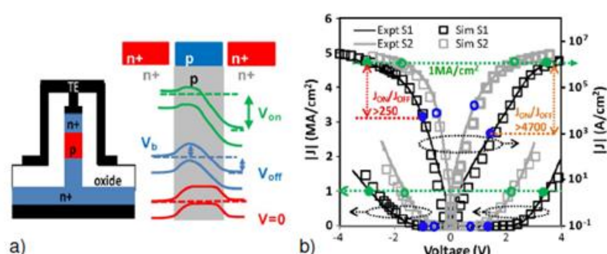


Fig. 13 (a) NPN selector structure and underlying conduction mechanism (b) Simulated and experimental I-V behavior of NPN selector. Reprinted from [34].

The device concept reported by S. Kim et al. as shown in fig. 13(a) is described as follows [37]. A potential barrier is formed at N^+/P junction to block the electrons to pass from one side to the other at zero and low bias. By increasing the applied voltage, the depletion region of the P/N^+ (cathode, reversed bias) extends and the P region becomes more attractive for electrons. This is an equivalent effect to reduce the barrier for electrons, which is similar to the "drain induced barrier lowering" (DIBL) or punch through effect in short channel transistors.

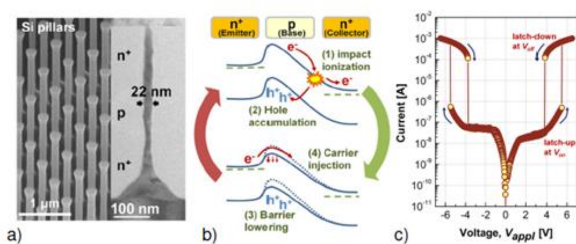


Fig. 14 (a) NPN selector structure and underlying conduction mechanism (b) Simulated and experimental I-V behavior of NPN selector. Reprinted from [37].

Srinivasan et al. demonstrated NPN punch through selector showing a maximum drive current density over 1MA/cm^2, with I_{on}/I_{off} ratio (half-bias nonlinearity) of about 4700[34]. The operating voltage range is tunable, for instance, by adjusting the thickness of the P region and doping concentration. Fabrication of such diodes requires in-situ doped epitaxial Si growth process with thermal budget of over 700 °C. The high temperature of process makes this concept less suitable for a BEOL process and 3D stacking. Kim et al. demonstrated a latch-up based NPN bidirectional selector [37]. The silicon N/P/N regions are formed subsequently by three-step ion implantation, followed by the silicon pillar dry etching. This resulted in the growth of Si pillars with diameter of 22nm as shown in fig. 14(a). Interestingly, such device is characterized by an abrupt increase of current in contrast to showing a smooth I-V behavior as shown in fig. 14(b). It is believed that excess holes are generated due to impact ionization at the reversely biased junction, and then are accumulated at the P region [37]. These holes effectively reduce the barrier height for electrons injected from the emitter. This further enhances the process of impact ionization. Thus, a positive feedback loop is established, at certain level it results in a sudden jump of the current. This NPN selector exhibits promising on-current exceeding 50 MA/cm^2 and on-/off-state selectivity of over 10^4. While the thermal budget is not mentioned, it is expected that a high temperature annealing is necessary for dopant activation. So far, we have introduced silicon-based two-terminal devices as potential selector applications. One common issue related to all silicon-based selectors remains the high temperature annealing process, which is required for dopant activation. This makes the devices less suitable for sub-400 °C BEOL process and 3D stacked multi-layer memory structures. Besides, dopant and grain-size induced cell variability could be a potential issue for scaled devices, specifically to lowly doped and polycrystalline films, when device dimension becomes comparable to the grain size.

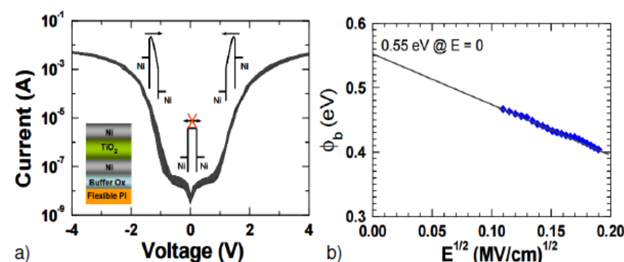


Fig. 15(a) I-V characteristics for Ni/TiO_2/Ni selector. (b) Extrapolation of barrier height at Ni/TiO_2 interface. Reprinted from [40]

B. Metal-insulator-metal based selectors

Various oxide-based diodes have been reported [38–44]. D. Y. Lee et al. fabricated a 1D1R structure using Pt/IZO/CoO/Pt/TiN oxide diode and Pt/HfO_2/ZrO_2/TiN resistive element [38]. Pt/IZO/CoO/Pt/TiN structure has shown non-linear I-V characteristics well fitted with basic diode I-V characteristics with slope of 8. The device has shown unipolar RS behavior under forward bias with sufficient forward current and large reverse current resulting in a large F/R ratio of 7×10^3 at 2 V. Huang et al. suggested a Ni/TiO_2/Ni structure showing bipolar non-linear characteristics as shown in fig.15(a) [39, 40]. The proposed device has a maximum drive current of about 10^5 A/cm^2 and an on/off ratio of about 10^6 (ratio between maximum current and current close to zero bias). From fig. 15(b), the

2168-6734 (c) 2016 IEEE. Translations and content mining are permitted for academic research only. Personal use is also permitted, but republication/redistribution requires IEEE permission. See http://www.ieee.org/publications_standards/publications/rights/index.html for more information.

This article has been accepted for publication in a future issue of this journal, but has not been fully edited. Content may change prior to final publication. Citation information: DOI 10.1109/JEDS.2016.2594190, IEEE Journal of the Electron Devices Society

conduction mechanism is described as Schottky emission at the Ni/TiO_2 interface, where the extracted barrier height is ~0.55 eV at zero bias. A non-linear Schottky diode is also fabricated using Pt/TiO_2/TiN by Shin et al. [41]. The device shows asymmetrical I-V behavior, i.e. lower current is observed when applying negative voltage on Pt electrode.

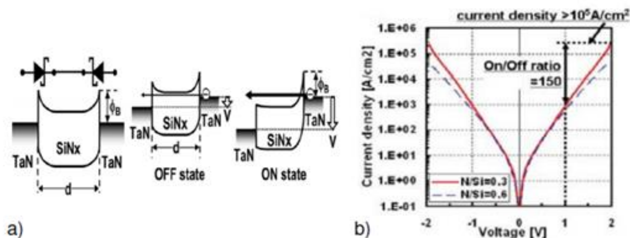


Fig. 16 (a) Schematic band diagram Metal/SiN_x/Metal Schottky selector. (b) I-V characteristics of selector. Reprinted from [41, 42].

This is explained by a higher Schottky barrier for electrons injected from Pt/TiO2 than that from TiN/TiO_2 interface. The maximum achievable current density is ~1.5×10^5 A/cm^2, when injecting current from the TiN/TiO_2 interface. By choosing a suitable metal electrode with respect to nitride-based semiconductor (SiN_x), a back-to-back Schottky diode is formed as shown in fig. 16(a). The injection current is mainly determined by the reversed biased Schottky contact at the cathode, yielding non-linear I-V characteristics, which are tunable, e.g. by increasing the N% content to increase the band-gap of SiN_x, thus increasing the Schottky barrier height as shown in fig. 16(b). With a N/Si ratio of ~0.3, the selector shows maximum current drive ~2×10^5 A/cm^2 and an on/off ratio (half-bias current ratio) of ~150.

Another approach to achieve highly non-linear I-V characteristics is to use an oxide layer as tunneling barrier. Electron tunneling is a quantum-mechanical process that causes exponentially increasing current with the applied voltage [45]. A simple Metal-Insulator-Metal (MIM) consisting of thin oxide film such as HfO_2, Al_2O_3, TiO_2, etc exhibits excellent non-linear I-V characteristics fulfilling the requirement of selector device [46, 47].

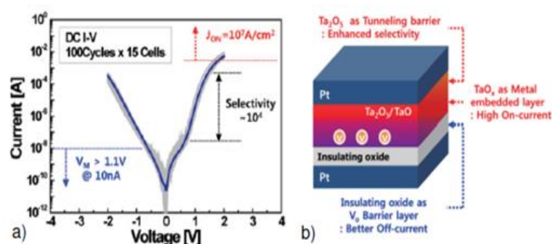


Fig. 17. (a) Schematic band diagram Metal/SiN_x/Metal Schottky selector. (b) I-V characteristics of selector. Reprinted from [49].

Govoreanu et al. [45] reported a novel TiN/Ta_2O_5/TiN bidirectional selector with an ultra-thin ALD deposited Ta_2O_5 layer, which achieves high drive current density ~10^5 A/cm^2, half-bias non-linearity ~360, fast turn-on/off speed and excellent AC endurance. By engineering the tunneling barrier of using multiple oxide stacks [48–50], MIM selector has been optimized towards ~10^7 A/cm^2 maximum drive current and half-bias nonlinearity of about 10^4 in Pt/Ta_2O_5/TaO_x/TiO_2/Pt structure proposed by Woo et al. [48]. Fig. 17 shows the schematic structure and I-V characteristics of the proposed structure. The oxide layers are formed by applying thermal oxidation annealing on TaOx/TiO_2, resulting in formation of Ta_2O_5/TaO_x/TiO_2 stack as shown in fig. 17(b).

The outer oxide layer provides large barrier height for electrons to be injected from both sides. Moreover, due to large total oxide thickness, the tunneling current at low bias is significantly suppressed. The barrier height gradually decreases towards the inner TaO_x layer. At high biases, the current increases dramatically due to band bending, which enables electrons to tunnel through the thin oxide barrier at the injected interface. Instead of using a Pt electrode, a fully CMOS process compatible W/Ta_2O_5/TaO_x/ TiO_2/TiN device was demonstrated recently [50]. However, this comes at the cost of reducing cell non-linearity, possibly due to barrier height lowering given the low-work function metal TiN.

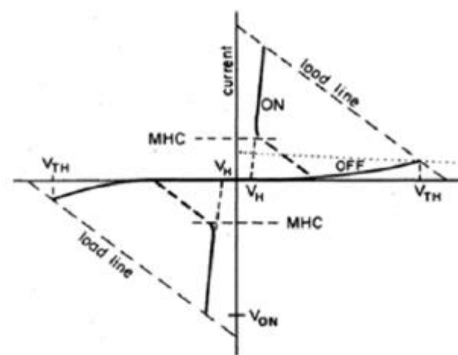


Fig. 18 Schematic of OTS characteristics. V_H: holding voltage. V_{TH}: threshold voltage. Reprinted from [51].

C. Threshold switching selectors

1) Ovonic threshold switching (OTS)

Ovonic threshold switching (OTS) behavior was firstly reported by S. R. Ovshinsky, in various amorphous chalcogenide alloy materials [51]. A rapid increase of current is observed in the I-V characteristics of the OTS selectors during voltage controlled sweep. This resembles that during the current controlled sweeps, I-V characteristics of the OTS exhibits negative differential resistance (NDR) behavior between a threshold voltage and a holding voltage. Fig. 18 represents the schematic illustration of the I-V characteristics of OTS selector device. From the fig. 18, it is clear that the NDR region is unstable resulting in a rapid and reversible transition to either a high resistance state (off-state) or to a low resistance state (on-state). Interests for using the OTS mechanism for selector device implementation mainly comes from two aspects: firstly, its large off-state resistance ratio provides 1S1R full cell selectivity at program and readout

2168-6734 (c) 2016 IEEE. Translations and content mining are permitted for academic research only. Personal use is also permitted, but republication/redistribution requires IEEE permission. See http://www.ieee.org/publications_standards/publications/rights/index.html for more information.

This article has been accepted for publication in a future issue of this journal, but has not been fully edited. Content may change prior to final publication. Citation information: DOI 10.1109/JEDS.2016.2594190, IEEE Journal of the Electron Devices Society

conditions. Secondly, most threshold switching materials show high on-state drive currents (e.g. >10 MA/cm^2), which enables resistive memory with over 10 A switching current at 10 nm-scale. The OTS phenomenon has been explained by several theories, such as thermally induced electronic switching [52], impact ionization and recombination [53, 54], etc. Recently, Ielmini et al. developed an analytical model based on trap-limited conduction [55, 56], which can fit with experimental data well as shown in fig. 19 (a). I-V behavior at the low current regime is described by the Poole-Frenkel (PF) model, where an exponential increase of the current is due to

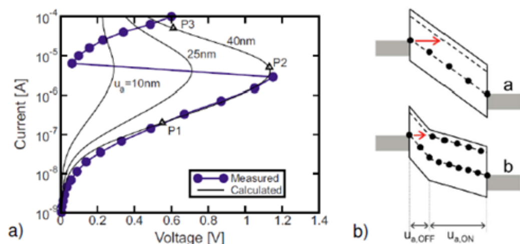


Fig. 19 (a) Measured I-V sweep for amorphous $Ge_2Sb_2Te_5$ chalcogenide phase-change memory cell and analytical model prediction. (b) Schematic for (a) low-voltage (off-state) region and (b) for high voltage (on-state) regime. Reprinted from [55, 56].

the field-induced barrier lowering effect, which enhances electron hopping conduction. As further increasing the applied voltage, electrons tunnel to higher energy traps. The tunneled electrons occupy the shallow traps close to the conduction band, resulting in a non-uniformity of the electric field across the OTS material. To a certain extent, the region near the cathode becomes 'invisible' for the tunneling electrons, as shown in Fig. 19(b). This corresponds to the occurrence of the S-type I-V snapback and then OTS switching happens. In 2009, D. Kau et al., from Intel group has demonstrated a PCRAM cross point array with OTS as select device which exhibited high density and large endurance of 10^6 cycles [57]. Several threshold switching selectors based on different chalcogenide alloy materials have been reported [58, 59]. Lee et al. demonstrated a structure of Ti/AsTeGeSiN/Ti [60, 61]. The reported selectors show limited degradation after applying alternative pulse voltage stress at on-state and off-state conditions up to 10^8 cycles, for both 30x30 nm^2 and 0.5x0.5 m^2 cell sizes. As shown in fig. 20, the selector was successfully integrated with a TaOx based resistive memory element, a clearly improvement on the low-bias leakage current can be observed in the full 1S1R cell configuration, with the on/off state non-linearity projected to ~100 at readout condition. The selector off-state leakage current can be further reduced by applying post deposition annealing. Such impact is well explained by a PF conduction model, where the trap density in the chalcogenide alloy is strongly reduced after the thermal annealing [60]. Chalcogenide alloy is an interesting material system for selector implementation given by its volatile OTS behavior. However, such volatile switching strongly depends on the alloy components and their concentration. With different alloy combination, nonvolatile switching characteristics can also occur, e.g. Chalcogenide-based PCRAM cells, due to the local heat induced material crystallization effect. Thus, chalcogenide material composition has to be carefully tuned, so as the device shows only volatile switching for the selector applications.

Next to it, the off-state leakage current should be minimized for selectors to cut-off the leakage paths. However, this can be very challenging to achieve given the large defect density in the amorphous alloy materials, which would enhance the PF conduction at low bias.

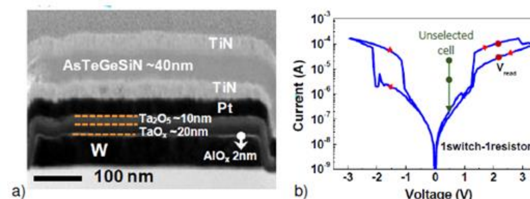


Fig. 20 (a) TEM picture of '1S +1R' device stack. (b) I-V sweeps of stacked 1S1R device. Inset: individual 1S, 1R cell behavior. Reprinted from [60].

2) *Metal-Insulator Transition (MIT)*

Metal-Insulator-Transition (MIT), is characterized by a fast, reversible transition between a low resistive metallic state and high resistive insulating state of an oxide [20]. This transition is triggered electrically or thermoelectrically, and was observed in transition metal oxides such as VO_2, NbO_2, etc. Son et al. presented Pt/VO_2/Pt selector, as shown in Fig. 21, showing moderate on/off non-linearity (~50), large drive current (>1 MA/cm^2), excellent switching uniformity during 100 switching cycles and fast switching speed (<20ns) [61].

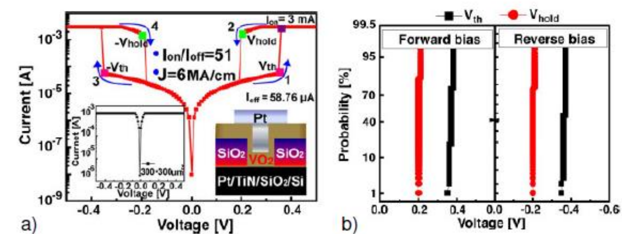


Fig. 21 (a) Typical threshold switching characteristics of Pt/VO_2/Pt selector in small 250nm hole structure. Inset: Linear I-V behavior of large micro-scale device. (b) CDF of threshold voltage (Vth) and hold voltage (Vhold) for 100 cycles. Reprinted from [61].

The MIT behavior is only observed in small size devices, while the large-area devices show ohmic I-V behavior as shown in the inset of fig. 21(a). This is possible due to the large defect density of the VO_2 layer, which increases the background leakage current. Although VO_2 exhibits excellent MIT behavior, its transition temperature is only around 67 °C [18]. A too low switching temperature makes it less suitable for practical applications at operating temperature up to 85 °C. In contrast to VO_2, NbO_2 based MIT selector remains stable up to 160 °C. Similar to VO_2, Pt/NbO_2/Pt selector, presented in fig. 22, shows excellent switching uniformity up to 1000 cycles [18]. The threshold voltage and the hold voltages are relatively

2168-6734 (c) 2016 IEEE. Translations and content mining are permitted for academic research only. Personal use is also permitted, but republication/redistribution requires IEEE permission. See http://www.ieee.org/publications_standards/publications/rights/index.html for more information.

This article has been accepted for publication in a future issue of this journal, but has not been fully edited. Content may change prior to final publication. Citation information: DOI 10.1109/JEDS.2016.2594190, IEEE Journal of the Electron Devices Society

larger compared to that of VO_2-based device, as observed from Fig. 22(b). A common concern for MIT based selectors is that the leakage current in the off-state is still very high. This can be attributed to the low band-gap specific to the MIT materials, which results in a low barrier height at the metal-oxide interface. On the other hand, such large off-state current is even necessary to enable Joule heating, as the transition is found to be thermally triggered in the reported cases.

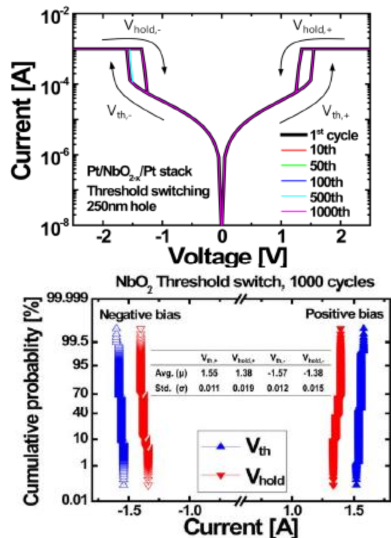


Fig. 22 (a) Threshold switching characteristics of $Pt/NbO_{2-x}/Pt$ selector in 250nm hole . (b) CDF of Vth and Vhold during 1000 consecutive DC cycles. Reprinted from [18].

3) *Field Assisted Superlinear threshold (FAST) selector*

Jo et al. reported a Field Assisted Superlinear threshold (FAST) selector utilizing a superlinear threshold layer (SLT) where a conduction path is formed at the threshold voltage and disappears below a hold voltage [62]. The threshold switching I-V behavior is characterized by an over 10^{10} nonlinearity (100 nmx100 nm), large drive current density exceeding 5×10^6 A/cm^2, excellent endurance of over 10^8 cycles and fast turn-on and off time less than 50 ns, etc. The FAST selectors are integrated with forming-free RRAM cells in a 4Mb 1S1R

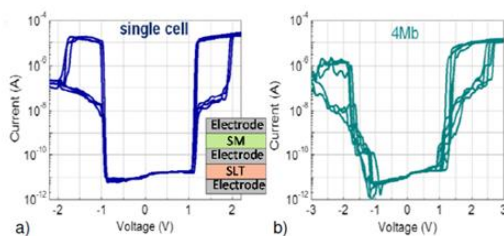


Fig. 23 Cross-point integration of RRAM devices with FAST selectors. (a) I-Vsweeps of a single 1S1R device. (b) I-V characteristics of multiple cells in 4Mbit cross-point array. Reprinted from [62].

crosspoint arrays. From fig. 23, the integrated 1S1R cell shows $>10^2$ on/off-state resistance window and ~10^6 selectively (half-bias current ratio) for both read and write conditions. The process temperature of FAST selector is less than 300 °C, which is suitable for 3D-stackable integration. In contrast to OTS and MIT based threshold switching selectors, FAST offers the largest on/off state current ratio. Although FAST selector shows excellent behaviors, the actual material system has not been revealed yet.

4) *Mixed Ionic-Electron Conduction (MIEC) selector*

Mixed Ionic-Electron Conduction (MIEC) occurs in materials that conduct both electronic charges and ions. Recently, Gopalakrishnan et al. reported selectors based on Cu-containing MIEC materials, where the MIEC layer is sandwiched between an inert bottom electrode (BEC) and top electrode (TEC) [63]. The applied voltage leads toa transient Cu ion movement, followed by steady electron/hole diffusion current, which generates strong non-linear I-V characteristics. With an optimized CMP process [64–66], the integrated MIEC selectors in large 512x1024 arrays at 100 % yield was achieved. The MIEC devices were integrated using diode-in-via method as shown in fig. 24(a) [64]. Bipolar DC I-V characteristics show ~1 pA leakage current near 0V and wide voltage range ~1.5 V with below 10 nA. Pulse measurements show that the MIEC devices can deliver maximum currents of over 100 A [64], which corresponds to a drive current density over 10MA/cm^2 for the reported selector size.

Thus, MIEC based selectors can offer the desirable

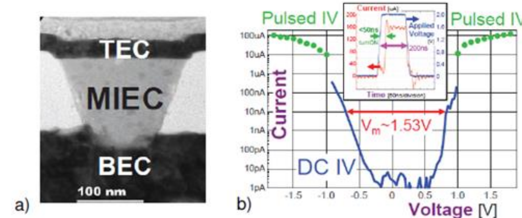


Fig. 24 (a) MIEC-based selectors with MIEC material sputter-deposited into a via hole, followed by CMP optimized process. (b) I-V characteristics of MIEC devices, the voltage margin (V_m) is defined as difference for reaching 10nA at positive/negative polarity. Reprinted from [64, 66].

combination of low off leakage current and high on current. At low-current (<10 A) stress condition, the MIEC selector can withstand over 1010 endurance cycles [63, 64]. At high-current stress, the voltage margin (V_m) degrades and eventually the selector becomes short-circuited, as observed in fig. 24 (b). TEM/EELS analysis implies endurance failure is possibly related to accumulation of Cu ions in the MIEC material [64]. Despite a Cu accumulation failure, another concern for MIEC-based selector is the low operating voltage range (or voltage margin). This makes MIEC selector less suitable for most of the resistive switching elements, which need to be programmed at relatively large voltages [29, 30].

2168-6734 (c) 2016 IEEE. Translations and content mining are permitted for academic research only. Personal use is also permitted, but republication/redistribution requires IEEE permission. See http://www.ieee.org/publications_standards/publications/rights/index.html for more information.

This article has been accepted for publication in a future issue of this journal, but has not been fully edited. Content may change prior to final publication. Citation information: DOI 10.1109/JEDS.2016.2594190, IEEE Journal of the Electron Devices Society

Table II: Performance of various reported selectors

Selector device/Parameters	ON current	Processing temperature	Non-linearity factor	Operation polarity
Si based pn diode selectors	>10MA/cm^2	>400 °C	> 10^5	Unipolar switching
Metal-insulator-Metal based selector	>1MA/cm^2	<400°C	>10^4	Bipolar
Threshold switching selectors	>10 MA/cm^2	<400°C	<10^3	Bipolar
FAST selector	>1MA/cm^2	<400°C	>10^5	Bipolar
MIEC selector	>10 MA/cm^2	< 400°C	>10^5	Bipolar

Comparison between different selectors:

The advantages and disadvantages of various kinds of selectors discussed above in terms of their important parameters are presented in Table II. The Silicon based selectors can provide a maximum drive current (J_{max}) to reach 10 MA/cm^2 current density. PN diode based on Si can provide a large half bias non-linearity (NL_{half}) of about 10^5. The main disadvantage of the Si based PN diode selectors is that they are not compatible with standard BEOL process as they need high temperature to fabricate. Another disadvantage is that they are suitable for unipolar switching only. To overcome this, Si NPN diodes can be fabricated but they are still incompatible with the standard BEOL process. Metal-oxide based schottky diodes are compatible with bipolar switching and compatible with standard BEOL process for fabrication. However, the NL_{half} is less than 10^3 and the J_{max} is also less than 1 MA/cm^2, which needed to be improved. Multi-layer tunneling layer based selector exhibits large J_{max}, high NL_{half}, bipolar switching and compatible with BEOL process. However the scalability and variability of these devices is still a challenge to obtain a high performance device. Threshold switch selectors shows bipolar switching, provides high J_{max} and compatible with BEOL process. However the complexity of the material system and small NL_{half} (< 10^3) makes OTS not suitable to use it in real time devices. Low transition temperature of the MIT selectors tends to the search of new materials to obtain high transition temperature for their future application. FAST selectors are the best systems to obtain all the requirements for a real time selector device. Currently, a challenging search for such a selector material is under intense investigation. MIEC selectors also offers all the requirements to make a best selector device, however the operating voltages of MIEC devices is very less which makes it incompatible to use with current RS elements.

VI. Summary

Non-linear characteristics are mainly generated by using the concept of complementary resistive switching, additional tunneling barrier and a Schottky barrier, or using an external select device. Interest on SRC originates from its simple structure. Most of the reported devices are compatible with VRRAM architecture, while the 1S1R cell configuration cannot fit for. To guarantee acceptable memory array performance, besides good memory properties, SRC operating a low program/erase voltage (current) and having highly non-linearity for both read and write operations are required. However, it seems very difficult to achieve all these performance targets at the same time for a single device. The reported SRCs can hardly fulfill the requirements from both memory properties and self-selectivity aspects. Recently, with the success of 3D VNAND in the mass production and its continuous development, industry is considering the SRC technology (so as the RRAM) being a long-term option for the VNAND successor. A separate selector device providing extra nonlinearity to the resistive memory elements should offer ultralow off leakage currents when the memory cells are unselected, and provide sufficient on-current for enabling the switching of the selected cell. To achieve high current, large non-linearity, good reliability under both device and process compatibility constraints remain challenge for selector device implementation.

Acknowledgment

This work was supported by the Ministry of Science and Technology, Taiwan, under Project No. 102-2221-E 009-134-MY3

References

[1] H. Nazarian and S. H. Jo, "Next generation non-volatile memory and its impact on system performance," in Standford EE computer systems colloquium, 2013.

[2] I. G. Baek, C. J. Park, H. Ju, D. J. Seong, H. S. Ahn, J. H. Kim, M. K. Yang, S. H. Song, E. M. Kim, S. O. Park, C. H. Park, C. W. Song, G. T. Jeong, S. Choi, H. K. Kang, and C. Chung, "Realization of vertical resistive memory (vrram) using cost effective 3d process," *in* IEEE *Electron Devices Meeting (IEDM)*, 2011, pp. 31–8.

[3] H. Tanaka, M. Kido, K. Yahashi, M. Oomura, R. Katsumata, M. Kito, Y. Fukuzumi, M. Sato, Y. Nagata, Y. Matsuoka, Y. Iwata, H. Aochi and A. Nitayama, "Bit cost scalable technology with punch and plug process for ultra high density flash memory,", *IEEE Symposium on VLSI Technology*, 2007, pp. 14–15.

[4] H. S. Yoon, I.-G. Baek, J. Zhao, H. Sim, M. Y. Park, H. Lee, G.-H. Oh, J. C. Shin, I.-S. Yeo, and U.-I. Chung, "Vertical cross-point resistance change memory for ultra-high density non-volatile memory applications," IEEE *Symposium on VLSI Technology*, 2009, pp. 26–27.

[5] S. G. Park, "Vertical reram technology for high density non-volatile memory," *5th IEEE Workshop on Innovative Memory Technologies*, 2013.

[6] G. Burr, R. Shenoy, P. Narayanan, K. Virwani, A. Padilla, B. Kurdi, and H. Hwang, "Access devices for 3-d crosspoint memory," *Journal of Vacuum Science Technology*, vol. (32)4, p. 040802, 2014.

[7] M.-J. Lee, Y. Park, B.-S. Kang, S.-E. Ahn, C. Lee, K. Kim, W. Xianyu, G. Stefanovich, J.-H. Lee, S.-J. Chung, et al., "2-stack 1D-1R cross-point structure with oxide diodes as switch elements for high density resistance ram applications," in *Electron Devices Meeting*, 2007, pp. 771–774.

[8] E. Linn, R. Rosezin, C. Kügeler, and R. Waser, "Complementary resistive switches for passive nanocrossbar memories," *Nature materials*, vol. 9, no. 5, pp. 403–406, 2010

[9] R. Rosezin, E. Linn, L. Nielen, C. Kügeler, R. Bruchhaus, and R. Waser, "Integrated complementary resistive switches for passive high-density nanocrossbar arrays*," IEEE Electron Device Letters,*, vol. 32, no. 2, pp. 191–193, 2011

[10] J. Lee, J. Shin, D. Lee,W. Lee, S. Jung, M. Jo, J. Park, K. P. Biju, S. Kim, S. Park, H. Hwang, "Diode-less nano-scale ZrOx/HfOx rram device with

2168-6734 (c) 2016 IEEE. Translations and content mining are permitted for academic research only. Personal use is also permitted, but republication/redistribution requires IEEE permission. See http://www.ieee.org/publications_standards/publications/rights/index.html for more information.

This article has been accepted for publication in a future issue of this journal, but has not been fully edited. Content may change prior to final publication. Citation information: DOI 10.1109/JEDS.2016.2594190, IEEE Journal of the Electron Devices Society

excellent switching uniformity and reliability for high-density cross-point memory applications," *in IEEE Electron Devices Meeting (IEDM),* 2010, pp. 19–5.

[11] M.-J. Lee, C. B. Lee, D. Lee, S. R. Lee, M. Chang, J. H. Hur, Y.-B. Kim, C.-J. Kim, D. H. Seo, S. Seo, et al., "A fast, high-endurance and scalable non-volatile memory device made from asymmetric ta2o5- x/tao2- x bilayer structures," *Nature materials*, vol. 10, no. 8, pp. 625–630, 2011.

[12] D. J. Wouters, L. Zhang, A. Fantini, R. Degraeve, L. Goux, Y. Y. Chen, B. Govoreanu, G. S. Kar, G. V. Groeseneken, and M. Jurczak, "Analysis of complementary rram switching," *IEEE Electron Device Letters,* vol. 33, no. 8, pp. 1186–1188, 2012

[13] Y. Chai, Y. Wu, K. Takei, H.-Y. Chen, S. Yu, P. C. Chan, A. Javey, and H.- S. P. Wong, "Nanoscale bipolar and complementary resistive switching memory based on amorphous carbon," *IEEE Transactions on Electron Devices,* vol. 58, no. 11, pp. 3933–3939, 2011

[14] F. Nardi, S. Balatti, S. Larentis, and D. Ielmini, "Complementary switching in metal oxides: Toward diode-less crossbar rrams," in *IEEE International Electron Devices Meeting (IEDM), 2011*, pp. 31–1.

[15] A. Fantini, L. Goux, R. Degraeve, D. Wouters, N. Raghavan, G. Kar, A. Belmonte, Y.-Y. Chen, B. Govoreanu, and M. Jurczak, "Intrinsic switching variability in hfo 2 rram," in *5th IEEE International Memory Workshop (IMW),* 2013, pp. 30–33.

[16] N. Raghavan, R. Degraeve, A. Fantini, L. Goux, D. Wouters, G. Groeseneken, and M. Jurczak, "Stochastic variability of vacancy filament configuration in ultra-thin dielectric rram and its impact on off-state reliability," *in IEEE International Electron Devices Meeting (IEDM),* 2013, pp. 21–1.

[17] S. Yu, X. Guan, and H.-S. P. Wong, "On the stochastic nature of resistive switching in metal oxide rram: Physical modeling, monte carlo simulation, and experimental characterization," *in IEEE International Electron Devices Meeting (IEDM),* 2011, pp. 17–3.

[18] S. Kim, X. Liu, J. Park, S. Jung, W. Lee, J. Woo, J. Shin, G. Choi, C. Cho, S. Park, et al., "Ultrathin (< 10nm) nb 2 o 5/nbo 2 hybrid memory with both memory and selector characteristics for high density 3d vertically stackable rram applications," in *IEEE Symposium on VLSI Technology (VLSIT),* 2012, pp. 155–156.

[19] X. Liu, S. M. Sadaf, S. Park, S. Kim, E. Cha, D. Lee, G.-Y. Jung, and H. Hwang, "Complementary resistive switching in niobium oxide-based resistive memory devices," *IEEE Electron Device Letters,* vol. 34, no. 2, pp. 235–237, 2013.

[20] M. Imada, A. Fujimori, and Y. Tokura, "Metal-insulator transitions," *Reviews of Modern Physics*, vol. 70, no. 4, pp. 1039, 1998.

[21] U. Chand, K.-C. Huang, C.-Y. Huang, and T.Y. Tseng, "Mechanism of Nonlinear Switching in HfO_2-BasedCrossbar RRAM With Inserting Large Bandgap Tunneling Barrier Layer", *Electron Devices, IEEE Transactions on*, vol. 62, no. 11, pp.3665, 2015

[22] S.-G. Park, M. K. Yang, H. Ju, D.-J. Seong, J. M. Lee, E. Kim, S. Jung, L. Zhang, Y. C. Shin, I.-G. Baek, et al., "A non-linear reram cell with sub-1μA ultralow operating current for high density vertical resistive memory (VRRAM)," *in IEEE International Electron Devices Meeting (IEDM),* 2012, pp. 20–8.

[23]] H. D. Lee, S. Kim, K. Cho, H. Hwang, H. Choi, J. Lee, S. Lee, H. Lee, J. Suh, S.-O. Chung, Y. S. Kim, K. S. Kim,W. S. Nam, J. T. Cheong, J. T. Kim, S. Chae, E.-R. Hwang, S. N. Park, Y. S. Sohn, C. G. Lee, H. S. Shin, K. J. Lee, K. Hong, H. G. Jeong, K. M. Rho, Y. K. Kim, S. Chung, J.Nickel, J. J. Yang, H. S. Cho, F. Perner, R. S. Williams, J. H. Lee, S. K. Park, S.-J. Hong., "Integration of $4f^2$ selector-less crossbar array 2 MB reram based on transition metal oxides for high density memory applications," *in IEEE Symposium on VLSI Technology (VLSIT),* 2012, pp. 151–152.

[24] B. Govoreanu, A. Redolfi, L. Zhang, C. Adelmann, M. Popovici, S. Clima, H. Hody, V. Paraschiv, I. P. Radu, A. Franquet, J. -C. Liu, J. Swerts, O. Richard, H. Bender, L. Altimime, M. Jurczak, "Vacancy-modulated conductive oxide resistive ram (vmco-rram): An area-scalable switching current, self-compliant, highly nonlinear and wide on/off-window resistive switching cell," *in IEEE International Electron Devices Meeting (IEDM*), 2013, pp. 10–2.

[25] R. Meyer, L. Schloss, J. Brewer, R. Lambertson, W. Kinney, J. Sanchez, and D. Rinerson, "Oxide dual-layer memory element for scalable non-volatile crosspoint memory technology," in *IEEE Non-Volatile Memory Technology Symposium,(NVMTS 2008),* 2008, pp. 1–5.

[26] C. J. Chevallier, C. H. Siau, S. F. Lim, S. R. Namala, M. Matsuoka, B. L Bateman, D. Rinerson, "A 0.13 *μ*m 64MB multi-layered conductive metal-oxide memory," in *IEEE International Solid-State Circuits Conference-(ISSCC2010)*, 2010, pp. 260–261.

[27] M. –C. Wu, Y. W. Lin, W. -Y. Jang, C. –H. Lin, T. –Y. Tseng, "Low-power and highly reliable multilevel operation in ZrO_2 1T1R RRAM," *IEEE Electron Device Letters,* Vol. 32,No. 8, pp.1026, 2011

[28] U. Chand, C. Y. Huang, D. Kumar, and T.-Y. Tseng, "Metal induced crystallized poly-Si-based conductive bridge resistive switching memory device with one transistor and one resistor architecture", Appl. Phys. Lett, vol. 107, pp. 203502, 2015

[29] L. Zhang, S. Cosemans, D. J. Wouters, G. Groeseneken, M. Jurczak, and B. Govoreanu, "Selector design considerations and requirements for 1 sir rram crossbar array," *in IEEE 6th International Memory Workshop (IMW),* 2014, pp. 1–4.

[30] P. Narayanan, G. Burr, R. Shenoy, K. Virwani, and B. Kurdi, "Circuit-level benchmarking of access devices for resistive nonvolatile memory arrays," *in IEEE International Electron Devices Meeting (IEDM),* 2014, pp. 29–7.

[31] J.H. Oh, J.H. Park, Y.S. Lim, H.S. Lim, Y.T. Oh, J.S. Kim, J.M. Shin, J.H. Park, Y.J. Song, K.C. Ryoo, D.W. Lim, S.S. Park, J.I. Kim, J.H. Kim, J. Yu, F. Yeung, C.W. Jeong, J.H. Kong, D.H. Kang, G.H. Koh, G.T. Jeong, H.S. Jeong, and Kinam Kim "Full integration of highly manufacturable 512MB pram based on 90nm technology," *in IEEE International Electron Devices Meeting(IEDM),* 2006. pp. 1–4.

[32] Y. Sasago, M. Kinoshita, T. Morikawa, K. Kurotsuchi, S. Hanzawa, T. Mine, A. Shima, Y. Fujisaki, H. Kume, H. Moriya**, N. Takaura and K. Torii, "Cross-point phase change memory with $4f^2$ cell size driven by low-contact-resistivity poly-si diode*," in 2009 IEEE Symposium on VLSI Technology,* 2009, pp. 24–25.

[33] K. Huet, C. Boniface, R. Negru, and J. Venturini, "Ultra low thermal budget anneals for 3d memories: Access device formation," *Proceedings of the 19th International Conference on Ion Implantation Technology*, *AIP Publishing,* vol. 1496, pp. 135–138, 2012

[34] V. Srinivasan, S. Chopra, P. Karkare, P. Bafna, S. Lashkare, P. Kumbhare, Y. Kim, S. Srinivasan, S. Kuppurao, S. Lodha, et al., "Punchthrough-diode-based bipolar rram selector by si epitaxy*," IEEE Electron Device Letters,* vol. 33, no. 10, pp. 1396–1398, 2012

[35] S. Lashkare, P. Karkare, P. Bafna, M. Raju, V. Srinivasan, S. Lodha, U. Ganguly, J. Schulze, and S. Chopra, "A bipolar rram selector with designable polarity dependent on-voltage asymmetry," in *IEEE International Memory Workshop (IMW),* 2013*,* pp. 178–181.

[36] M. Lee, C.-Y. Kao, C.-L. Yang, Y. Chen, H. Lee, F. Chen, and M. Tsai, "Reliability of ambipolar switching poly-si diodes for cross-point memory applications," *in IEEE Device Research Conference (DRC),* 2011, pp. 89– 90.

[37] S. Kim, D.-I. Moon, W. Lu, D. H. Kim, D. M. Kim, Y.-K. Choi, and S.-J. Choi, "Latch-up based bidirectional npn selector for bipolar resistance-change memory," *Appl. Phys. Lett.*, vol. 103, no. 3, pp. 033505, 2013.

[38] D. –Y. Lee, T.-L. Tsai, and T.-Y. Tseng, "Unipolar resistive switching behavior in Pt/HfO_2/TiN device with inserting ZrO_2 layer and its 1 diode-1 resistor characteristics", *Appl. Phys. Lett*. vol. 103, no. 3, pp. 032905, 2013.

[39] J.-J. Huang, Y.-M. Tseng, W.-C. Luo, C.-W. Hsu, and T.-H. Hou, "One selectorone resistor (1s1r) crossbar array for high-density flexible memory applications," *in IEEE International Electron Devices Meeting (IEDM),* 2011, pp. 31–7.

[40] J. -J. Huang, Y. -M. Tseng, C. W. Hsu, and T. H. Hou., "Bipolar nonlinear Ni/TiO_2/Ni selector for 1S1R crossbar arrary applications", *IEEE Electron Device Letters*, vol. 32, no. 10, pp. 1427–1429, 2011.

[41] J. Shin, I. Kim, K. P. Biju, M. Jo, J. Park, J. Lee, S. Jung, W. Lee, S. Kim, S. Park, et al., "Tio2-based metal-insulator-metal selection device for bipolar resistive random access memory cross-point application," *J. Appl. Phys.*, vol. 109, no. 3, pp. 033712, 2011.

[42] J. Shin, G. Choi, J.Woo, J. Park, S. Park,W. Lee, S. Kim, M. Son, and H. Hwang, "Mim-type cell selector for high-density and low-power cross-point memory application," *Microelectronic Engineering*, vol. 93, pp. 81–84, 2012.

[43] A. Kawahara, R. Azuma, Y. Ikeda, K. Kawai, Y. Katoh, Y. Hayakawa, K. Tsuji, S. Yoneda, A. Himeno, K. Shimakawa, T. Takagi, T. Mikawa, and K. Aono, "An 8 MB multi-layered crosspoint reram macro with 443 MB/s write throughput," *IEEE Journal of Solid-State Circuits,* , vol. 48, no. 1, pp. 178–185, 2013.

[44] A. Kawahara, R. Azuma, Y. Ikeda, K. Kawai, Y. Katoh, K. Tanabe, T. Nakamura, Y. Sumimoto, N. Yamada, N. Nakai, S. Sakamoto, Y. Hayakawa, K. Tsuji, S. Yoneda, A. Himeno, K. Origasa, K. Shimakawa, T. Takagi, T. Mikawa, and K. Aono, "An 8mb multi-layered cross-point reram macro with 443mb/s write throughput," *in IEEE International*

2168-6734 (c) 2016 IEEE. Translations and content mining are permitted for academic research only. Personal use is also permitted, but republication/redistribution requires IEEE permission. See http://www.ieee.org/publications_standards/publications/rights/index.html for more information.

This article has been accepted for publication in a future issue of this journal, but has not been fully edited. Content may change prior to final publication. Citation information: DOI 10.1109/JEDS.2016.2594190, IEEE Journal of the Electron Devices Society

Solid-State Circuits Conference Digest of Technical Papers (ISSCC), 2012, pp. 432–434.

[45] B. Govoreanu, C. Adelmann, A. Redolfi, L. Zhang, S. Clima, and M. Jurczak, “High-performance metal-insulator-metal tunnel diode selectors,” *IEEE Electron Device Letters,* vol. 35, no. 1, pp. 63–65, 2014.

[46] E. Cimpoiasu, S. Tolpygo, X. Liu, N. Simonian, J. Lukens, K. Likharev, R. Klie, and Y. Zhu, “Aluminum oxide layers as possible components for layered tunnel barriers,” *J. of Appl. Phys.,* vol. 96, no. 2, pp. 1088–1093, 2004.

[47] K. K. Likharev, “Layered tunnel barriers for nonvolatile memory devices,” *Appl. Phys. Lett.*, vol. 73, no. 15, pp. 2137–2139, 1998.

[48] W. Lee, J. Park, J. Shin, J. Woo, S. Kim, G. Choi, S. Jung, S. Park, D. Lee, E. Cha, H. D. Lee, S. G. Kim, S. Chung, and H. Hwang, “Varistor-type bidirectional switch (j_{MAX}>10^7 A/cm^2, selectivity ~10^4) for 3d bipolar resistive memory arrays,” *in IEEE Symposium on VLSI Technology (VLSI),* 2012, pp. 37–38.

[49]] J. Woo, W. Lee, S. Park, S. Kim, D. Lee, G. Choi, E. Cha, J. H. Lee, W. Y. Jung, C. G. Park, H. Hwang, “Multi-layer tunnel barrier (Ta_2O_5/TaO_x/TiO_2) engineering for bipolar rram selector applications*,” in IEEE Symposium on VLSI Technology (VLSIT),* 2013, pp. T168–T169.

[50] J. Woo, J. Song, K. Moon, J. H. Lee, E. Cha, A. Prakash, D. Lee, S. Lee, J. Park, Y. Koo, C. G. Park, H. Hwang, “Electrical and reliability characteristics of a scaled (30nm) tunnel barrier selector (W/Ta_2O_5/TaO_x/TiO_2/TiN) with excellent performance (j_{max}> 10^7 A/cm^2),” *in IEEE Symposium on VLSI Technology: Digest of Technical Papers,* 2014, pp. 1–2.

[51] S. R. Ovshinsky, “Reversible electrical switching phenomena in disordered structures,” *Phys. Rev. Lett.*, vol. 21, no. 20, pp. 1450, 1968.

[52] D. Kroll, “Theory of electrical instabilities of mixed electronic and thermal origin. ii. switching as a nucleation process,” *Phys. Rev. B*, vol. 11, no. 10, pp. 3814, 1975.

[53] D. Adler, H. K. Henisch, and N. Mott, “The mechanism of threshold switching in amorphous alloys,” *Reviews of Modern Physics*, vol. 50, no. 2, pp. 209, 1978.

[54] D. Adler, M. Shur, M. Silver, and S. Ovshinsky, “Threshold switching in chalcogenide-glass thin films,” *J. Appl. Phys.*, vol. 51, no. 6, pp. 3289–3309, 1980.

[55] D. Ielmini and Y. Zhang, “Analytical model for subthreshold conduction and threshold switching in chalcogenide-based memory devices,” *J. Appl.Phys.*, vol. 102, no. 5, pp. 054517, 2007.

[56] D. Ielmini, “Threshold switching mechanism by high-field energy gain in the hopping transport of chalcogenide glasses,” *Phys. Rev. B*, vol. 78, no. 3, pp. 035308, 2008.

[57] D. Kau, S. Tang, I. V. Karpov, R. Dodge, B. Klehn, J. A. Kalb, J. Strand, A. Diaz, N. Leung, J. Wu, S. Lee, T. Langtry, K. Chang, C. Papagianni, J. Lee, J. Hirst, S. Erra, E. Flores, N. Righos, H. Castro and G. Spadini, “A stackable cross point phase change memory,” in *IEEE International Electron Devices Meeting(IEDM),* 2009, pp. 617-620.

[58] J. Song, J. Woo, A. Prakash, D. Lee, and H. Hwang, “Threshold Selector With High Selectivity and Steep Slope for Cross-Point Memory Array”, in *IEEE Electron Device Letters*, vol. 36, no. 7, pp. 681–683, 2015.

[59] W. Chen, H. J. Barnaby, and M. N. Kozicki, “Volatile and Non-Volatile Switching in Cu-SiO2 Programmable Metallization Cells”, *IEEE Electron Device Letters*, vol. 37, no. 5, pp. 580–583, 2016.

[60] M.-J. Lee, D. Lee, H. Kim, H.-S. Choi, J.-B. Park, H. G. Kim, Y.-K. Cha, U.-I. Chung, I.-K. Yoo, and K. Kim, “Highly-scalable threshold switching select device based on chaclogenide glasses for 3D nanoscaled memory arrays,” *in IEEE International Electron Devices Meeting (IEDM),* 2012, pp. 2–6.

[61] M. Son, J. Lee, J. Park, J. Shin, G. Choi, S. Jung, W. Lee, S. Kim, S. Park, and H. Hwang, “Excellent selector characteristics of nanoscale for high-density bipolar reram applications,”*IEEE Electron Device Letters*, vol. 32, no. 11, pp. 1579–1581, 2011.

[62] S. H. Jo, T. Kumar, S. Narayanan, W. D. Lu, and H. Nazarian, “3d-stackable crossbar resistive memory based on field assisted superlinear threshold (fast) selector,” *in IEEE International Electron Devices Meeting (IEDM),* 2014, pp. 6– 7.

[63] K. Gopalakrishnan, R. S. Shenoy, C. T. Rettner, K. Virwani, D. S. Bethune, R. M. Shelby, G. W. Burr, A. Kellock, R. S. King, K. Nguyen, A. N. Bowers, M. Jurich, B. Jackson, A. M. Friz, T. Topuria, P. M. Rice, and B. N. Kurdi, “Highly-scalable novel access device based on mixed ionic electronic conduction (miec) materials for high density phase change memory (pcm) arrays,” in *IEEE Symposium on VLSI Technology; Digest of Technical Papers, 2010*,.pp. 205–206,.

[64] R. S. Shenoy, K. Gopalakrishnan, B. Jackson, K. Virwani, G. W. Burr, C. T. Rettner, A. Padilla, D. S. Bethune, R. M. Shelby, A. J. Kellock, M. Breitwisch, E. A. Joseph, R. Dasaka, R. S. King, K. Nguyen, A. N. Bowers, M. Jurich, A. M. Friz, T. Topuria, P. M. Rice, and B. N. Kurdi, “Endurance and scaling trends of novel access-devices for multi-layer crosspoint-memory based on mixed-ionic-electronic-conduction (MIEC) materials,” in *IEEE Symposium on VLSI Technology; Digest of Technical Papers*, 2011, pp. 94–95.

[65] G. W. Burr, K. Virwani, R. S. Shenoy, A. Padilla, M. BrightSky, E. A. Joseph, M. Lofaro, A. J. Kellock, R. S. King, K. Nguyen, A. N. Bowers, M. Jurich, C. T. Rettner, B. Jackson, D. S. Bethune, R. M. Shelby, T. Topuria, N. Arellano, P. M. Rice, B. N. Kurdi, and K. Gopalakrishnan., “Large-scale (512kbit) integration of multilayer-ready access-devices based on mixed-ionic-electronic-conduction (miec) at 100% yield,” *in IEEE Symposium on VLSI Technology; Digest of Technical Papers*, 2012, pp. 41– 42.

[66] K. Virwani, G. W. Burr, R. S. Shenoy, C. T. Rettner, A. Padilla, T. Topuria, P. M. Rice, G. Ho, R. S. King, K. Nguyen, A. N. Bowers, M. Jurich, M. BrightSky, E. A. Joseph, A. J. Kellock, N. Arellano, B. N. Kurdi and K. Gopalakrishnan, “Sub-30 nm scaling and high-speed operation of fully-confined access-devices for 3D crosspoint memory based on mixed-ionic-electronic-conduction (MIEC) materials*,” IEDM Tech. Dig*, 2012, pp. 36–39.

2168-6734 (c) 2016 IEEE. Translations and content mining are permitted for academic research only. Personal use is also permitted, but republication/redistribution requires IEEE permission. See http://www.ieee.org/publications_standards/publications/rights/index.html for more information.