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A three-dimensional simulation of electrostatic characteristics for carbon nanotube array field effect transistors

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Abstract

We, in this paper, study the electrostatic characteristics and the gate capacitances for carbon nanotube (CNT) array field effect transistors (FETs). The explored CNT-array FET is with three configurations of gate electrode, the top gate, the wrap around gate, and the bottom gate. Taking the pitch distance of structures and the gate length of CNT FET into consideration, a three-dimensional (3D) electrostatic simulation are performed by using an adaptive finite volume method, where different gate capacitance are calculated and compared. It is found that there is at least a 20% difference in calculating the gate capacitance between the 2D and 3D modeling and simulations. Our 3D simulation shows that a wrap around gate gives the largest gate capacitance among structures. A bottom gate possesses the weakest gate controllability. Effects of the pitch distance and the gate length on the gate capacitances of CNT-array FET are investigated. Results of the 3D electrostatic simulations can be applied to estimate the magnitude of the on-current of CNT FETs.

Keywords: Carbon nanotube array; Field effect transistor; Top gate; Warp around gate; Bottom gate; Electrostatic potential; Gate capacitance; 3D Modeling; Computer simulation

1. Introduction

Carbon nanotube (CNT) field effect transistors (FETs) with promising nanoscale device characteristics have recently been explored [1]. For ultra-small nanoscale FETs, CNT FETs have provided fascinating characteristics by comparing with silicon-based metal-oxide-semiconductor FETs (MOSFETs). Array of CNTs is one of effective ways to improve the performance of CNT FETs. Different structure and gate configuration of CNT array have been proposed for CNT FETs [1–11]. For CNT FETs with a planar bottom gate

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electrode configuration, the CNT is unpassivated [4,5,11]. The larger thickness of the back gate dielectric and the lower dielectric constant of the air surrounding the CNT result in a small gate-to-nanotube capacitance and produce the lower on-state current. For the top gate geometry, the CNT is covered by a gate insulator and demonstrates several advantages over the case of bottom gate [6,7], such as lower operating voltage due to a stronger coupling between the gate and the nanotube, and more flexibility to control individual devices. For CNT FETs with a wrap around gate [11], the CNT is surrounded by a cylindrical gate and this coaxial structure exhibits the strongest capacitive coupling between the gate and the tube. Among these three structures, it is known that single CNT can only contribute little driving current, array of CNT has been considered as a candidate to improve the electrical characteristics and physical properties (e.g., driving capability) of CNT FETs [1–11]. For an array of CNTs, the screening of the charge induced by CNTs significantly affects the electrostatic characteristics of structures, such as capacitance, in particular when many CNTs are in close proximity [1–11]. A unified investigation on the electrostatic characteristics with a multidimensional electrostatic simulation will clarify the main difference among three gate configurations of CNT-array FET and benefits the design and fabrication of CNT FET devices.

In this paper, we computationally study the electrostatic characteristics and the gate capacitance for an array of CNTs with three gate electrode configurations, the top gate (TG), wrap around gate (WG), and the bottom gate (BG). By solving the classical three-dimensional (3D) Laplace equation [12,13], the potential and electric field of structures are computed, where various gate capacitances are simultaneously extracted. The effect of structure's radius and the gate length of CNT FET on the gate capacitance are discussed and compared among structures.

It is found that there is about 20% difference in calculating the gate capacitance between the 2D and 3D modeling and simulations. Our 3D simulation shows that the structure with a top gate design demonstrates acceptable characteristics and wrap around gate has the best characteristics among structures. The 3D simulation shows that a wrap around gate gives the largest gate capacitance among structures. If we take the difficulties of fabrication into consideration, the top gate design may provide a compromise between device performance and manufacturability. A bottom gate possesses the weakest gate controllability. The pitch distance and gate length effects on capacitances are investigated. Results of the 3D electrostatic simulations can also be applied to estimate the magnitude of the on-state current of CNT FETs.

This paper is organized as follows. In Section 2, we state the computational model and the structures of array of CNTs. In Section 3, we discuss the simulation results. Finally, we draw conclusions and suggest future work.

2. Computational model and structures

We calculate the gate capacitance of a CNT array with three, TG, WG, and BG gate electrode configurations, shown in Figs. 1(a), (b), (c), respectively. Each CNT in an array has an identical radius $R = 0.7$ nm. The gate dielectric is assumed to be SiO2 with thickness 0.7 nm, where the dielectric constant is 3.9. These identical CNTs are placed in an array with a uniform spacing. Pitch is defined as the distance between two centers of any adjacent CNTs. By varying pitch, we study their electrostatic properties among three structures.

To focus on how screening by any two neighbor tubes affects gate-to-channel capacitance, the CNT is treated as a classical metal with equal potential over the tube [10]. Numerical results are computed by solving the 3D electrostatics of the CNT array. Taking the pitch distance of structures and the gate length of CNT FET into consideration, the 3D potential distribution and corresponding gate capacitance are calculated using the adaptive finite volume method [12,14,18]. To compute the capacitance of a conductor pair that is to calculate the charge, we apply the charge integration method. It assumes constant potentials at the electrodes and divides it by the potential difference. The gate-to-channel capacitances, such as the gate-to-end tube capacitance and the gate-to-middle-tube capacitance for an array of CNTs is analyzed for

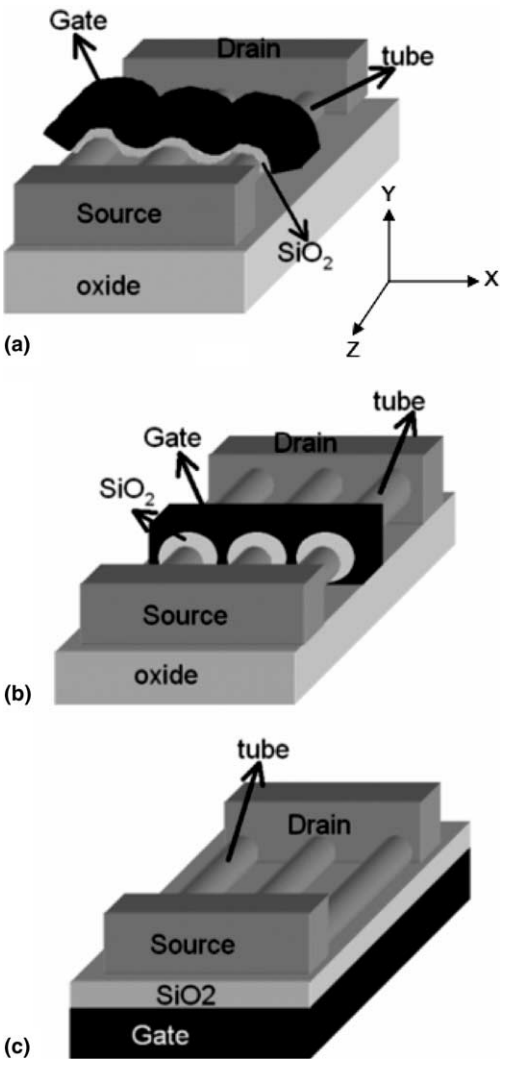

Fig. 1. Illustration of the three simulated: (a) TG, (b) WG, and (c) BG, configurations in the CNT-array FET, respectively.

different pitch, where the oxide thickness is fixed. The capacitance of gate-to-end tube is the capacitance between the gate and the end tube. The end tube can be the right tube or the left tube. The capacitance of gate-to-middle tube is the capacitance between the gate and the middle tube. Our results indicate the main trends to be expected for the gate to channel capacitance of an array of CNTs over a range of packing densities. Nevertheless, we note that any more accurate estimations on the gate capacitance should consider the quantum mechanical effects in the simulation model for the device with ultrathin insulators [15,16]. We believe that any inputs of quantum capacitance will result in more proper quantitative calculation; however, it cannot alter the main tendency discussed here. The classical approach shown here may have a sight overestimation on the capacitance compared with quantum collected approaches [10,15,16]. However, the difference between the classical and quantum mechanical simulation is quite small and it is decreased when the distance of pitch is increased [10].

3. Simulation results and discussion

Figs. 2(a), (b), (c) show the normalized contour plots for the three simulated CNT structures, respectively. The total length of tube is equal to 30 nm and the gate length is equal to 10 nm in this calculation. These contours have shown different electrostatic potential distributions; for the CNT FET with the WG configuration, the potential distributes uniformly in the channel region. The distribution of the surface potential is conformal among tube's surface for the TG configuration. A large potential variation appears in the BG setting and loses the distribution uniformity. Shown in Fig. 3, we plot the ratio of the capacitance calculated with the 2D and 3D modeling and simulations for the three structures. Both the gate-to-end-tube and gate-to-middle-tube capacitances are computed. It is found, for TG and WG configurations, there is about 20% difference in calculating capacitance between the 2D and 3D modeling and simulations whenever the pitch distance is varied. For BG case, the difference is significant for both capacitances. To explore the main difference among three gate configurations, our following calculations are, therefore, mainly based on the 3D modeling and simulation.

The gate-to-middle-tube capacitance and the gate-to-end-tube capacitance versus the pitch distance are calculated for the CNT-array FET with TG, WG, and BG configurations. The gate length of the CNT-array FET varies from 5 to 20 nm. Figs. 4(a) and (b) are the gate-to-middle-tube capacitance and gate-to-end-tube capacitance for

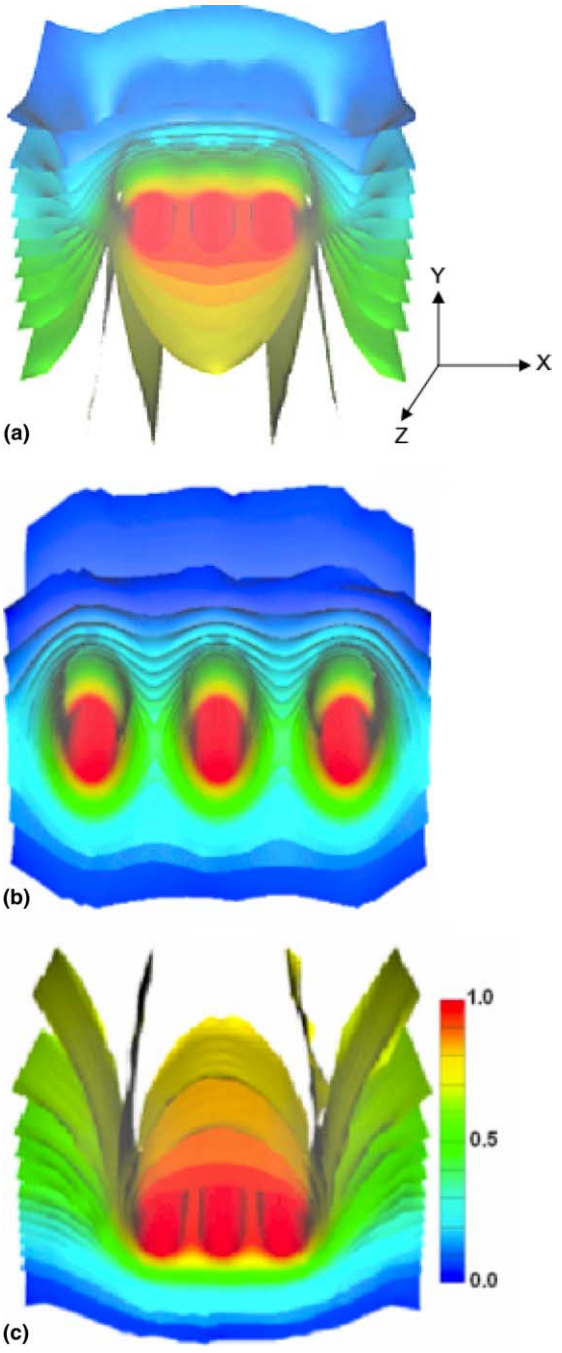

Fig. 2. The normalized contour plots of the 3D simulated electrostatic potential for the: (a) TG, (b) WG, and (c) BG configurations.

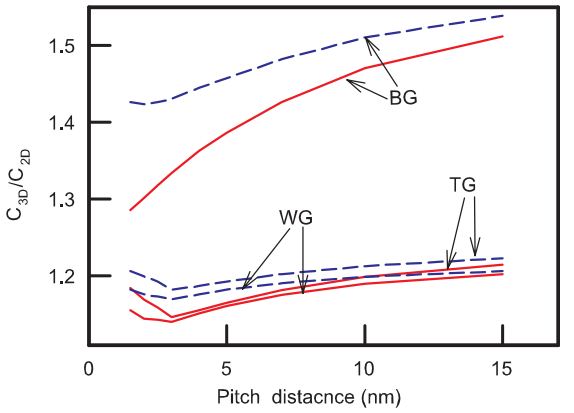

Fig. 3. The capacitance ratio of the 3D–2D simulation versus the pitch distance. The gate-to-end-tub (blue – dash line) and gate-to-middle-tube (red – solid line) capacitances versus the pitch distance are calculated for the three structures. The total length of tube is equal to 30 nm and the gate length is equal to 10 nm in this calculation.

the device with TG configuration. The gate-to-middle-tube capacitance is greater than that of the gate-to-end-tube capacitance due to a stronger field coupling effect appearing in the middle tube. For WG case, we find, shown in Figs. 4(c) and (d), they show the largest gate-to-middle-tube and gate-to-end-tube capacitances among three gate configurations due to it has the best uniform distribution of the potential. However, shown in Figs. 4(e) and (f), the BG configuration has the smallest gate-to-middle-tube and gate-to-end-tube capacitances. The capacitance difference among three gate configurations is reduced when the pitch distance approaches to the diameter of the tube shown in Fig. 5. The capacitance difference is increased and tends to a fixed value when the pitch distance is greater than 10 nm due to the weakened field coupling between any two adjacent tubes. For the CNT-array FET with 15 nm gate length, there is about 25% capacitance difference for both the gate-to-middle-tube and gate-to-end-tube capacitances between WG and TG configurations. The capacitance difference of the CNT-array FET with TG configuration is two times greater than that of BG case (more than 53%).

Taking TG configuration as an example, we calculate the gate-to-middle-tube capacitance versus the gate length of the CNT-array FET shown in

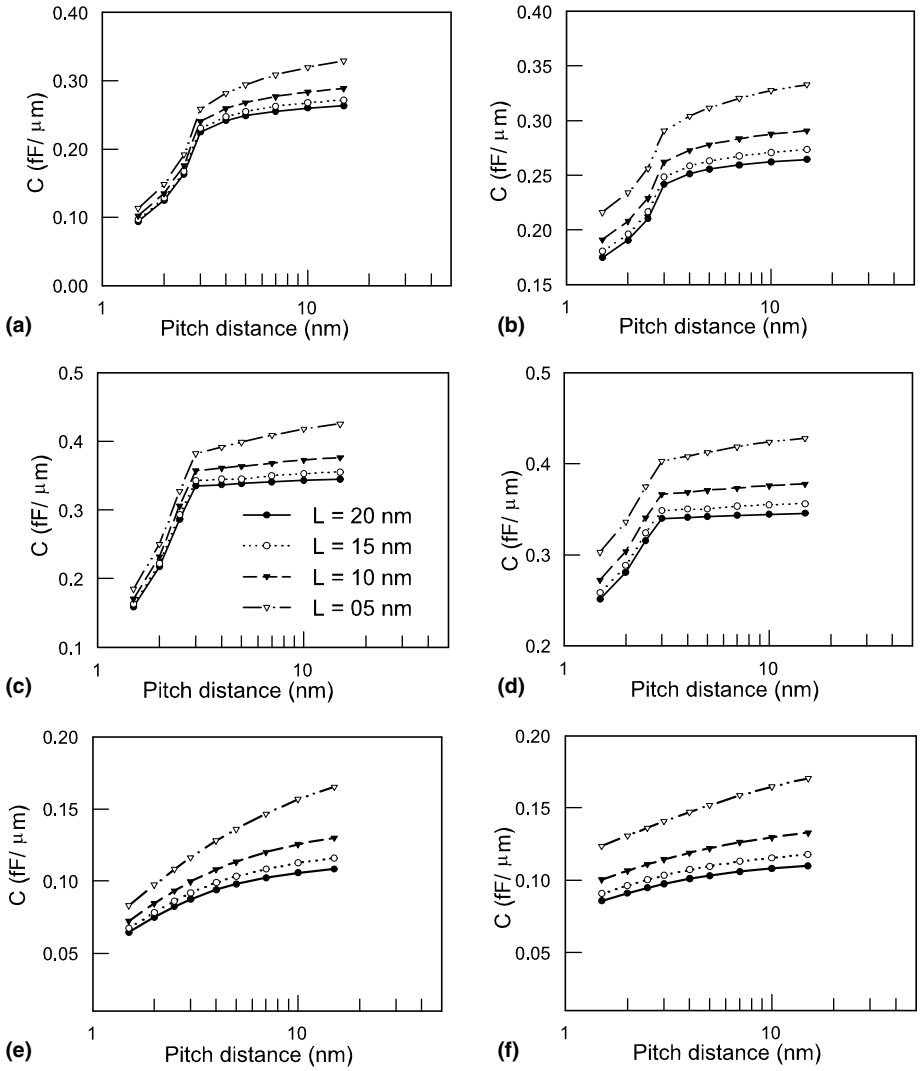

Fig. 4. For the TG configuration; (a) the gate-to-middle-tube and (b) the gate-to-end-tube capacitances versus the pitch distance. For the WG configuration; (c) the gate-to-middle-tube and (d) the gate-to-end-tube capacitances versus the pitch distance. For the BG configuration; (e) the gate-to-middle-tube and (f) the gate-to-end-tube capacitances versus the pitch distance. The CNT array FETs gate length varies from 5 to 20 nm.

Fig. 5. The calculation is with respect to different pitch distance ranging from 1.5 to 15 nm. For a given pitch distance, the gate-to-middle-tube capacitance is increased linearly when the gate length is increased. When the pitch distance is increased the slope of the capacitance is increased. The slope of the curve of the capacitance versus the gate length is also increased when the pitch distance is increased. However, the increase of the slope tends to a fixed function when the pitch distance is greater than 5 nm. We also calculate the fringing capacitance [17], shown in Fig. 6, the TG and WG configuration has very small but non-zero fringing capacitances. The fringing capacitance of the gate-to-end-tube and gate-to-middle-tube is increased when the pitch distance is increased to 20 nm. According to our 3D calculation, the CNT-array FET with BG configuration has almost zero value

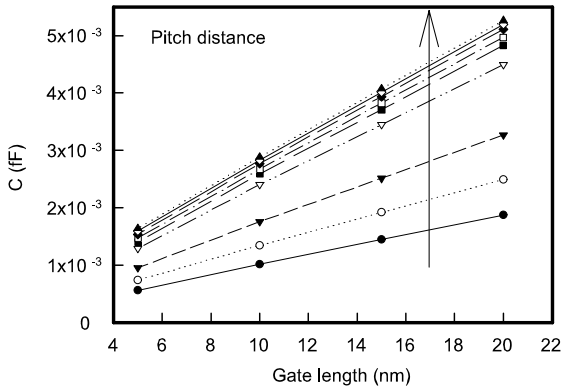

Fig. 5. The gate-to-middle-tube capacitance versus the gate length for the CNT array FET with TG configuration, where the pitch distance is from 1.5 nm (the lowest curve) to 15 nm (the highest one). They are 1.5, 2, 2.5, 3, 4, 5, 7, 10 and 15 nm, respectively.

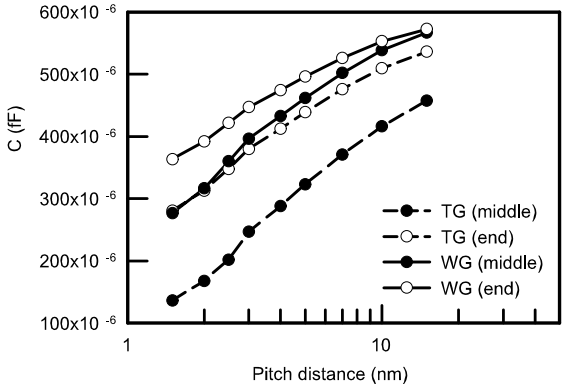

Fig. 6. The fringing capacitance the gate-to-end-tube and gate-to-middle-tube versus the pitch distance for the CNT array FET with TG and WG configurations.

(is about one order magnitude smaller than the others) of the fringing capacitance.

4. Conclusions

In this paper, we have simulated the gate capacitance of a array of CNTs with three, TG, WG, and BG, electrode structures. By considering the structure's pitch distance and the gate length of CNT FET into consideration, the 3D potential distribution and corresponding gate capacitance have been calculated using the adaptive finite volume method and the charge integration method. The 3D modeling and simulation plays an important role in theoretical investigation of CNT FET with small gate length. We found that there is about 20% difference in calculating capacitance between the 2D and 3D modeling and simulations. Our 3D approach has shown that the CNT structure with a TG design will provide an acceptable electrostatic characteristics and structure with a WG has the best characteristics among structures. The CNT structure with a WG has the largest gate capacitance among three structures, where the structure with a BG has the weakest gate controllability. The pitch distance and the gate length effects on capacitances have also been investigated and compared. We are currently including the quantum mechanical effect in our multidimensional simulation model for more accurate estimation on the electrostatic characteristics of CNT array FETs.

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