PAPER

A Varactor-Based All-Digital Multi-Phase PLL with Random-Sampling Spur Suppression Techniques

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SUMMARY This paper presents a varactor-based all-digital phase-locked loop (ADPLL) with a multi-phase digitally controlled oscillator (DCO) for near-threshold voltage operation. In addition, a new all-digital reference spur suppression (RSS) circuit with multiple phases random-sampling techniques to effectively spread the reference clock frequency is proposed to randomize the synchronized DCO register behavior and reduce the reference spur. Because the equivalent reference clock frequency is reserved, the loop behavior is maintained. The area of the proposed spur suppression circuit is only 4.9% of the ADPLL (0.038 mm^2). To work reliably at the near-threshold region, a multi-phase DCO with NMOS varactors is presented to acquire precise frequency resolution and high linearity. In the near-threshold region (V_{DD} = 0.52 V), the ADPLL only dissipates 269.9 μW at 100 MHz output frequency. It has a reference spur of −52.2 dBc at 100 MHz output clock frequency when the spur suppression circuit is deactivated. When the spur suppression circuit is activated, the ADPLL shows a reference spur of −57.3 dBc with the period jitter of 0.217% UI.

key words: *all-digital phase-locked loop, digitally controlled oscillator, low voltage, spur suppression, low jitter, low spur*

1. Introduction

The serious reference spurs of all-digital phase-locked loops (ADPLLs) are generated by the periodic updating on the digital control word of the digitally controlled oscillator (DCO). Large reference spurs will mix the signals from adjacent channels to degrade both transmitter and receiver performance [1]. The design tradeoff in an ADPLL between the fast lock-in time (large loop bandwidth) and the magnitude of in-band reference spurs is a critical issue.

There are several spur suppression techniques presented in traditional charge-pump phase-locked loops (CPPLLs) to improve spurious performance [2]–[6]. The magnitude of the reference spur can be estimated by the narrow band frequency modulation method [7] for CPPLLs. The relation between the spur amplitude A^C_{Spur} and the carrier amplitude $A^C_{Carrier}$ is determined as

$$\frac{A^C_{Spur}}{A^C_{Carrier}} = \frac{1}{2} \cdot \frac{K_{VCO} \cdot V_m}{2\pi \cdot f_{ref}}. \quad (1)$$

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where K_{VCO} (Hz/V) is the VCO gain, V_m is the ripple voltage and f_{ref} is the reference clock frequency. In [2], the distributed phase-frequency detectors (PFDs) and the charge-pumps (CPs) are used to decrease the magnitude of the ripples on the control line and acquire low-spur performance. However, the number of PFDs/CPs used is increased and there are mismatch issues. In [3], the randomized charge redistribution time in the charge-pump circuit and the doubling spur frequency are used to reduce the spurs. There are also mismatch and charge injection issues due to the charge redistribution. By utilizing a charge-distribution mechanism with an edge-interpolator that generates k sampling edges in a reference clock period on the control voltage of the VCO without using multiple PFDs or CPs, the spur performance is improved in [4]. Its methodology is similiar to the doubling spur frequency [3] with a different circuit design. In [5], the mechanism of reducing the VCO gain is presented to acquire lower spurious tone energy. A random clock generator is presented to randomize and average the CP output ripple to improve the spurs performance in [6]. The digital approach is used to equivalently increase the reference clock frequency and do the random choices of two updating frequencies. However, the mismatch issue is not resolved due to multiple PFDs.

Compared with the mixed-signal spur suppression methods used in CPPLLs, digital methods with novel signal processing schemes shall be proposed for ADPLLs. The relation between the spur amplitude A^D_{Spur} and the carrier amplitude $A^D_{Carrier}$ of ADPLLs can be modified from Eq. (1) to as

$$\frac{A^D_{Spur}}{A^D_{Carrier}} \propto \frac{K_{DCO} \cdot \Delta W_{DCO}}{f_{ref}}. \quad (2)$$

where K_{DCO} (Hz/LSB) is the gain of digitally controlled oscillators (DCOs), ?W_{DCO} is the difference of control code during updating the DCO frequency and f_{ref} is the reference clock frequency for ADPLLs. K_{DCO} in ring-type varactor-based DCOs is very difficult to be very small as compared with CPPLLs. The f_{ref} is a parameter in ADPLLs to determine the loop bandwidth. In this paper, a new all-digital spur suppression circuit with random-sampling techniques to effectively spread the reference clock frequency of the ADPLL is proposed to reduce the energy of the spurious tones. The method does not change the equivalent reference clock frequency.

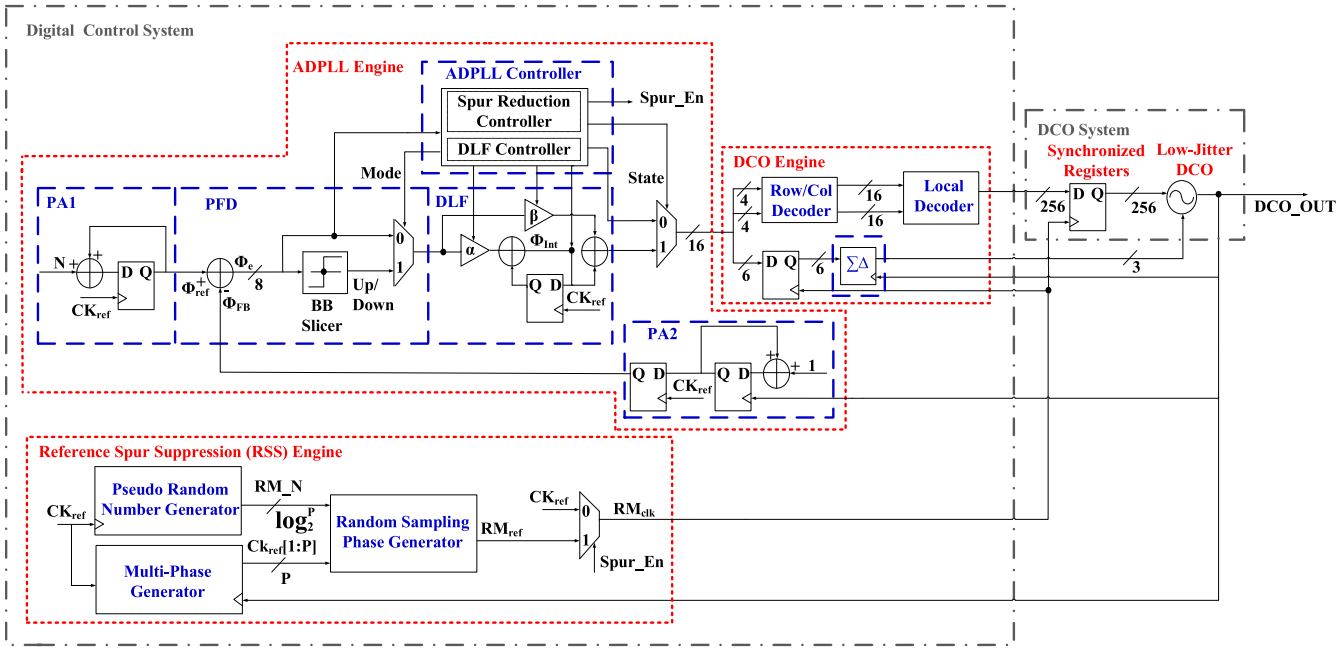


Fig. 1 Proposed varactor-based ADPLL architecture with random-sampling spur suppression techniques.

Well-characterized cells with layout are preferred than custom sized logic in varactor-based DCOs . The target application of the proposed ADPLL is used as clock generator for micro-controller or smart sensing applications [8], [9]. Power consumption can be reduced significantly at low voltage operation [10]. However, in advanced process technology, process, voltage, and temperature (PVT) variations on circuit performance are more serious [11] and PVT variations cause more than 10 times performance variation at the near-threshold voltage operation. Consequently, the DCO architecture with high reliability varactors is used in this design. The system application of the proposed ADPLL works at around 100 MHz for low power consumption with the voltage supply of 0.5 V from a DC-to DC buck converter. A closed-loop dynamic voltage frequency scaling (DVFS) is implemented to compensate PT variations. Moreover, with the supply voltage from 0.35 V to 0.5 V, the operational frequency can be from several MHz to around 100 MHz.

This paper is organized as follows: Section 2 describes the proposed ADPLL architecture with new random-sampling techniques for spur reduction. Section 3 shows the low-jitter DCO circuit and the design considerations. In addition, the architecture and the operation mechanism of spur suppression circuit are described in Sect. 3. The simulated ADPLL spectrum performance with RSS is also discussed in Sect. 3. Section 4 shows the experimental results. Finally, a summary regarding this work is concluded in Sect. 5.

2. Varactor-Based ADPLL Architecture with RSS

The proposed ADPLL architecture with division ratio N and reference spur suppression (RSS) circuit is shown in Fig. 1, which is divided into two modules. The first module is digital control system and the second module is the DCO system. The digital control system consists of three modules, an ADPLL engine, a DCO engine and an RSS engine. The ADPLL engine is composed of two phase-accumulators (PA1 and PA2), a phase-frequency detector (PFD), a programmable proportional (β) and integral (α) digital loop filter (DLF) and an ADPLL controller [12]. The DCO engine is composed of a $\Sigma\Delta$ modulator for dithering, a row/column thermometer code decoder and a local decoder. The proposed RSS is composed of a pseudo random number generator, a multi-phase generator, and a random-sampling phase generator. Finally, the DCO system consists of a low-jitter ring-based DCO and the synchronized registers.

2.1 Overview of Frequency and Phase Acquisition Mode

The whole lock-in procedures can be divided into four modes as shown in Fig. 2. The first is a frequency acquisition (FA) mode, the second is a phase acquisition (PA) mode, the third is a dithering mode [12] and the last is a proposed spur suppression mode. According to the design constraints, this system will switch modes automatically. In the FA mode, the DCO output signal (DCO_OUT) is used as the trigger clock signal for the frequency counters in PA2. The phase of the reference clock (CK_{ref}) and DCO_OUT are accumulated by PA1 and PA2. The PFD senses the phase difference (ϕ_e) between CK_{ref} and DCO_OUT by a subtractor. After capturing the phase difference between CK_{ref} and DCO_OUT, the DLF controller inside the ADPLL controller will activate the DLF and transmit adequate α/β according to the magnitude of the phase difference. In addition, the

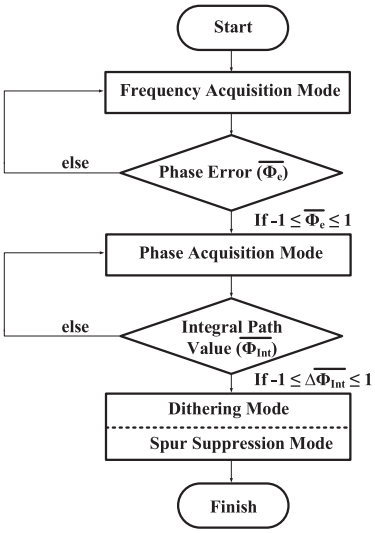


Fig. 2 ADPLL engine flow chart. $\overline{\phi_e}$ and $\overline{\phi_{int}}$ are long term average of ϕ_e and ϕ_{int}, respectively.

DCO frequency is updated and the frequency error is reduced when the DLF output value is mapped and converted to the DCO control code. In the PA mode, ϕ_e between CK_{ref} and DCO_OUT can be quantized and sent to the slicer to generate the Up/Down signal for filtering in the loop filter, as the design in [12], [13]. As a result, the phase error between CK_{ref} and DCO_OUT is also reduced.

2.2 Dithering and RSS Mode

After the system switches to the dithering mode, the ADPLL is in the lock-in state. A 14-bit signal is produced after the DLF operation and the first 8-bits of the 14-bit control code are transmitted to the row/column decoder in the DCO engine. The row/column decoder produces 16-bit row signals and 16-bit column signals. The local decoder receives the row and column signals to produce 256-bit signals which control 256 delay elements to update the DCO output frequency when the synchronized registers are triggered by RM_{clk}. In addition, the digital ΣΔ modulator produces 3-bit dithering signals to control the additional 3 delay elements. With the dithering mechanism, the equivalent frequency steps between two discrete frequencies are created due to the time-average concept. In consequence, the DCO frequency resolution is enhanced. The synchronized registers of the DCO control code are triggered at the rising edge of the reference clock signal (CK_{ref}).There are induced spurious tones in the frequency domain due to the updated and synchronized DCO behavior at fixed reference clock period.

Consequently, at the forth mode, the spur reduction controller inside the ADPLL controller will activate the spur suppression circuit to acquire the multi-phase reference clock signals (RM_{ref}) when the system is switched to the spur suppression mode. RM_{ref} have the same frequency with CK_{ref} but different randomly chosen phases are designed to replace the original reference clock source. Non-periodic

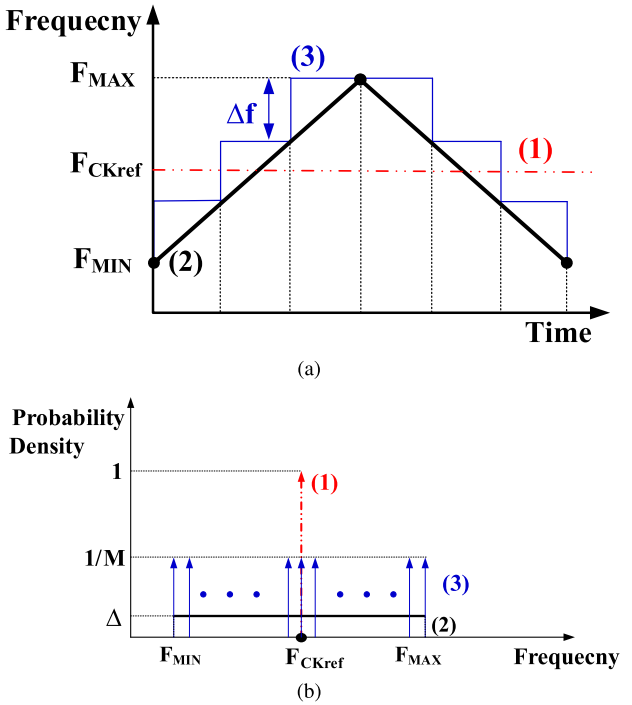


Fig. 3 (a) Different methods of (1) to (3) for providing reference clock frequency (CK_{ref}). (b) Probability density distribution comparison between different profiles for providing reference clock frequency (CK_{ref}).

signals are transmitted to RM_{clk} when Spur_En is set to one. In consequence, the DCO control code is updated according to RM_{ref} instead of CK_{ref}. Therefore, the synchronized DCO register behavior is randomized and the energy of spurious tones in the frequency domain is reduced.

Figure 3 (a) shows different profiles to provide RM_{clk} as the sampling clock for the synchronized registers. Method-(1) uses a fixed reference clock frequency (CK_{ref}). On the other hand, a continuous varying frequency with the triangular profile is used in method-(2). Compared with method-(2), M discrete varying frequencies with Δf/step are used in method-(3). The probability density distribution of different profiles for providing CK_{ref} are shown in Fig. 3 (b). The probability are one at F_{CKref} and zero at other frequencies in method-(1). The probability density distribution is uniform when method-(2) is used. The probability are Δ ($\Delta \ll 1$) at frequencies from F_{MIN} to F_{MAX}. Consequently, it implies the energy of reference spur can be reduced. However, the continuous varying frequency with the triangular profile is difficult to design due to the infinite frequency resolution and is certainly impossible for digital circuit design. Method-(3) uses M discrete frequencies to approximate the continuous profile and the probability at each frequencies are also reduced. However, the design overhead and the difficulty are increased when large M is used.

In this paper, a new all-digital spur suppression circuit based on method-(3) with multiple phases random-sampling techniques is presented to provide non-periodic signals (RM_{ref}). In consequence, the reference spur can be improved.

3. DCO and RSS Circuit Design

3.1 All-Digital Ring-Based Multi-Phase DCO Architecture

In [10] and [14], an array of tri-state inverters-based DCO architecture are used to work reliably over the wide PVT variations. In [15], an array of unit-sized PMOS drain capacitive loading cells are used as the DCO fine-tuning stage at the same purpose of working reliably under wide PVT variations. In [16], the binary-weighted varactor array is used to enlarge frequency range and improve jitter performance. In this paper, a unary-controlled varactor array is used to maintain a linear frequency response behavior through PVT variations. The ring-based multi-phase DCO architecture is shown in Fig. 4 (a). The unit cells of each stages are shown in Fig. 4 (b) and composed of driving inverters, cross-coupled inverters, a digitally controlled varactor array and a dithering part. The digitally controlled varactor array is composed of the varactor delay units. The minimum-sized NMOS in N-well varactor provided by the process design kit (PDK) is used as the capacitive loading and to guarantee the monotonic and good linearity. The dithering part also consists of the same varactor delay unit. This DCO architecture and circuit are very suitable for low-voltage V_{DD} because only inverters and unit-sized varactors are used.

The symmetry property must be preserved in the DCO layout to alleviate the mismatch caused by the local variation. In consequence, the 256 DCO control units are uniformly distributed in each stages of DCO to make the environment of them identical. Furthermore, the delay cells composed of the unary NMOS varactors instead of the binary-weighted varactors [16] are used to reduce the effect of the local variation and to maintain good linearity.

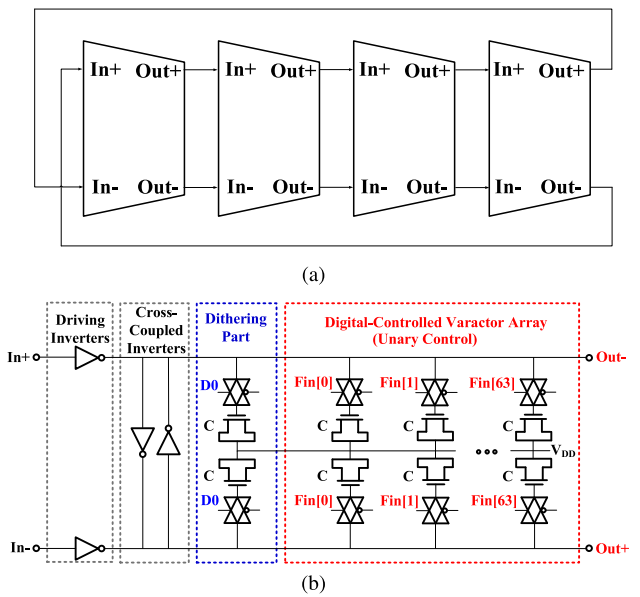


Fig. 4 The low-jitter DCO architecture and the unit cells of each multi-phase stages. (a) All-digital multi-phase DCO architecture. (b) The unit cells of each stages.

3.2 Random-Sampling Spur Suppression Circuit

The block diagrams of the spur suppression module is shown in the bottom left portion of Fig. 1. The pseudo random number generator produces the random sequence (RM_N) at every reference clock cycle. The multi-phase generator produces multi-phase reference clock signals ($CK_{ref}[1:P]$) based on the reference clock signal (CK_{ref}) by utilizing the DCO output clock signal to sample CK_{ref}. According to RM_N, the random-sampling phase generator determines one of $CK_{ref}[1:P]$ as the random-sampling clock signals (RM_{ref}). The spur suppression circuit utilizes RM_{ref} as the triggering source for the synchronized registers at every rising edge of RM_{ref} to update the DCO output frequency.

As a result, the fixed periodic behavior of updating DCO frequency is dispersed and the synchronized behavior is non-periodic. Therefore, the spurious tone in the original ADPLL output spectrum can be effectively suppressed. Because there is only one of the multi-phase signals delivered as RM_{ref} by the spur-suppression circuit within one reference clock period, the synchronization operation number of the synchronized registers triggered by RM_{ref} is the same in average as the number by CK_{ref}. This preserves the original loop stability and keeps the lock-in condition while disrupting the fixed-period synchronization behavior. The phase difference between the adjacent two multi-phase reference clock signals must in average equal to time period of the DCO output signal. If there are some phase difference, the spur suppression ability is degraded. In order to mitigate the effect of the phase error, the sampling clock signal must align to the reference clock signal in phase. That is why the DCO output clock signal (DCO_OUT) is used as the sampling clock source to sample CK_{ref}.

Figure 5 (a) shows the timing diagram and the relation of multi-phase number (P) and divider ratio (N), where $P \leq N$. One of the multi-phase signals ($CK_{ref}[1:P]$) is selected according to RM_N. The phase difference (ΔT) of the two rising edges of two selected consecutive multi-phase signals is located between ΔT_{min} and ΔT_{max}.

$$\Delta T_{max} = \left(1 + \frac{P-1}{N}\right) \cdot T_{Ckref}. \tag{3}$$

$$\Delta T_{min} = \left(1 - \frac{P-1}{N}\right) \cdot T_{Ckref}. \tag{4}$$

In addition, the probability density distribution of each $\Delta T/T_{CKref}$ is derived as the relation of N and P in Fig. 5 (b). Note that probability depends only on P and is independent of N. Furthermore, the number of discrete frequencies has the relation of 2P-1 and is independent of N.

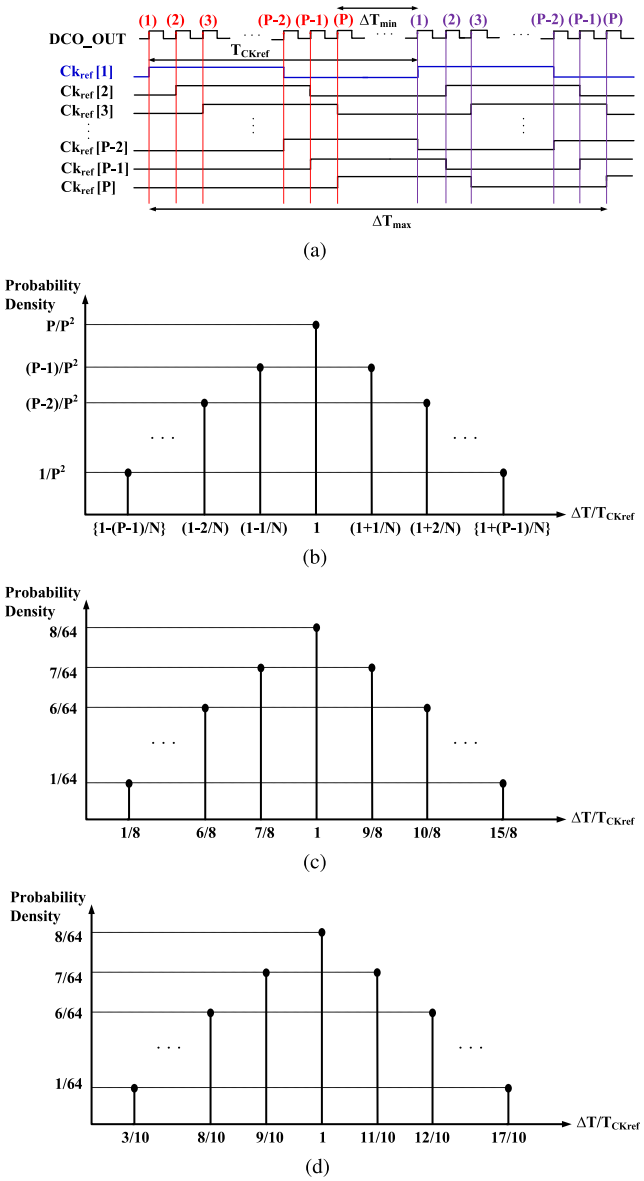


Fig. 5 (a)Timing diagram of $CK_{ref}[1:P]$ and DCO_OUT. (b) Probability density distribution of each sampling frequencies. (c) Probability density distribution with P=N=8. (d)Probability density distribution with P=8 and N=10.

From the probability density distribution, the probability is reduced to the value between 1/P and $1/P^2$. In consequence, the reference spur performance is improved with the increasing multi-phase number (P). The probability density distribution of $\Delta T/T_{CKref}$ is shown in Fig. 5 (c) when P and N are 8. The probability are 1/8, 1/64 and 1/64 when $\Delta T/T_{CKref}$ are 1, 15/8 and 1/8, respectively. Moreover, P is not necessary to be equal to N and can be any number with P ≤ N. From Fig. 5 (d), when P is 8 and N is 10, the probability are also 1/8, 1/64 and 1/64 when $\Delta T/T_{CKref}$ are 1, 17/10, and 3/10, respectively. With the same P, the number of discrete frequencies is equal no matter N is 8 or 10. However, the discrete frequency values are different. Therefore, the loop behavior and the spur improvement are not the same.

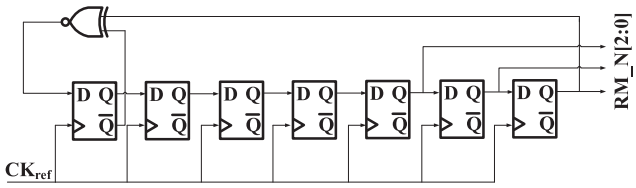


Fig. 6 Architecture of PRBS-based pseudo ransom number generator.

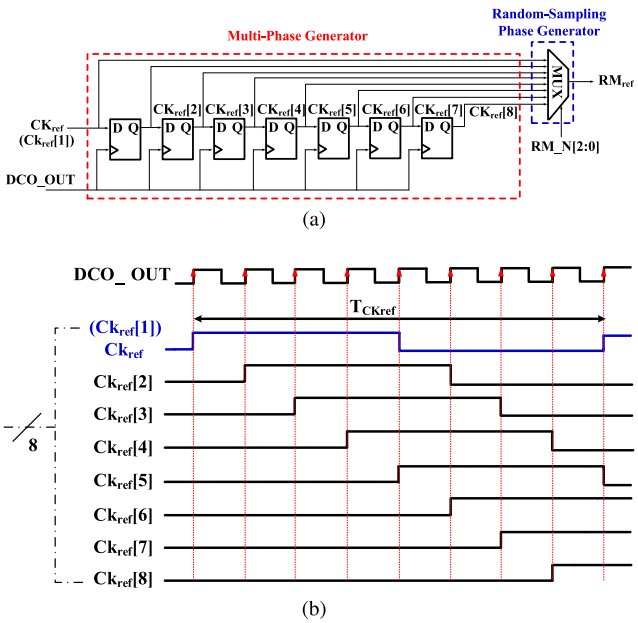
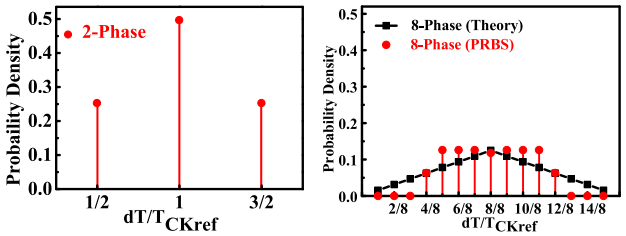


Fig. 7 (a) Architectures of multi-phase ganerator and random-sampling phase generator. (b) The basic operation concepts of the multi-phase ganerator and random-sampling phase generator.

The probability density distribution of $\Delta T/T_{CKref}$ is derived according to the assumption without considering the impact of α/β gain in the DLF.

In the chip implementation, P, N, f_{DCO_OUT}, f_{CKref} and α/β are 8, 10, 100 MHz, 10 MHz and (1/64)/(1/8), respectively. In addition, the target V_{DD} is 0.52 V. Pseudo-random binary sequence (PRBS)-based generator is used to provide the pseudo random number in this paper. The 7-bit PRBS-based generator used is shown in Fig. 6. A group of 3-bit random number signals is used in the spur reduction circuit as the pseudo random number. Figure 7 shows the architectures and the operation concepts of multi-phase generator and random-sampling phase generator. The multi-phase generator consists of seven delay elements (DFFs) to provide eight multi-phase reference clock signals based on the reference clock signal (CK_{ref}). The multi-phase reference clock signals are generated with the same reference clock frequency but different phase. Based on RM_N, the random-sampling phase generator (Multiplexer) selects one of these multi-phase signal as the random-sampling clock signals (RM_{ref}). In [2], the pulse-position modulation (PPM) is used and the periodic behavior on the control line is eliminated. However, the delay time (t_d) of each delay stage and the de-



(a) (b)

Fig. 8 Probability density distribution of (a) 2-Phase and (b) 8-Phase with the PRBS-based pseudo random number generator.

lay time difference cannot be determined precisely due to the local variation or the environmental mismatch. In this paper, the reference spur suppression performance can be improved with the increasing of multi-phase number (P). All-digital reference spur suppression is presented with low area overhead.

To verify the proposed spur suppression method, behavioral simulations with the same α/β of (1/64)/(1/8) and different P/N are carried out for 100 MHz output frequency. The reference spur of a 2-Phase system can be improved from −65.7 dBc to −68.67 dBc when N is 8. When N is 10, the reference spur of the 2-Phase system can be improved from −71.88 dBc to −74.97 dBc. Consequently, the spur suppression techniques can be operated in different reference clock frequencies.

Compared with the 2-Phase system, the reference spur is improved from −71.88 dBc to −77.02 dBc in an 8-Phase system when N is 10. The performance is better than that of the 2-Phase system. In consequence, the spur suppression techniques of the 8-Phase system is preferred. However, the improvement in the 8-Phase system is lower than the prediction due to the impact of α/β gain in the DLF.

The probability density distribution of $\Delta T/T_{CKref}$ in the 2-Phase and the 8-phase spur suppression systems are shown in Fig. 8. The number of discrete frequencies in the 8-phase system is more than that of the 2-Phase system. As a result, the reference spur improvement is superior in the 8-Phase system. However, several discrete frequencies are missing and the probability is higher in some discrete frequencies in the probability density distribution as compared with the theoretical analysis. This implies that the 3-bit random sequence from PRBS-based pseudo random number generator cannot be true randomness. The reference spur can be further improved if RM_{clk} with true randomness as the sampling clock is created for the synchronized registers. However, the design overhead is dramatically increased. According to the ADPLL spectrum shown in Fig. 9, there are rapid roll-off and flat regions. If RM_{clk} is created in the rapid roll-off region, RM_{clk} with true randomness can be used to improve the reference spur. On the other hand, if RM_{clk} is in the flat region, RM_{clk} with the proposed pseudo random number generator is efficient to acquire low spur as well as low area overhead.

The post-layout simulated ADPLL spectrum performance at 100 MHz are shown in Fig. 9. The reference spur at 10 MHz offset frequency is improved to −55.9 dBc from −50.8 below the main carrier of 100 MHz when the PRBS-based spur suppression circuit is activated. Moreover, the energy of spurious tones in the frequency domain are reduced and are redistributed to other frequency around the original spurious tones. Therefore, a higher noise floor is observed in the spectrum when the RSS circuit is activated. The jitter performance is degraded due to the RSS but is still very low.

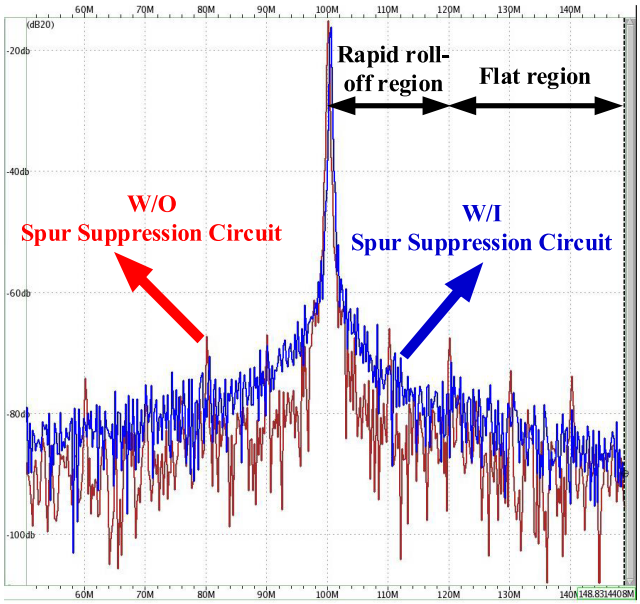


Fig. 9 Post-layout simulated ADPLL spectrum performance at 100 MHz when the PRBS-based spur suppression circuit is activated.

4. Experimental Rseults

The design of ADPLL test chip is implemented in LP-65 nm LVT CMOS process with the threshold voltage of 0.42 V. Figure 10 shows the die photo with layout. The active area is only 0.038 mm^2, which is composed of the digital control system (0.022 mm^2) and the DCO system (0.016 mm^2). The area of the presented spur suppression circuit is 4.9% of the active area. The ADPLL output waveform and spectrum performance are measured by Agilent sampling oscilloscope (MSO9404A) and Agilent spectrum analyzer (E4440A), respectively. All measurements are carried out with an external power source of 0.52 V V_{DD}, and digital tapped inverter chain buffers are used to transmit signals to the output pad. The power supply noise are about 120 mV_{p-p} and 100 mV_{p-p} for I/O and ADPLL core V_{DD}, respectively. This is to show the robustness of all-digital PLL.

4.1 Measurement of ADPLL w/o RSS Circuit

The measured characteristic curve of the multi-phase DCO at 0.52 V V_{DD} is shown in Fig. 11. This DCO shows good linearity and monotonic performance. In addition, the mea-

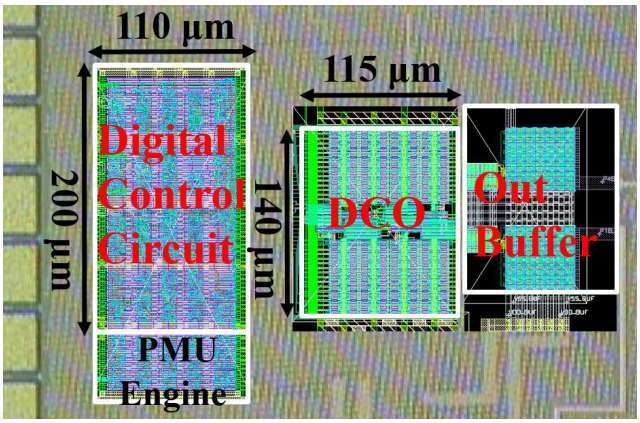


Fig. 10 Die photo and layout of the proposed ADPLL.

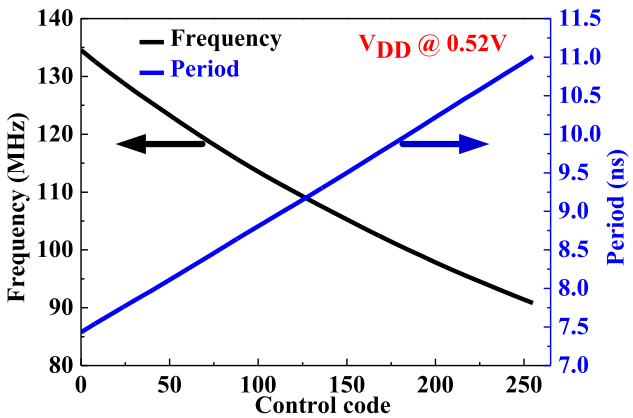


Fig. 11 The characteristic curve measurement of the multi-phase DCO at 0.52 V V_{DD}.

sured time-domain DCO resolution is 14 ps/LSB at 0.52 V V_{DD} operation and the LSB frequency resolution of the ADPLL output clock is only 252 KHz (0.19%) at maximum frequency (134.5 MHz). Moreover, the measured differential nonlinearity (DNL) and integral nonlinearity (INL) performance are shown in Fig. 12 to imply high linearity performance when NMOS varactors are used as the capacitive loading cells. The maximum DNL of ± 0.05 LSB under 0.52 V is better than the state of the art from [17], [18]. The maximum/minimum DCO frequency is 134.5 MHz/90.8 MHz and it consumes only 201.8 μW and 235.6 μW, respectively. As a result, the DCO architecture based on NMOS varactors has the advantages of high resolution and high linearity, which is suitable for low-jitter systems.

The ADPLL circuit dissipates 269.9 μW at 0.52 V V_{DD} when the ADPLL output frequency is 100 MHz with 10 MHz reference clock. With 10 MHz reference clock and the divider ratio of 10, the measured spectrum at 100 MHz under 0.52 V V_{DD} operation is shown in Fig. 13. The spurious tones at 10 MHz, 20 MHz and 30 MHz offset frequency are about −52.2 dBc, −53.8 dBc and −59.4 dBc below the main carrier when the spur suppression circuit is deactivated. The measured rms/peak-to-peak period jitter performance at 100 MHz are 16.5 ps (0.165 UI)/123.9 ps (1.239% UI) under

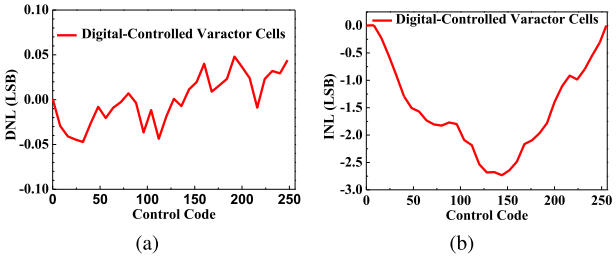


Fig. 12 (a) DNL and (b) INL characteristic measurement of the multi-phase DCO at 0.52 V V_{DD}

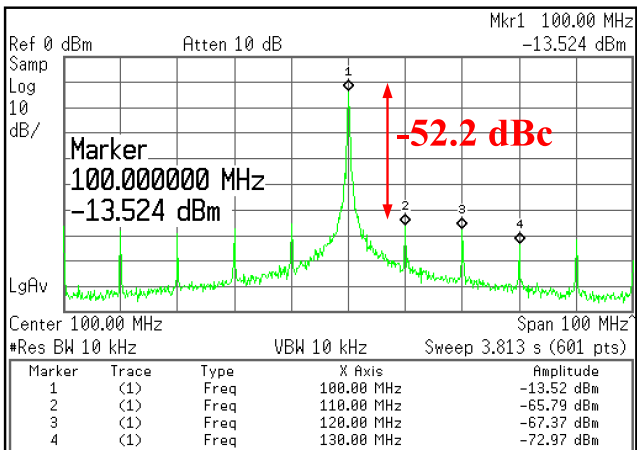


Fig. 13 A measured ADPLL spectrum performance at 100 MHz under 0.52 V V_{DD} when the PRBS-based spur suppression circuit is deactivated.

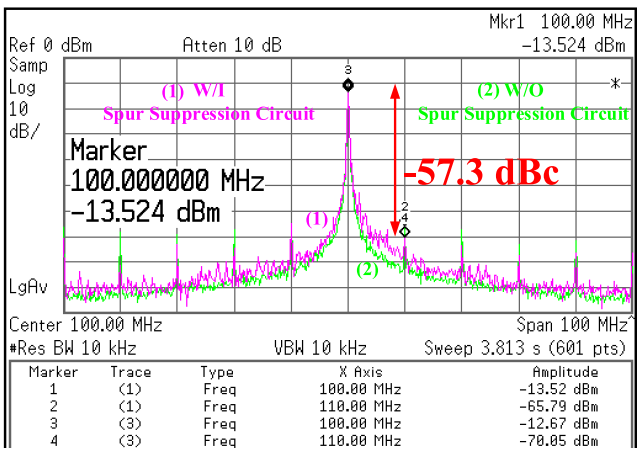


Fig. 14 Measured ADPLL spectrum performance at 100 MHz under 0.52 V V_{DD} when the PRBS-based spur suppression circuit is activated.

0.52 V V_{DD}. Therefore, the ADPLL architecture shows worse reference spurs when the spur suppression circuit is deactivated.

4.2 Measurement of ADPLL w/i RSS Circuit

The ADPLL spectrum performance at 100 MHz under 0.52 V V_{DD} is shown in Fig. 14 when the PRBS-based spur suppression circuit is activated. Table 1 summaries the spur

Table 1 Spur suppression performance summary at 100 MHz

V_{DD} (0.52V)	1st spurious tone	2nd spurious tone	3rd spurious tone
w/o spur reduction (dBc)	-52.2	-53.8	-59.4
w/i PRBS (dBc)	-57.3	-60.6	-64.8

Table 2 Near-threshold ADPLL with RSS circuit summary

Process Technology	CMOS 65_LP/LVT/1.2 V, V_{DD} = 0.52 V
Architecture	Differential Ring OSC.
Stage/Phase number	4/8
Bit Number	14bit (Dithering : 6bit)
DCO Frequency (MHz) ; F_{max}/F_{min}	90.8~134.5 ; 1.48
*** Energy per Cycle (pJ)**	2.699 (@ 100 MHz)
Reference Spur w/o RSS (dBc)	-52.2
Reference Spur w/i RSS (dBc)	-57.3
Period Jitter (RMS) w/i RSS (ps)/(UI)	21.7 /0.217% (@ 100 MHz)
Area (mm^2)	0.038 1) Digital controller : 110 µm × 200 µm (Spur reduction circuit :43 µm × 43 µm) 2) DCO : 115 µm × 140 µm

* Energy per Cycle (pJ) = Power (µW)/ Frequency (MHz)

suppression performance when the spur suppression circuit based on the PRBS random number generator is activated or deactivated. The reference spur improvement is about 5.1 dBc from −52.2dBc to −57.3 dBc. Moreover, the noise floor also increases in the spectrum when the RSS circuit is activated. The measured rms/peak-to-peak period jitter performance at 100 MHz are 21.7 ps (0.217 UI)/516.7 ps (5.167% UI) under 0.52 V V_{DD}. Consequently, the presented random-sampling spur suppression circuit can improve the spectrum performance and have low jitter performance as well.

Table 2 summarizes the key performance of the presented ADPLL when operating at the near-threshold supply voltage. The ADPLL architecture shows low jitter performance and the random-sampling spur suppression techniques are effective to suppress the spurious tones. The state of the art with low voltage ADPLLs in the literature are summarized in Table 3. Due to more bits, the proposed ADPLL has the least DCO gain and the best jitter performance with higher power consumption. Finally, the state of the art with spur suppression techniques in the literature are summarized in Table 4. However, there is no information in the literature about the reference spur suppression techniques used specifically in the ADPLLs. The state of the art with spur suppression techniques in the literature are from CPPLLs works. Although CPPLLs from [4] and [6] have superior reference spur performance, the parameters of loop bandwidth, reference clock frequency and the order of loop filter are related to spur performance. Different design specification also makes designers use different approaches to design. The proposed ADPLL is designed to acquire lower area and energy per cycle. The area overhead of the presented all-digital reference spur suppression circuit is only 4.9% (43 µm x 43µm) of the ADPLL. In addition, the reference spur performance is improved with the increasing multi-phase number (P). Therefore, all-digital approach can be used to extend the multi-phase number with lower overhead and to mitigate the mismatch issue.

Table 3 Low voltage ADPLL summary of the state of the art.

Performance indices	[8]	[9]	This work
nm/V_{th}/Supply voltage	40/X/0.9V, V_{DD} = 0.5 V	90/RVT/1.0 V, V_{DD} = 0.52 V	65_LP/LVT/1.2 V, (V_{DD} = 0.52 V)
DCO frequency range (MHz)	10 ~ 100	30 ~ 120	90.8 ~ 134.5 with 8 phases
Bit number	12	11	14
LSB resolution (KHz/LSB)	437	300	252
$Period_{RMS}$ jitter (ps)/(UI)	44.2/0.442% (@ 100 MHz)	26.8/0.322% (@ 120 MHz)	16.5/0.165% (@ 100 MHz)
FoM *	-220 dB @ 100 MHz	-225 dB @ 120 MHz	-221 dB @ 100 MHz
Oscillator approach	Ring DCO (CCO + DAC)	TDC-embedded	Ring DCO (Differential & Varactor)
Area (mm^2)	0.049	0.065	0.038

* FoM = 10xlog[(σ^2/1s)x(Power/1mW)

Table 4 Spur suppression PLL summary of the state of the art

Performance Indices	[2]	[4]	[6]	This work
nm/Supply Voltage	180/1.8V	180/1.8V	180/1.8V	65LP/1.2V (V_{DD} = 0.52V)
Architecture	CPPLL	CPPLL	CPPLL	ADPLL
DCO/VCO Frequency Range (MHz)	2400	700~1050	2200~2800	90.8~134.5
F_{max}/F_{min}	N.A.	1.50	1.27	1.48
Energy per Cycle (pJ)	7.500 @2.4GHz	33.110 @897MHz	7.491 @2.67GHz	2.699 @100MHz
DCO Resolution (KHz/LSB) or VCO gain (MHz/V)	N.A.	40 ~ 50	336	252
Reference Spur (dBc)	-55.0	-66	-72.0	-57.3
Loop Bandwidth (KHz)	N.A.	300	50	100
Reference Clock Frequency (MHz)	1	13	5	10
Oscillator Approach	LC-based	Ring VCO	LC-based	Ring DCO (Varactor-based)
Area (mm^2)	0.175	0.43	1.56	0.038 (Spur reduction circuit : 43 µm × 43 µm)

5. Conclusion

In this paper, a near-threshold operation ADPLL with a multi-phase and monotonic capability DCO is proposed in 65 nm CMOS process and is favorable for the low supply voltage applications. A new all-digital reference spur suppression (RSS) circuit with random-sampling techniques to effectively spread the reference clock frequency is presented to improve the spectrum performance and the low-jitter performance is reserved as well. As a result of using the same

equivalent reference clock frequency for spur suppression, the same loop behavior is maintained. The area of reference spur suppression is only 4.9% of the ADPLL with 0.038 mm^2.

Under 0.52 V V_{DD}, the ADPLL dissipates 269.9 μw at 100 MHz output clock frequency. The reference spur of −52.2 dBc is measured at 100 MHz output clock frequency when the spur suppression circuit is deactivated. When the spur suppression circuit is activated, the reference spur of −57.3 dBc at 100 MHz output clock frequency is measured with the rms period jitter of 21.7 ps (0.217%). Consequently, the reference spur improvement of 5.1 dBc and the low jitter performance below 0.3% UI at 100 MHz output clock frequency make the proposed ADPLL suitable in low-jitter and low-spur applications.

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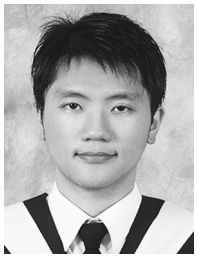

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