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Modification of intrinsic defects in IZO/IGZO thin films for reliable bilayer thin film transistors

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Dual active channel IZO/IGZO thin film transistors as such and with ZnO interlayer are fabricated and characterized to investigate the impact of ultra-thin ZnO insertion on their performance and bias stability. The ZnO interlayer suppresses the pre-existing divalent zinc vacancies and oxygen vacancies in the IZO front layer as systematically investigated by photoluminescence and XPS analysis. This interlayer leads to an enhancement of the electrical characteristics and stability of the bilayer TFT in comparison to the counterpart TFTs fabricated by a single IZO and a-IGZO-channel device. A high-field effect mobility (~14 $cm^2\ V^{-1}\ s^{-1}$) IZO/IGZO transistor with excellent photo-bias stability ($\Delta V_{th} \sim -2.45$ V) was obtained from 2 nm ZnO insertion in between the IZO and IGZO layer-enabling backplane electronics for high-resolution and large-sized AMOLED and TFT-LCD displays.

1. Introduction

Zinc oxide based TFTs receive considerable attention and have emerged the most promising candidates in pixel arrays, acting as either switching or driving forces for next generation displays due to their low process temperature, excellent uniformity, high electron mobility, low leakage current, compatibility with the conventional a-Si TFT fabrication process, low fabrication cost, transparency to visible light, compatibility with flexible substrates, and feasibility for solution processing.[1] The peripheral and pixel circuit design of the displays requires a TFT with high mobility, low threshold voltage and excellent stability. However, the high instability of zinc oxide TFT to photo-bias is the utmost issue that must be resolved to apply the TFT in such applications. The photo-biased instability was improved by using: (1) a high quality gate insulator *viz.*, SiO_2, Al_2O_3 deposited by plasma enhanced chemical vapor deposition (PECVD); (2) choosing the appropriate passivation layer on back channel; and (3) incorporation of carrier suppressors such as Zr, Hf, Ga, and Sn.[2–6] Consequently, the trade-off relationship between mobility and photo-bias stability in a single channel makes it difficult to produce oxide TFTs with both good bias stability and high field-effect mobility. As an alternative approach, double channel structures of IZO/HIZO, GZO/IGZO, IZO/IGZO were proposed to obtain high mobility and stability.[7–9] Double-stacked hafnium doped indium zinc oxide (HIZO thickness ~ 50 nm) was realized on gate insulator of SiN_x (400 nm)/SiO_x (50 nm) through r.f. sputtering at room temperature in Ar/O_2 (1 : 10) ambient at a chamber pressure of 3 m Torr and an r.f. power of 80 W to propose a-HIZO TFT with a staggered bottom gate structure. The resulting TFT showed high field effect mobility ~15 $cm^2\ V^{-1}\ s^{-1}$ with better stability ($\Delta V_{th} \sim -2.55$ V) under bias illumination.[10] Chong *et al.*, prepared a highly doped, buried layer of gallium–zinc–oxide (GZO thickness ~ 25 nm) in an a-IGZO channel layer (thickness ~ 25 nm) at 200 °C in Ar ambient to resulting in a TFT with field effect mobility ($\mu_{FE} \sim$ 10.04 $cm^2\ V^{-1}\ s^{-1}$), subthreshold swing (SS ~ 0.93 V per decade), threshold voltage ($V_{th} \sim 1.2$ V), and good bias-temperature-stress stability ($\Delta V_{th} = 0.94$ V).[8] Ding *et al.*, prepared an IZO (5 nm)/IGZO (17 nm) dual-active-layer for low voltage driving and high mobility thin film transistors on an Al_2O_3 (thickness ~ 150 nm) gate insulator grown at 250 °C by an atomic layer deposition (ALD) process. The TFT showed reliable performance ($\mu_{FE} \sim 14.4\ cm^2\ V^{-1}\ s^{-1}$, SS ~ 0.13 V per decade, $V_{th} \sim 0.8$ V) with excellent temperature stress stability ($\Delta V_{th} \sim$ 0.51 V).[9] Liu *et al.*, fabricated an In_2O_3/IZO bilayer metal oxide TFTs based on ultra-thin (5.5 nm) UV-cured amorphous ZrO_x dielectrics. The TFT showed high-transistor performance with a field-effect mobility of 37.9 $cm^2\ V^{-1}\ s^{-1}$, an on/off current ratio of 10^9, a subthreshold swing voltage of 0.12 V per decade, and a voltage shift of 0.4 V under positive bias stress for 2.5 h, for a gate voltage of 3 V and a drain voltage of 1 V.[11] However, they did not show negative-biased illumination stress stability tests. Recently, H. Y. Jung *et al.*, fabricated dual active channel IZO (5 nm)/ZTO (35 nm) TFT and suggested that the superior photo bias stability ($\Delta V_{th} \sim 4.1$ V) in the device was caused by suppression in oxygen vacancies due to Sn inter-diffusion in the IZO layer during thermal annealing at 500 °C.[6] Yen *et al.*, studied the gettering effect induced by oxygen deficient titanium oxide in the IZO and IGZO channel for low power display applications. They observed that the IGZO (10 nm)/TiO_x (5 nm)

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system exhibits superior transfer characteristics including a low sub-threshold swing of 79 mV per decade, a very high mobility of 68 $cm^2 V^{-1} s^{-1}$, and good on/off-current ratio of 5.61×10^6. However, the IZO (10 nm)/TiO_x (5 nm) system showed poor transistor characteristics with a linear field effect mobility of 8 $cm^2 V^{-1} s^{-1}$, a sub-threshold swing of 0.57 V per decade, and an on/off-current ratio of 1.05×10^4 due to the generation of excess oxygen vacancies originating from In–O, Zn–O bonds, and grain-boundary-assisted defects.[12] In this paper, ultra-thin ZnO seed layers were introduced in between the IZO/IGZO dual channel to study the impact of the seed layer on defects to affect the performance and negative biased illumination stress stability of the TFT fabricated on SiO_2 as a gate dielectric.

2. Experimental

Indium zinc oxide (IZO), indium gallium zinc oxide (IGZO), their bilayer thin films without and with ZnO interlayer were deposited at room temperature on glass and SiO_2 (100 nm)/Si (p-type) substrates by a sequential r.f. magnetron sputtering deposition technique in an Ar : O_2 environment. For this, the sputtering chamber was evacuated to 3×10^{-6} mbar before introducing the Ar : O_2 (flow rates $\sim$ 10 : 0.6 sccm) gas to maintain the chamber pressure of ~3 m Torr for sputtering of IZO, IGZO, and ZnO targets at a rate of ~3.6, 3.6, and 1.8 Å s^{-1}, respectively, using the same r.f. power of 80 W. Their structure, morphology, and surface composition were investigated using an X-ray diffractometer (XRD, Bede-D1), a transmission electron microscope (TEM, JEOL-JEM-2100F), and an X-ray photoelectron spectroscope (XPS, PHI 5000 versa probe II with monochromatic Al Kα radiation, 1486.6 eV), respectively. Furthermore, the photoluminescence of films deposited on glass substrates was measured with a fluorescence spectrometer (Edinburgh Instruments, M300 Monochromator, Xe 900). The resulting films of IZO (5 nm), IGZO (25 nm), IZO/IGZO (5 nm/25 nm), and IZO/ZnO/IGZO (5 nm/2 nm/25 nm) on SiO_2/Si substrates were utilized as an active channel layer for TFT fabrication (Fig. 1). The drain and source were realized with ITO thin films ($t \sim 65$ nm) using shadow masks. The devices with an electrode width (W) of 1000 μm and channel length (L) of 200 μm were finally annealed at 300 °C for 1 h in N_2 environment. The electrical characterization was performed at room temperature in the dark using a semiconductor parameter analyzer (B1500A).

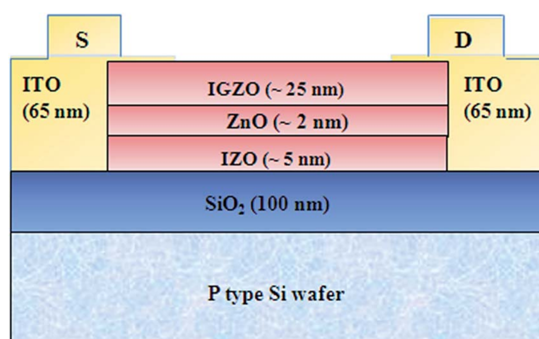

Fig. 1 Schematic diagram of TFT device.

3. Results and discussion

The XRD patterns (Figures are not shown here) of IZO, IGZO, and IZO/IGZO exhibited no diffraction peak. Meanwhile, broad, faint and asymmetric diffraction peaks corresponding to the (00l) planes of $InGaZnO_4$ were observed after inserting the ultra-thin ZnO seed layer (~2 nm) in a bilayer structure of IZO/IGZO. Nevertheless, ZnO was unable to change the nature of the film from amorphous to crystalline. For clear evidence of an amorphous phase, the IZO/IGZO and IZO/ZnO/IGZO thin films were analyzed using a high resolution transmission electron microscope (HRTEM). The cross-sectional images of the IZO/IGZO and IZO/ZnO/IGZO thin films on a SiO_2/Si substrate are shown in Fig. 2a and b, respectively. Selected electron diffraction patterns (insets of Fig. 2c and d) did not show any characteristic patterns indicative of an amorphous phase. The magnified images of IZO/IGZO and IZO/ZnO/IGZO thin films are shown in Fig. 2c and d, respectively. Note that the ZnO layer diffused within the bilayer films during annealing the film, due to high diffusion ability of zinc at high temperature,[13] leading two inhomogeneous contrasts near the interfaces (Fig. 2d). The zinc species diffused towards the more vacant sites in the IZO front layer; the IZO layer occupied more zinc vacancies than the back IGZO channel layer as confirmed from the XPS depth and PL analysis (discussed later). The diffusion ability of the ZnO

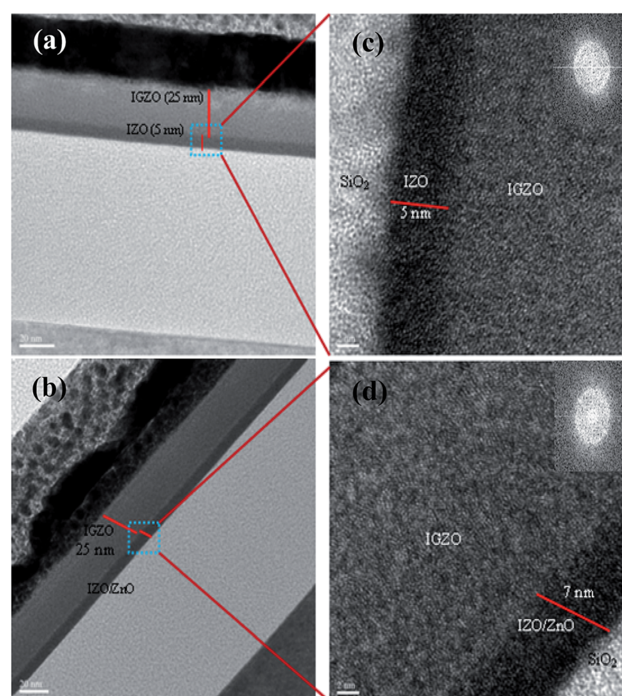

Fig. 2 HRTEM images and its Fourier transforms (FTs) in inset: (a) IZO/IGZO; (b) IZO/ZnO/IGZO; (c, d) magnified images of IZO/IGZO, and IZO/ZnO/IGZO films, respectively, after annealing at 300 °C for 1 h in nitrogen ambient.

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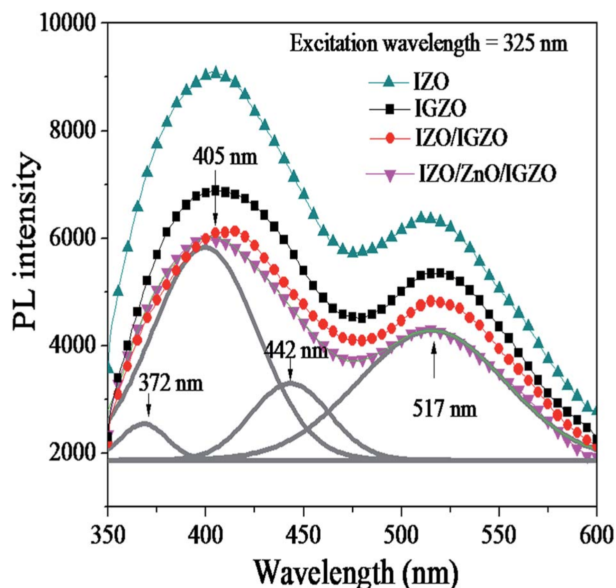

Fig. 3 Photoluminescence spectra of IZO (5 nm), IGZO (25 nm), IZO (5 nm)/IGZO (25 nm), and IZO (5 nm)/ZnO (2 nm)/IGZO (25 nm) thin films after annealing at 300 °C for 1 h in nitrogen ambient, displaying nearly similar characteristics and Gaussian fitting curves for the case of an IZO (5 nm)/ZnO (2 nm)/IGZO (25 nm) layer with peaks centered around 372, 405, 442, and 517 nm of possible defect levels.

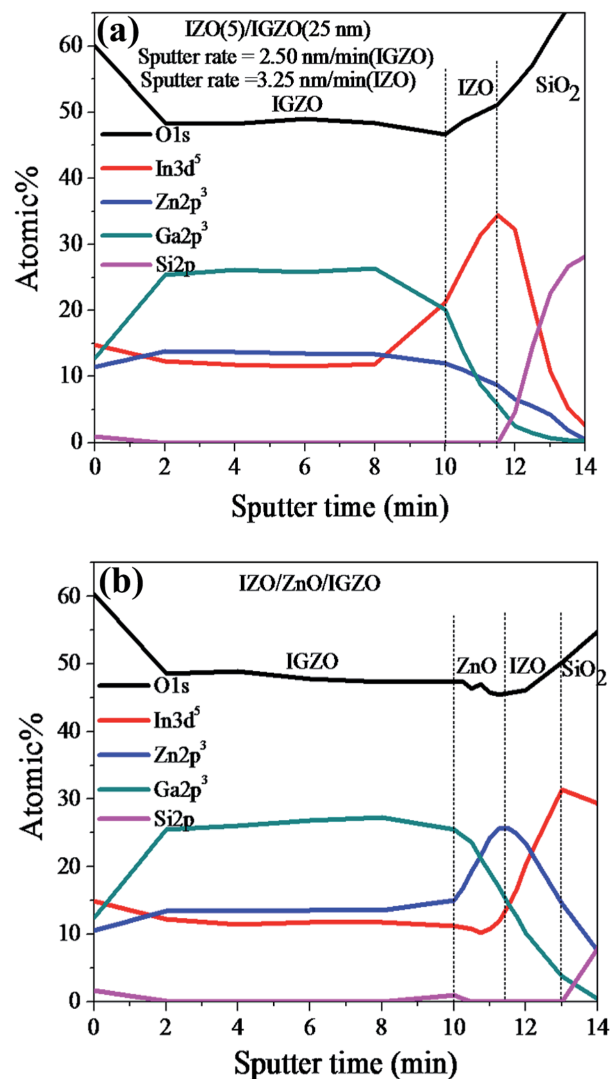

Fig. 4 XPS profile of O (1s), In ($3d^5$), Zn ($2p^3$), Ga ($2p^3$) and Si (2p) as a function of sputter time in (a) IZO (5 nm)/IGZO (25 nm), and (b) IZO (5 nm)/ZnO (2 nm)/IGZO (25 nm) layer structure.

seed layer leads a key role to modify the defect levels within the front channel of IZO for improving the performance and stability of thin film transistors. The nature and type of defects present in the films (Fig. 3) are analyzed by photoluminescence study. Note that all the films exhibit a broad and asymmetric PL spectrum extending from the ultraviolet (UV) to the visible region. The broad and asymmetric peak of IZO/ZnO/IGZO thin films was deconvoluted into four Gaussian curves centered at 372, 405, 442, and 510 nm (Fig. 3). The UV emission at 372 nm arises due to near band edge transition involving recombination of excitons. The green emission at 510 nm (2.43 eV) is attributed to the radiative recombination of a delocalized electron close to the conduction band with a deeply trapped hole in the oxygen vacancy (V_O^+).[14] The violet and blue emissions are primarily associated with zinc defects. The zinc defects include: (i) a neutral zinc vacancy (V_{Zn}^0) as a deep accepter at 0.3 eV above the valance band; (ii) a monovalent zinc vacancy (V_{Zn}^{1-}) as an acceptor with an energy level (0.3–0.7) eV above the valance band; and (iii) a divalent zinc vacancy (V_{Zn}^{2-}) and a monovalent interstitial zinc (Zn_i^+) as donors and located (0.4–0.7) eV below the conduction band.[15] Since the formation energy of zinc vacancies is low,[16] the violet emission at 405 nm (3.06 eV) and blue emission at 442 nm (2.80 eV) are attributed to neutral zinc vacancy and divalent zinc vacancy, respectively.[17,18] Note that the intensity of the blue emission peak at 442 nm is higher in the bilayer IZO/IGZO thin film; it is reduced in the IZO/ZnO/IGZO structure (Fig. 3). This indicates that the zinc species diffuse to fill the divalent zinc vacancy in the IZO/ZnO/IGZO structure, leading to a high quality of film, consistent with the high resolution TEM analysis. This fact is also justified by X-ray photoelectron spectroscopy (XPS). The depth-profile of the various elements in the IGZO/IZO/SiO_2 and IGZO/ZnO/IZO/SiO_2 stacks is shown in Fig. 4a and b. The zinc molar cation ratio, M_{Zn} = (Zn)/(In + Zn + Ga) in the IZO front channel layer of IGZO/ZnO/IZO/SiO_2 stack is higher ($M_{Zn} \sim 0.41$) than the IGZO/IZO/SiO_2 stack ($M_{Zn} \sim 0.19$) due to the high diffusion ability of zinc during annealing at 300 °C. This result suggests that the zinc vacancies, especially the divalent zinc vacancies, were depleted in the front IZO channel layer of the IGZO/ZnO/IZO/SiO_2 stack. On the other hand, the influence of the ZnO interlayer on the oxygen vacancy was studied by the evaluation of O 1s XPS spectra along the depth (Fig. 5a and b). The O 1s peaks deconvoluted into two Gaussian curves (continuous gray color) centered at binding energies of 530.5 ± 0.1 and 531.2 ± 0.6 eV arising from oxygen atoms in the oxide lattices (O_O) and from oxygen vacancies (V_O), respectively.[19] The ratio of the peak areas of V_O and O_O gives an estimate of oxygen deficiency. The value

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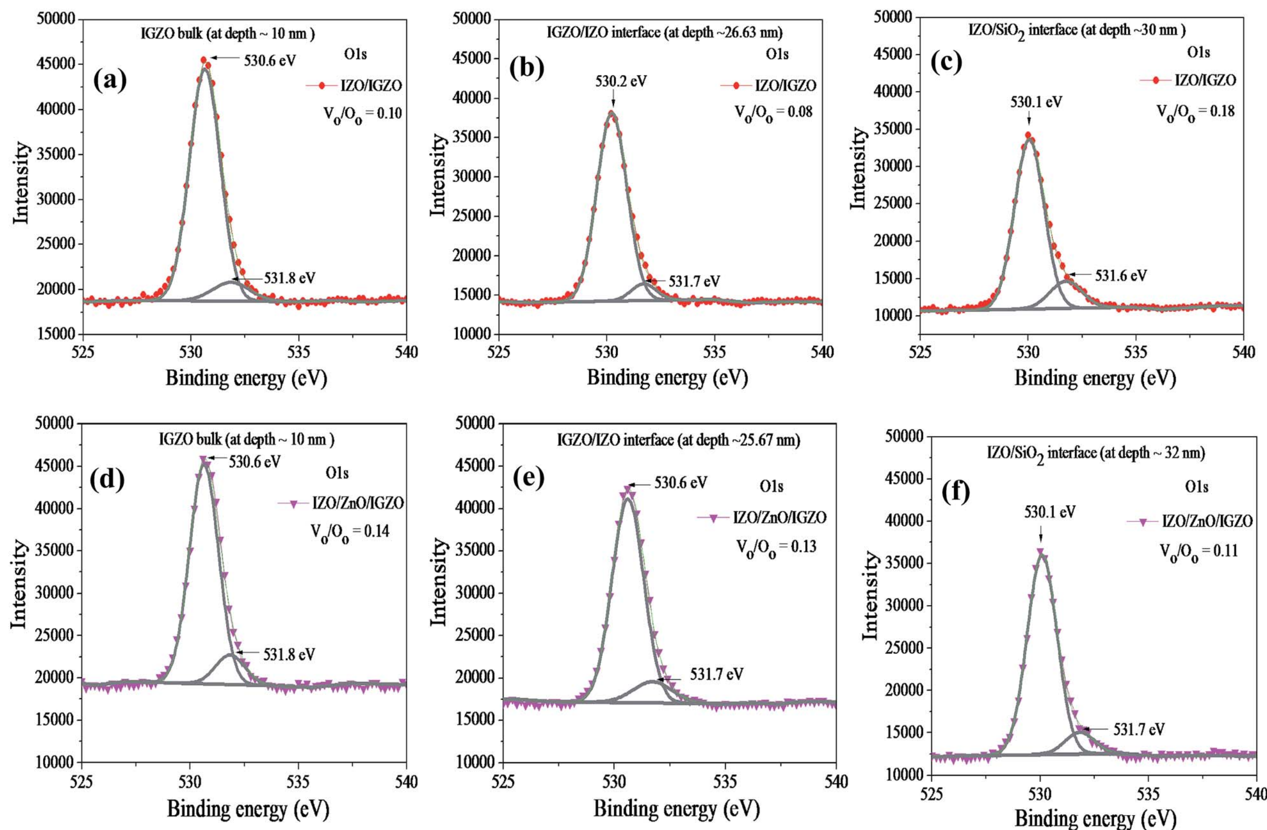

Fig. 5 O 1s XP spectra of the position (a–c) at a depth of 10, 26.63, and 30 nm for IZO/IGZO/SiO_2 stack, and (d–f) at a depth of 10, 25.67, and 32 nm for IZO/ZnO/IGZO/SiO_2 stack, which correspond to the bulk IGZO region, near-interfacial IGZO/IZO region, and interfacial IZO/SiO_2 region, respectively. The O 1s spectra were de-convoluted into two different peaks, the lattice oxygen peak without oxygen vacancies (530.5 ± 0.1 and), the lattice oxygen peak in the oxygen deficient region (531.2 ± 0.6 eV).

of V_O/O_O in IGZO/IZO/SiO_2 stack was found to be 0.10, 0.08, and 0.18 for IGZO bulk (at depth ~ 10 nm), IGZO/IZO interface (at depth ~ 26.63 nm), and IZO/SiO_2 interface (at depth ~ 30 nm), respectively. The value of V_O/O_O in IGZO/ZnO/IZO/SiO_2 stack was found to be 0.14, 0.13, and 0.11 for IGZO bulk (at depth ~ 10 nm), IGZO/IZO interface (at depth ~ 25.67 nm), and IZO/SiO_2 interface (at depth ~ 32 nm), respectively. Clearly, the IZO front channel of IGZO/ZnO/IZO/SiO_2 stack yields lower oxygen vacancies (V_O/O_O ~ 0.11) than the channel of the IGZO/IZO/SiO_2 stack (V_O/O_O ~ 0.18). The role of the ZnO interlayer on the modification of intrinsic defects, especially the divalent zinc and oxygen vacancies in the active front channel, can actively influence the performance and stability of thin film transistors. Therefore, an attempt is made here to fabricate single IZO, IGZO, IZO/IGZO, and IZO/ZnO/IGZO TFTs for a complete understanding of the impact of ZnO incorporation on device performance and negative bias illumination stress (NBIS) stability. The transfer ($I_{DS} - V_{GS}$) characteristics of the TFTs are shown in Fig. 6. The linear field effect mobility (μ_{FE}) was determined by the maximum *trans*-conductance, [$g_m = (\partial I_{DS}/\partial V_{GS}) = \mu_{FE}C_{ox}(W/L)V_{DS}$; where C_{ox} is gate dielectric (SiO_2) capacitance per unit area ~3.45×10^{-8} F cm^{-2}, I_{DS} is the drain current, V_{GS} is the gate-source voltage, V_{DS} is the drain–source voltage] at a drain voltage (V_{DS}) of 0.1 V (Fig. 6a), and the threshold voltage (V_{th}) was extracted from the *x*-axis intercept of the ($\sqrt{I_{DS}} - V_{GS}$) curve measured at a drain voltage of 10 V (Fig. 6b). The subthreshold gate swing (SS ~ $dV_{GS}/d\log_{10} I_{DS}$) was extracted from the linear portion of a plot of the log I_{DS} *versus* V_{GS} (Fig. 6c).[20] The extracted performance parameters of the TFTs are given in Table 1. The V_{th}, SS and μ_{FE} values for the IGZO TFT were 8.10 V, 0.47 V per decade, 11.5 cm^2 V^{-1} s^{-1}, respectively. The V_{th}, SS and μ_{FE} values for the IZO TFT were −12.50 V, 0.56 V per decade, 36 cm^2 V^{-1} s^{-1}, respectively. The high channel mobility and large negative threshold voltage in IZO TFT are ascribed to large carrier density within the channel.[21] However, the large SS value is attributed to increase in total charge trap density (N_t) including the bulk trap density (N_b) of the IZO itself and interface trap density (N_{it}) at or near the interface between IZO and SiO_2.[20] To confirm the fact whether the SS value in our devices is more dependent on N_{it} or N_b, a bilayer TFT of IZO/IGZO is fabricated. The SS value for the bilayer TFTs (SS ~ 0.34 V per decade) is decreased substantially compared to the single layer IZO (SS ~ 0.56 V per decade) and IGZO (SS ~ 0.47 V per decade) TFTs. This indicates that the SS value is mainly dependent on N_b rather than the N_{it}. The bilayer IZO/IGZO thin film exhibits a lower value of bulk trap density *viz.* zinc vacancies and oxygen vacancies than the IZO and IGZO film, as confirmed from the PL (Fig. 3) and XPS (Fig. 4 and 5)

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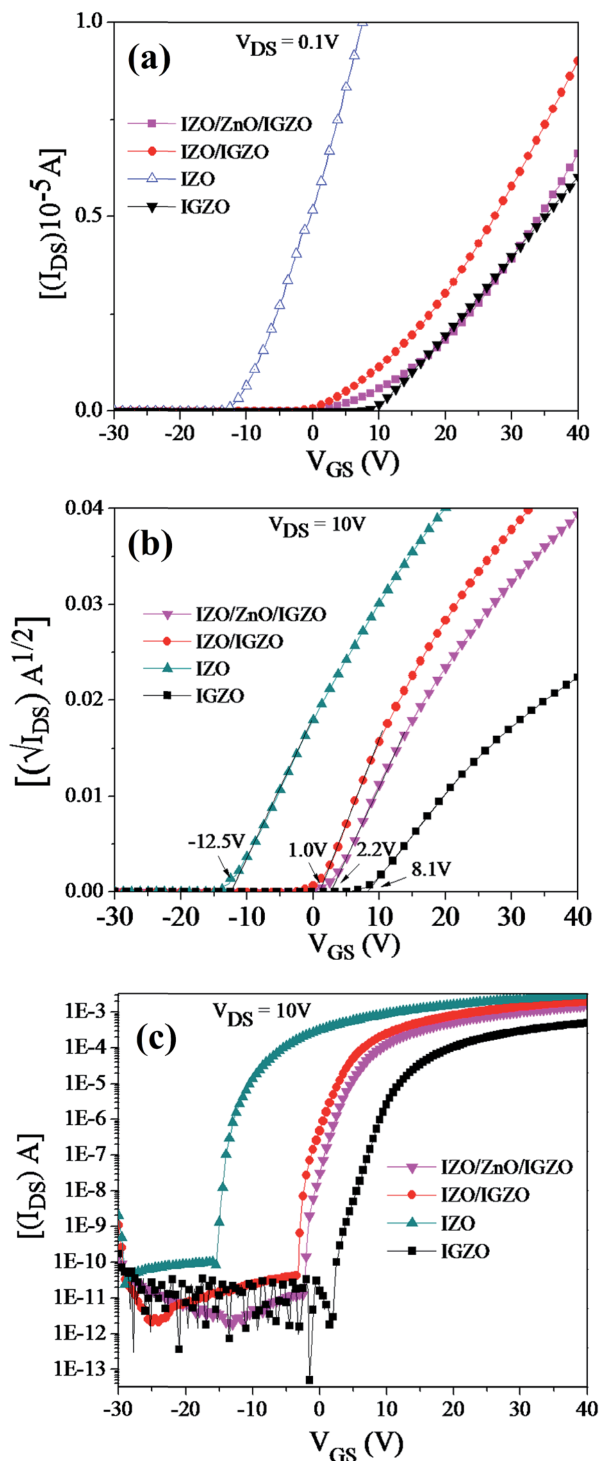

Fig. 6 Transfer characteristics of IZO (5 nm), IGZO (25 nm), IZO (5 nm)/IGZO (25 nm), and IZO (5 nm)/ZnO (2 nm)/IGZO (25 nm) active layer based TFTs: (a) I_{DS} *versus* V_{GS} plot at $V_{DS} = 0.1$ V, (b) $\sqrt{I_{DS}}$ *versus* V_{GS} plot at $V_{DS} = 10$ V, and (c) semi-log plot of I_{DS} *versus* V_{GS} at $V_{DS} = 10$ V for deduction of mobility, threshold voltage, and sub-threshold swing, respectively.

analysis, leading to a smaller gate swing for the bilayer TFT. The SS is an important parameter in switching TFT backplanes for display, because it determines the minimum V_{GS} required to turn a TFT from the off state to the on state. Therefore, the SS value is much more improved while inserting the ZnO thin layer in the bilayer structure of IZO/IGZO; the value being 0.27 V per decade in IZO/ZnO/IGZO stack TFT. The ZnO diffused within the IZO front channel layer to suppress the zinc and oxygen vacancies (Fig. 3 and 4), enabling a superior SS value (Table 1). On the other hand, to analyze the impact of the ZnO layer on device stability (*i.e.*, threshold voltage shift, ΔV_{th}), negative biased illumination stress (NBIS) tests were conducted, under an illumination wavelength of 365 nm in the dark with gating at −20 V and source as well as drain electrodes at zero bias in order to keep a uniform potential through the channel layer of TFTs. The transfer characteristics of the devices before and after illumination for 0 and 2500 s are shown in Fig. 7. Under NBIS conditions, V_{th} of the IZO, IGZO and IZO/IGZO TFTs exhibits a more negative V_{th} shift of −8.25, −4.68 V, −3.14 V, respectively, after 2500 s stressing. This can be understood by (1) the presence of high density of oxygen vacancies (V_O^+) that act as a negative U defect center; the (V_O^+) defect transits to a meta-stable (V_O^{2+}) excited state releasing one free electron in the conduction band upon light illumination,[22] and (2) the presence of a high density of divalent zinc vacancies (V_{Zn}^{2-}); the (V_{Zn}^{2-}) transits to a neutral charge state (V_{Zn}^0) releasing two free electrons in the conduction band upon light illumination ($V_{Zn}^{2-} + h\nu \rightarrow V_{zn}^0 + 2e$) and leading to a more negative V_{th} shift. With insertion of the ZnO layer in a bilayer of IZO/IGZO, the defects *viz.*, divalent zinc and oxygen vacancies were reduced (Fig. 3 and 4) due to the high diffusion ability of ZnO within the front IZO channel (Fig. 2 and 4)—resulting in a less negative V_{th} shift ($\Delta V_{th} \sim -2.45$ V) under NBIS conditions. Interestingly, the IZO/ZnO/IGZO TFT exhibits far better electrical characteristics and stability than the a-IGZO TFTs under annealing in N_2 ambient (Table 1) and can be considered as a potential candidate to be utilized in TFT backplanes for displays. The modification of the interfaces and IZO channels by various treatments such as plasma and vapors may lead to improvement of the mobility without sacrificing NBIS stability.

4. Conclusions

In summary, we have developed a noble device structure of IZO/ZnO/IGZO to result in high electrical performance and a good reliability including a linear field effect mobility of 14 cm^2 V^{-1} s^{-1}, $I_{on}/I_{off} \sim 1.2 \times 10^8$, a threshold voltage of 2.20 V, and a subthreshold swing voltage of 0.27 V per decade. Besides, the TFT displayed superior NBIS stability ($\Delta V_{th} \sim -2.45$ V) to that of the bilayer ($\Delta V_{th} \sim -3.14$ V) and its single IZO ($\Delta V_{th} \sim -8.25$ V) or single IGZO TFTs ($\Delta V_{th} \sim -4.68$ V). These excellent properties are attributed to the ZnO interlayer which suppressed the pre-existing defects (*viz.*, V_{Zn}^{2-}, V_O^+) within the front IZO channel. Therefore, the ZnO interlayer (~2 nm) is essential for designing a double-channel device that exhibits improved performance and bias stability compared to the single-channel device. Overall, the ZnO interlayer of 2 nm within the double-channel IZO/IGZO TFTs can be used as backplane electronics for high-resolution and large-sized AMOLED and TFT-LCD displays.

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Table 1 Electrical parameters of TFTs fabricated with IZO, IGZO, IZO/IGZO and IZO/ZnO/IGZO active channels

TFT with active layer	μ_{FE}/cm^2 V^{-1} s^{-1}	SS/V dec^{-1}	V_{th}/V	ΔV_{th}/V
IGZO (25 nm)	11.5	0.47	8.10	−4.68
IZO (5)/IGZO (25 nm)	15.4	0.34	1.00	−3.14
IZO (5)/ZnO (2)/IGZO (25 nm)	14.0	0.27	2.20	−2.45
IZO (5 nm)	36.0	0.56	−12.50	−8.25

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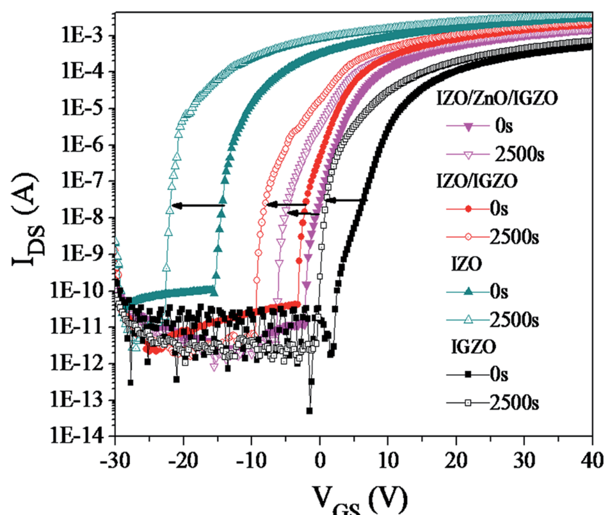

Fig. 7 Transfer characteristics of TFTs fabricated with IZO (5 nm), IGZO (25 nm), IZO (5 nm)/IGZO (25 nm), and IZO (5 nm)/ZnO (2 nm)/IGZO (25 nm) as the active channel layer after stressing at $V_{GS} = -20$ V with an illumination wavelength of 365 nm for different time intervals (zero − 2500 s).

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Notes and references

1 T.-Y. Hsieh, T.-C. Chang, T.-C. Chen and M.-Y. Tsai, *ECS J. Solid State Sci. Technol.*, 2014, **3**, Q3058–Q3070.

2 J. H. Kim, U. K. Kim, Y. J. Chung and C. S. Hwang, *Phys. Status Solidi RRL*, 2011, **5**, 178–180.

3 J. K. Jeong, H. W. Yang, J. H. Jeong, Y.-G. Mo and H. D. Kim, *Appl. Phys. Lett.*, 2008, **93**, 123508.

4 B. S. Yang, M. S. Huh, S. Oh, U. S. Lee, Y. J. Kim, M. S. Oh, J. K. Jeong, C. S. Hwang and H. J. Kim, *Appl. Phys. Lett.*, 2011, **98**, 122110.

5 J.-Y. Kwon, J. S. Jung, K. S. Son, K.-H. Lee, J. S. Park, T. S. Kim, J.-S. Park, R. Choi, J. K. Jeong, B. Koo and S. Lee, *J. Electrochem. Soc.*, 2011, **158**, H433–H437.

6 H. Y. Jung, Y. Kang, A. Y. Hwang, C. K. Lee, S. Han, D.-H. Kim, J.-U. Bae, W.-S. Shin and J. K. Jeong, *Sci. Rep.*, 2014, **4**, 3765.

7 H.-S. Kim, J. S. Park, H.-K. Jeong, K. S. Son, T. S. Kim, J.-B. Seon, E. Lee, J. G. Chung, D. H. Kim, M. Ryu and S. Y. Lee, *ACS Appl. Mater. Interfaces*, 2012, **4**, 5416–5421.

8 E. Chong, Y. W. Jeon, Y. S. Chun, D. H. Kim and S. Y. Lee, *Thin Solid Films*, 2011, **519**, 4347–4350.

9 X. Ding, H. Zhang, H. Ding, J. Zhang, C. Huang, W. Shi, J. Li, X. Jiang and Z. Zhang, *Superlattices Microstruct.*, 2014, **76**, 156–162.

10 J. C. Park, S. Kim, S. Kim, C. Kim, I. Song, Y. Park, U.-I. Jung, D. H. Kim and J.-S. Lee, *Adv. Mater.*, 2010, **22**, 5512–5516.

11 G. X. Liu, A. Liu, F. K. Shan, Y. Meng, B. C. Shin, E. Fortunato and R. Martins, *Appl. Phys. Lett.*, 2014, **105**, 113509.

12 S. S. Yen, Y.-C. Chiu, C.-H. Cheng, P. C. Chen, Y.-C. Yeh, C.-H. Tung, H.-H. Hsu and C.-Y. Chang, *J. Disp. Technol.*, 2016, **12**, 219–223.

13 A. Janotti and C. G. V. d. Walle, *Rep. Prog. Phys.*, 2009, **72**, 126501.

14 N. Tiwari, R. N. Chauhan, H.-P. D. Shieh, P.-T. Liu and Y.-P. Huang, *IEEE Trans. Electron Devices*, 2016, **63**, 1578–1581.

15 A. K. Srivastava and J. Kumar, *Sci. Technol. Adv. Mater.*, 2013, **14**, 065002.

16 A. Janotti and C. G. V. d. Walle, *Phys. Rev. B: Condens. Matter Mater. Phys.*, 2007, **76**, 165202.

17 B. Lin, Z. Fu and Y. Jia, *Appl. Phys. Lett.*, 2001, **79**, 943–945.

18 S. A. M. Lima, F. A. Sigoli, M. Jafelicci Jr and M. R. Davolos, *Int. J. Inorg. Mater.*, 2001, **3**, 749–754.

19 Y. Jeong, C. Bae, D. Kim, K. Song, K. Woo, H. Shin, G. Cao and J. Moon, *ACS Appl. Mater. Interfaces*, 2010, **2**, 611–615.

20 T. Kamiya, K. Nomura and H. Hosono, *Sci. Technol. Adv. Mater.*, 2010, **11**, 044305.

21 B. Yaglioglu, H. Y. Yeom, R. Beresford and D. C. Paine, *Appl. Phys. Lett.*, 2006, **89**, 062103.

22 S. Kim, S. Kim, C. Kim, J. C. Park, I. Song, S. Jeon, S.-E. Ahn, J.-S. Park and J. K. Jeong, *Solid-State Electron.*, 2011, **62**, 77–81.

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