Physical Mechanism and Device Simulation on Transient-Induced Latchup in CMOS ICs Under System-Level ESD Test

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***Abstract*—The physical mechanism of transient-induced latchup (TLU) in CMOS ICs under the system-level electrostatic discharge (ESD) test is clearly characterized by device simulation and experimental verification in time domain. For TLU characterization, an underdamped sinusoidal voltage stimulus has been clarified as the realistic TLU-triggering stimulus under the system-level ESD test. The specific "sweep-back" current caused by the minority carriers stored within the parasitic pnpn structure of CMOS ICs has been qualitatively proved to be the major cause of TLU. All the simulation results on TLU have been practically verified in silicon with test chips fabricated by 0.25-μm CMOS technology.**

***Index Terms*—Holding voltage, latchup, silicon controlled rectifier (SCR), system-level electrostatic discharge (ESD) test, transient-induced latchup (TLU).**

I. Introduction

TRANSIENT-INDUCED LATCHUP (TLU) will increasingly be a primary reliability issue in CMOS IC products [1]–[5]. Recently, the test standard to verify the immunity of TLU on CMOS ICs has been announced [6]. This TLU tendency is caused by several reasons. First, there are much more complicated implementations of ICs, such as mixed-signal, multiple power supplies, RF, system-on-chip, etc. The environment where these CMOS devices locate will suffer from considerable noises coming from both interior and exterior of CMOS ICs. Thus, such transient stimuli, those unpredictably exist on power, ground, or I/O pins of ICs, certainly induce TLU much more easily than before. Second, more and more ICs, unfortunately, are rather susceptible to TLU under a strict demanded system-level electrostatic discharge (ESD) test [7]. Third, aggressive scaling of both device feature size, as well as the clearance between pMOS and nMOS devices, leads the inevitable parasitic silicon controlled rectifier (SCR) in CMOS ICs to exhibit a rather worse latchup immunity. The occurrence of latchup could still happen, even though the power supply voltage is reduced with the scaling rule of CMOS ICs. The latchup triggering current does not prominently increase with the scaling rule of CMOS ICs while the power supply voltage keeps decreasing [8].

To investigate the physical mechanism of TLU under the system-level ESD test, the most significant part is to clarify the TLU-triggering stimulus at first. So far, several TLU-triggering stimuli have been found to probably trigger on TLU [9]–[11]. The first developed TLU-triggering stimulus is to consider the power-on situation when power supply voltage ramps up from 0 V to its normal operating voltage during the power-on transition [9]. Once the rise time (ramp rate) of the power supply voltage during the power-on transition is short (fast) enough, latchup will probably be triggered on by the transient displacement current that flows through the parasitic well/substrate resistance of CMOS ICs. However, this situation only interpreted the occurrence of TLU during the initial power-on transition, but cannot reflect most TLU during the normal circuit operation. The second developed TLU-triggering stimulus is to utilize a single-positive (single-negative) voltage pulse applying on the pMOS (NMOS) drain terminal of CMOS ICs [10]. Such single-positive (single-negative) voltage pulse is used to generate the transient overshooting (undershooting) noise on the output nodes of CMOS logic gates to simulate the dynamically switching operations. Thus, TLU could be triggered on due to the instantaneous forward-biased emitter/base junction current of the parasitic pnp (or npn) bipolar junction transistor (BJT). However, TLU issue still exists even if CMOS ICs are operated in a dc steady state without dynamically switching under the system-level ESD test. Recently, a single-positive current pulse [11] applying to the power pins of CMOS ICs is also used for TLU characterization. This TLU-triggering stimulus, however, does not reflect the real one under the system-level ESD test.

To clarify this issue, an underdamped sinusoidal voltage stimulus, which can be observed on all ICs within the equipment under test (EUT) under the system-level ESD test [12]–[14], is adopted in this paper as the TLU-triggering stimulus for both TLU measurement and device simulation [15]. With the clearly defined TLU-triggering stimulus, the physical mechanism of TLU under the system-level ESD test can be well explained in time domain by device simulation. Finally, all the simulation results on TLU have been practically verified in silicon with test chips fabricated by 0.25-μm CMOS technology.

II. TLU Under System-Level ESD Test

To evaluate the performance of electrical/electronic equipments when subjected to ESD events, performing the system-level ESD test for the electrical/electronic equipments is necessary. For example, a notebook under the system-level ESD test with direct contact-discharge test mode is shown in Fig. 1. An electrical/electronic product with CMOS ICs must

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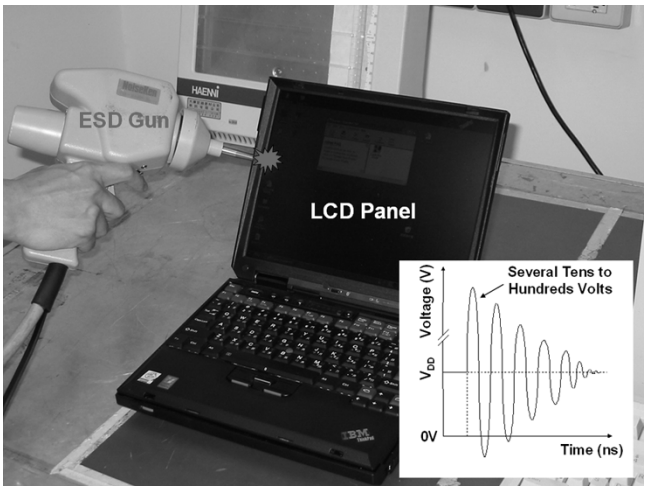

Fig. 1. System-level ESD test on a notebook with direct contact-discharge mode according to IEC 61 000-4-2 international standard [7]. The inset figure depicts the typically measured waveforms of transient noise voltage on the power pins of CMOS ICs, which locate within the EUT, under the system-level ESD test [12]–[14].

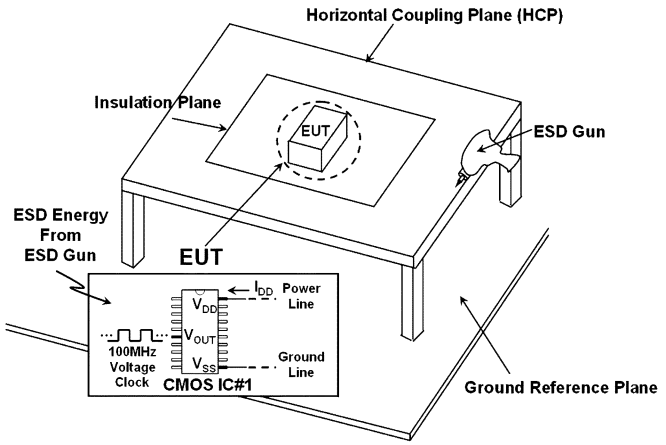

Fig. 2. Measurement setup of the system-level ESD test with indirect contact-discharge test mode [7]. CMOS IC#1 is one of the CMOS ICs inside the EUT. The ESD gun zapping on the HCP could cause TLU events on the ICs, especially those inside the EUT.

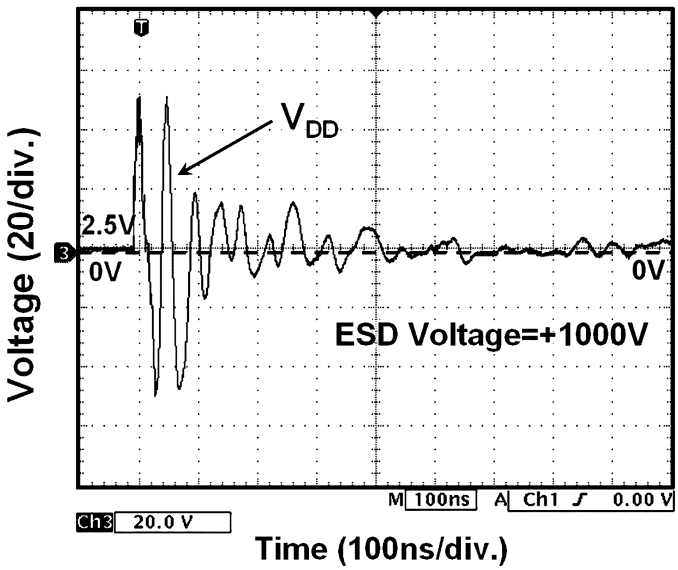

Fig. 3. Measured $V_{\rm DD}$ transient waveform on one of the CMOS ICs (CMOS IC#1) inside the EUT, when the ESD gun with ESD voltage of $+1000$ V zapping on the HCP.

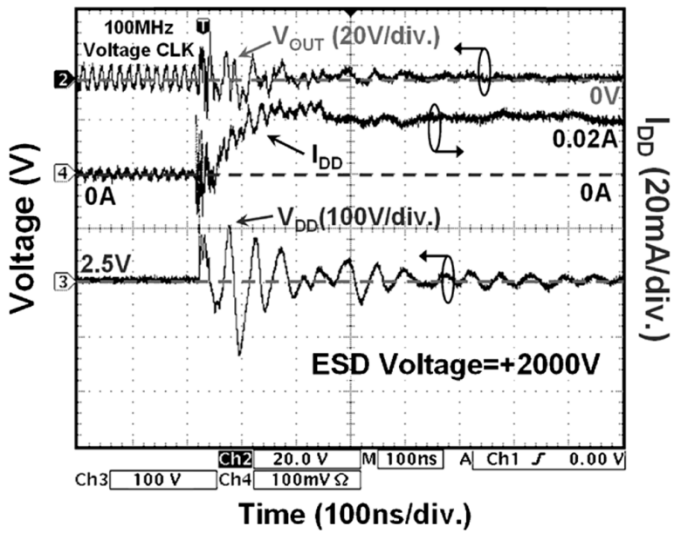

Fig. 4. Measured $V_{\rm DD}$, $I_{\rm DD}$, and $V_{\rm OUT}$ transient waveforms on CMOS IC#1 inside the EUT, when the ESD gun with ESD voltage of $+2000$ V zapping on the HCP, to verify the occurrence of TLU during system-level ESD test.

sustain the ESD level of ± 8 kV (± 15 kV) under contact-discharge (air-discharge) test mode to achieve the immunity requirement of "level 4" in the system-level ESD test [7]. During such a system-level ESD test, electromagnetic interference (EMI) coming from the ESD will be coupled into the driver ICs of the liquid crystal display (LCD) panel. The inset figure in Fig. 1 depicts the typically measured ESD-generated voltage waveforms on the power pins of CMOS ICs, which locate within the equipment under test (EUT), under the system-level ESD test [12]–[14]. This ESD-generated transient voltage is quite large (with an amplitude of several tens to hundreds of volts) and fast (with period of several tens of nanoseconds), which can randomly exist on power, ground, or I/O pins of the driver ICs to cause TLU failures.

To clarify this issue, the system-level ESD test with indirect contact-discharge test mode is shown in Fig. 2, [7]. When the ESD gun zaps to the horizontal coupling plane (HCP), EMI coming from the ESD will be coupled into all CMOS ICs inside the EUT. With ESD voltage of $+1000$ V, the measured $V_{\rm DD}$ transient waveforms on one of the CMOS ICs (CMOS IC#1) inside the EUT are shown in Fig. 3. The transient peak voltage on $V_{\rm DD}$ is as large as ± 50 V in Fig. 4. Clearly, the $V_{\rm DD}$ with initial dc voltage of $+2.5$ V will become an underdamped sinewave-like voltage due to the disturbance of the ESD energy. Once the ESD voltage keeps increasing, the TLU can be initiated and results in the malfunction or damage of the CMOS IC inside the EUT. For example, with an ESD voltage of $+2000$ V, the measured $V_{\rm DD}$, $I_{\rm DD}$, and $V_{\rm OUT}$ transient waveforms on CMOS IC#1 are shown in Fig. 4. The transient peak voltage on $V_{\rm DD}$ is greater than ± 100 V, during such a system-level ESD test. TLU occurs with instantaneously increasing $I_{\rm DD}$, so that $V_{\rm OUT}$ (100-MHz voltage clock) will fail to function correctly (pulled

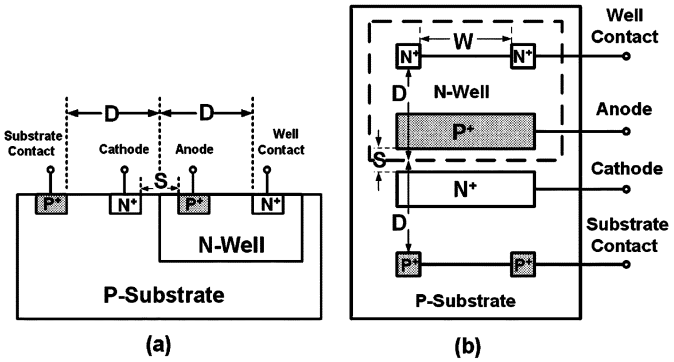

Fig. 5. (a) Device cross-sectional view and (b) layout top view of the SCR structure for TLU measurements. Geometrical parameters such as D, S, and W represent the distances between well-edge and well (substrate) contact, anode and cathode, and the adjacent well (substrate) contacts, respectively. The specified SCR structure, fabricated by 0.25-μm CMOS technology, with layout parameters of $D = 6.7$, $S = 1.2$, and $W = 22.5$ μm is used for all the TLU measurements in this paper.

down to 0 V). Thus, it can be clarified that the underdamped sinusoidal voltage existing on the power (ground) line of the CMOS ICs is the major cause to initiate TLU during the system-level ESD test.

III. Test Structure

The SCR structure is used as the test structure for TLU measurements because the occurrence of latchup is due to the inherent SCR of two cross-coupled BJTs, parasitic vertical pnp and lateral npn BJTs, in bulk CMOS ICs [8]. The device cross-sectional view and layout top view of the SCR structure are sketched in Fig. 5(a) and (b), respectively. The geometrical parameters such as D, S, and W represent the distances between well-edge and well (substrate) contact, anode and cathode, and the adjacent well (substrate) contacts, respectively. In CMOS ICs, the p^+ anode (source of PMOS) and the n^+ well contact are connected to V_{DD}, whereas the n^+ cathode (source of NMOS) and the p^+ substrate contact are connected to ground. Once latchup occurs inside the SCR structure, huge current will be generated through a mechanism of positive-feedback regeneration [16]. As a result, the huge current will conduct through a low-impedance path from V_{DD} to ground, and further probably burn out the chip due to excess heat.

Different values of geometrical parameters such as D, S, and W in Fig. 5(a) and (b) will certainly result in different TLU immunities of the SCR structures due to different latchup triggering (holding) voltages or currents [8]. However, TLU physical mechanism should be the same and not related to the variations of geometrical parameters. As a result, to qualitatively analyze the physical mechanism of TLU through TLU measurements, a specified SCR structure with layout parameters of $D = 6.7$, $S = 1.2$, and $W = 22.5$ μm fabricated in 0.25-μm CMOS technology is used for all TLU measurements in this paper. Because the parasitic SCR existing in the core circuitry of CMOS ICs is most sensitive to TLU due to compact integration, the minimum anode-to-cathode spacing ($S = 1.2$ μm) according to foundry's design rule is used to consider the worst case situation (most sensitive to TLU) encountered in the core circuitry of CMOS ICs.

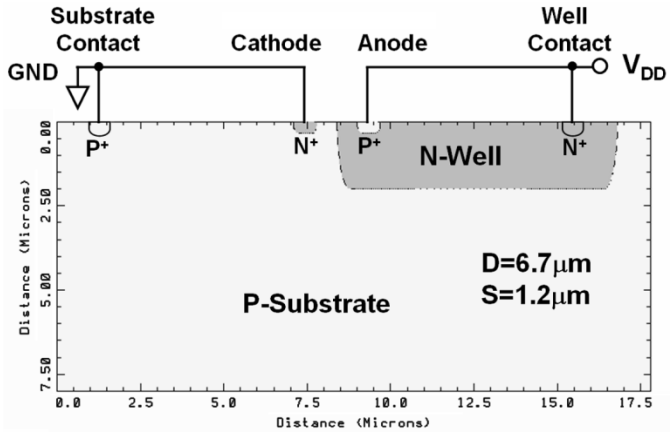

Fig. 6. SCR structure used in a 2-D device simulation tool (MEDICI). The specified SCR structure with the geometrical parameters of $D = 6.7$ μm and $S = 1.2$ μm is used for all the TLU device simulations in this paper.

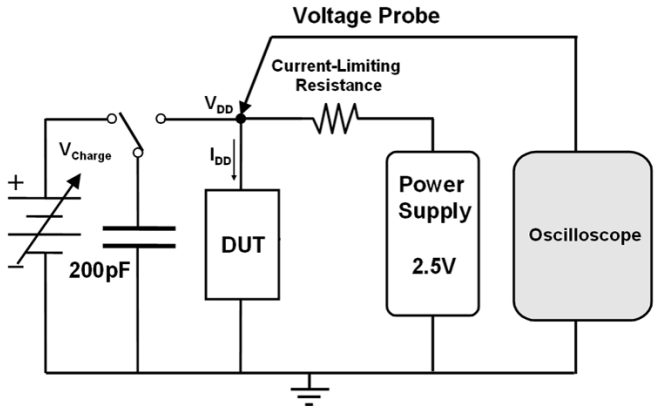

Fig. 7. Component-level TLU measurement setup [3]. It can accurately simulate how an IC inside the EUT will be disturbed by the ESD-generated noise under the system-level ESD test.

To verify the relationship between the TLU measurement and device simulation, the specified SCR structure with the same geometrical parameters of $D = 6.7$ and $S = 1.2$ μm is used for all TLU device simulations in this paper by the two-dimensional (2-D) device simulation tool (MEDICI), as shown in Fig. 6. With the specified 2-D SCR structure, the boundary condition can be well defined to perform the numerical analysis of electrical characteristics such as electric potential, electric field, carrier concentration, 2-D current flow line, etc.

IV. Measurement Setup

For the system-level ESD test, it can only judge whether the EUT passes the required criterion through its abnormal function (e.g., EUT shuts down). Nevertheless, it is hard to directly evaluate the TLU immunity of single IC inside the EUT. To solve this problem, a component-level TLU measurement setup with the following two advantages is used. First, it can easily evaluate the TLU immunity of single IC by the related measured voltage/current waveforms through oscilloscope. Second, with the ability of generating an underdamped sinusoidal voltage, it can accurately simulate how an IC inside the EUT will be disturbed by the ESD-generated noise under the system-level ESD test. Fig. 7 depicts such a component-level TLU measurement

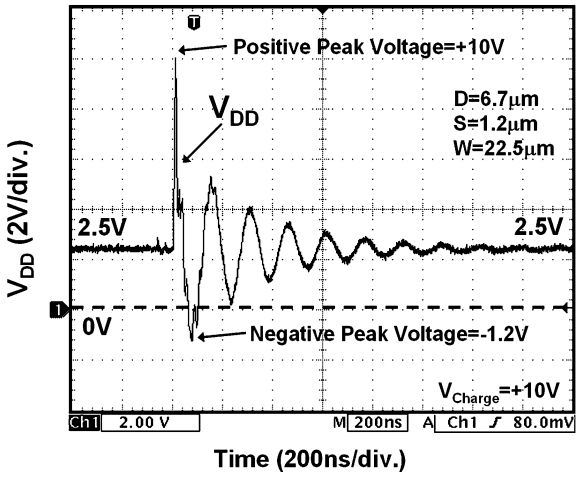

Fig. 8. Measured $V_{\rm DD}$ waveform for the SCR structure with $V_{\rm Charge}$ of (a) $+10$ V, and (b) -2 V. Clearly, the intended positive-going (negative-going) underdamped sinusoidal voltage can be generated just as that under the system-level ESD test for ESD gun with positive (negative) voltage [12].

setup [3]. The SCR structure shown in Fig. 5 is used as the device under test (DUT) where the p^+ anode and the n^+ well contact are connected together to $V_{\rm DD}$, but the n^+ cathode and the p^+ substrate contact are connected to ground. An electrostatic-discharge simulator is used as the TLU-triggering source, $V_{\rm Charge}$, to produce an underdamped sinusoidal voltage stimulus. Through applying a positive (negative) $V_{\rm Charge}$, the intended positive-going (negative-going) underdamped sinusoidal voltage can be generated just as that under the system-level ESD test for ESD gun with positive (negative) voltage [12]. For example, with $V_{\rm Charge}$ of $+10$ V (-2 V), Fig. 8(a) and (b) shows the measured $V_{\rm DD}$ waveform across the SCR structure. Clearly, the intended underdamped sinusoidal voltage can be produced to simulate the transient voltage on power pins of CMOS ICs under the system-level ESD test, no matter which polarity (positive or negative) the ESD voltage is. Because a large discharge resistance will result in a large damping factor of the intended underdamped sinusoidal voltage [3], there is no discharge resistance (0 Ω) between the relay and the $V_{\rm DD}$ node, as shown in Fig. 7. As a result, the intended underdamped sinusoidal voltage can be produced, but not the unwanted overdamped voltage waveform due to a large discharge resistance [3]. In addition, a charged capacitance of 200 pF is used to store charges offered by the TLU-triggering source, $V_{\rm Charge}$, and then these stored charges are discharged to DUT through the relay. Because the charged capacitance will affect the damping frequency of the underdamped sinusoidal voltage, it should be properly selected to achieve the reasonable damping frequency as that under the system-level ESD test. For example, the damping frequency ($\sim$10 MHz) observed in Fig. 8(a) and (b) is slightly smaller than that under the system-level ESD test ($\sim$20 MHz) [12], therefore indicating that this measurement setup is reasonable for TLU characterization. Moreover, a small current-limiting resistance (5 Ω) is recommended to protect the DUT from electrical-over-stress (EOS) damage during a high-current (low-impedance) latchup state.

V. Device Simulation for TLU

A 2-D device simulation tool (MEDICI) is used to investigate the physical mechanism of TLU in time domain under the system-level ESD test. In this 2-D device simulation tool, a specific time-dependent voltage source given by

$$V(t) = V_0 + V_a \cdot \exp(-(t - t_d)D_a) \cdot \sin(2\pi f(t - t_d)) \quad (1)$$

is used to apply an underdamped sinusoidal voltage on $V_{\rm DD}$ of the already defined SCR structure in Fig. 6. With the proper parameters such as initial voltage V_0, applied voltage amplitude V_a, damping factor D_a, damping frequency f, and time delay t_d, the intended underdamped sinusoidal voltage can be constructed. In the following TLU simulation with positive or negative $V_{\rm Charge}$, the same parameters such as $V_0 = 2.5$ V, $D_a = 2 \times 10^7$ s^{-1}, $f = 20$ MHz, and $t_d = 50$ ns are used in both positive and negative $V_{\rm Charge}$, whereas the only difference is $V_a = +14.6$ V for positive $V_{\rm Charge}$, but -14.6 V for negative $V_{\rm Charge}$. In addition, the specified SCR structure with geometrical parameters of $D = 6.7\ \mu$m and $S = 1.2\ \mu$m is used for all TLU device simulations in this paper.

A. Simulated Latchup DC I–V Characteristics

The simulated latchup dc current–voltage (I–V) characteristic of the specified SCR structure is shown in Fig. 9. Once latchup occurs in the SCR structure, a low-impedance path will exist from $V_{\rm DD}$ to ground, resulting in huge current conducting through this low-impedance path. The inset figure in Fig. 9 shows that the dc latchup triggering voltage (current), $V_{\rm Trig}$ ($I_{\rm Trig}$), is about 15.5 V (0.24 mA), while the dc latchup holding voltage (current), $V_{\rm Hold}$ ($I_{\rm Hold}$), is about 1.25 V (0.5 mA). Clearly, under a latchup state, when the power supply voltage, $V_{\rm DD}$, keeps at its normal circuit operating voltage ($+2.5$ V), the total power supply current, $I_{\rm DD}$, flowing into both anode and well contact is about 150 mA. This will offer a vital evidence to verify whether TLU certainly occurs in time domain through device simulation.

B. TLU Simulation With Negative $V_{\rm Charge}$

With a negative $V_{\rm Charge}$, the simulated $V_{\rm DD}$ and $I_{\rm DD}$ transient responses on the SCR structure are shown in Fig. 10. This can be divided into several parts for detailed discussions

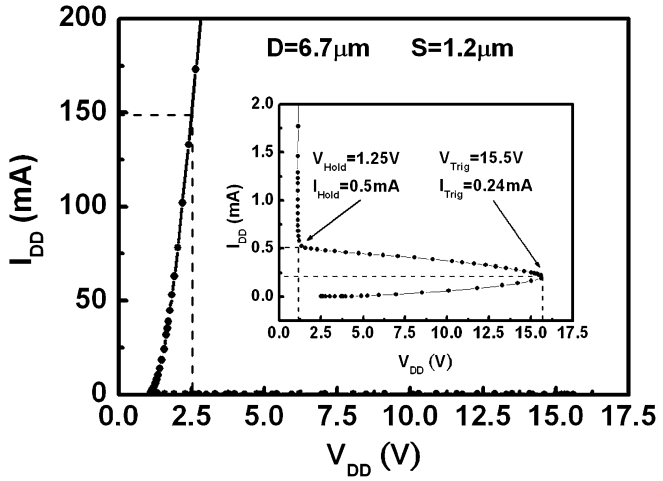

Fig. 9. Simulated latchup dc I–V characteristic for the SCR structure. Under a latchup state, the fact that $I_{\rm DD}$ is about 150 mA when $V_{\rm DD}$ keeps at its normal operating voltage ($+2.5$ V) will offer a vital evidence to prove whether TLU certainly occurs in time domain through device simulation.

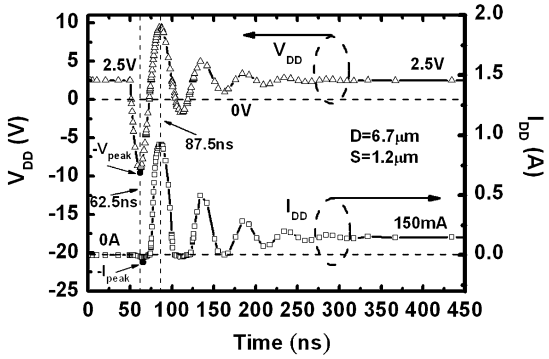

Fig. 10. Simulated $V_{\rm DD}$ and $I_{\rm DD}$ transient responses for TLU with a negative $V_{\rm Charge}$. During the period of 62.5 ns $\leq t \leq 87.5$ ns, the "sweep-back" current, $I_{\rm Sb}$, will be produced to initiate TLU ($I_{\rm DD}$ significantly increases) when $V_{\rm DD}$ increases from its negative peak voltage to the normal operating voltage of $+2.5$ V.

in time domain. First, during the period of 0 ns$\leq t <$ 50 ns, the SCR operates in the blocking condition and $V_{\rm DD}$ is fixed at its normal operating voltage, $+2.5$ V. Within this duration, the n-well/p-substrate junction is at a normal reverse-biased state, and $I_{\rm DD}$ only comes from the negligible leakage current in the reverse junction. Second, during the period of 50 ns $\leq t \leq$ 62.5 ns, $V_{\rm DD}$ begins to decrease rapidly from $+2.5$ V at $t =$ 50 ns, and will eventually reach the negative peak voltage, $-V_{\rm peak}$ (-8 V), at $t = 62.5$ ns. Within this duration, the n-well/p-substrate junction gradually becomes slightly reverse biased when $V_{\rm DD}$ decreases from $+2.5$ to 0 V, and even becomes forward biased when $V_{\rm DD}$ drops below 0 V. Thus, at $t = 62.5$ ns, the largest forward-biased n-well/p-substrate junction can generate the forward peak current, $-I_{\rm peak}$ ($\sim$20 mA). Third, during the period of 62.5 ns $< t \leq$ 75 ns, when $V_{\rm DD}$ increases from $-V_{\rm peak}$ to its normal operating voltage, $+2.5$ V, the n-well/p-substrate junction will rapidly change from the forward-biased state to its original reverse-biased state. Meanwhile, inside the n-well (p-substrate) region, large number of stored minority holes (electrons) offered by the forward peak current at $t = 62.5$ ns, will be instantaneously "swept-back" to

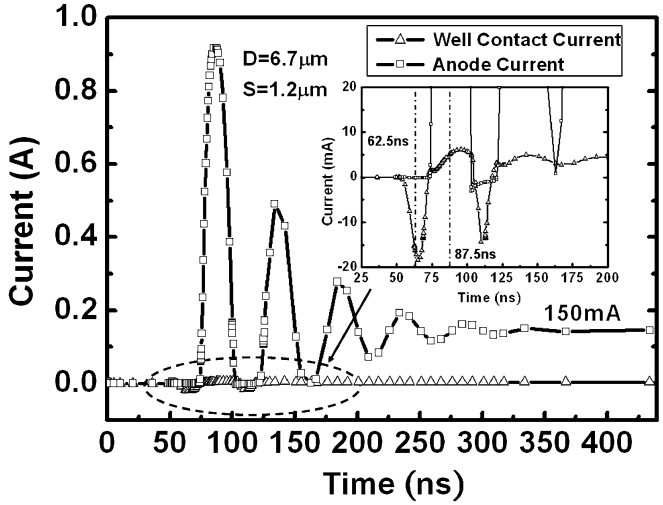

Fig. 11. Simulated transient responses of both anode current and well contact current for TLU with a negative $V_{\rm Charge}$. During the period of 62.5 ns $\leq t \leq$ 87.5 ns, latchup will be triggered on by $I_{\rm Sb}$. Meanwhile, huge anode current will conduct through the pnpn latchup path of the SCR structure.

the p-substrate (n-well) region where they originally come from. Thus, such "sweep-back" current, $I_{\rm Sb}$, will produce a localized voltage drop while flowing through the parasitic p-substrate or n-well resistance. Once this localized voltage drop approaches to some critical value, the emitter-base junction of either vertical pnp or lateral npn BJT in the SCR structure will be forward biased to further trigger on latchup. This can be further illustrated by the simulated transient responses of both anode and well contact current, as shown in Fig. 11. It clearly proves where these stored minority carriers, $Q_{\rm Stored}$, come from and when they will be "swept-back" to cause TLU. For example, the gradually-enhanced forward-biased n-well/p-substrate junction will lead the gradually-increasing well contact current during the period of 50 ns $\leq t \leq$ 62.5 ns. Meanwhile, anode current is the negligible junction-leakage current due to an almost zero bias across the p^+-anode/n-well junction. Afterwards, during the period of 62.5 ns $< t \leq$ 75 ns, the forward well contact current will gradually decrease when $V_{\rm DD}$ increases from $-V_{\rm peak}$ to $+2.5$ V, indicating that the stored minority electrons (holes) are swept-back to the n-well (p-substrate) region where they originally come from. As a result, once the $V_{\rm DD}$ returns to, and even above, $+2.5$ V (75 ns $< t \leq$ 87.5 ns), latchup will be triggered on and huge anode current will conduct through the pnpn latchup path of the SCR structure. Meanwhile, the well contact current, however, is much smaller than the anode current because the well contact current is only the small base current of the parasitic vertical pnp BJT in the SCR structure.

In real CMOS ICs, when a low-impedance latchup state appears, $V_{\rm DD}$ may be pulled down to about the dc latchup holding voltage. This phenomenon is caused by two reasons. One is a finite current-supply ability of the system power supply, and the other is the inevitable parasitic series resistance existing between the $V_{\rm DD}$ node and the system power supply. In device simulation, however, when TLU occurs during the period of 75 ns $< t \leq$ 100 ns shown in Figs. 10 and 11, $V_{\rm DD}$ was not immediately pulled down to the dc latchup holding voltage. Instead, $V_{\rm DD}$ keeps at the given underdamped sinusoidal voltage.

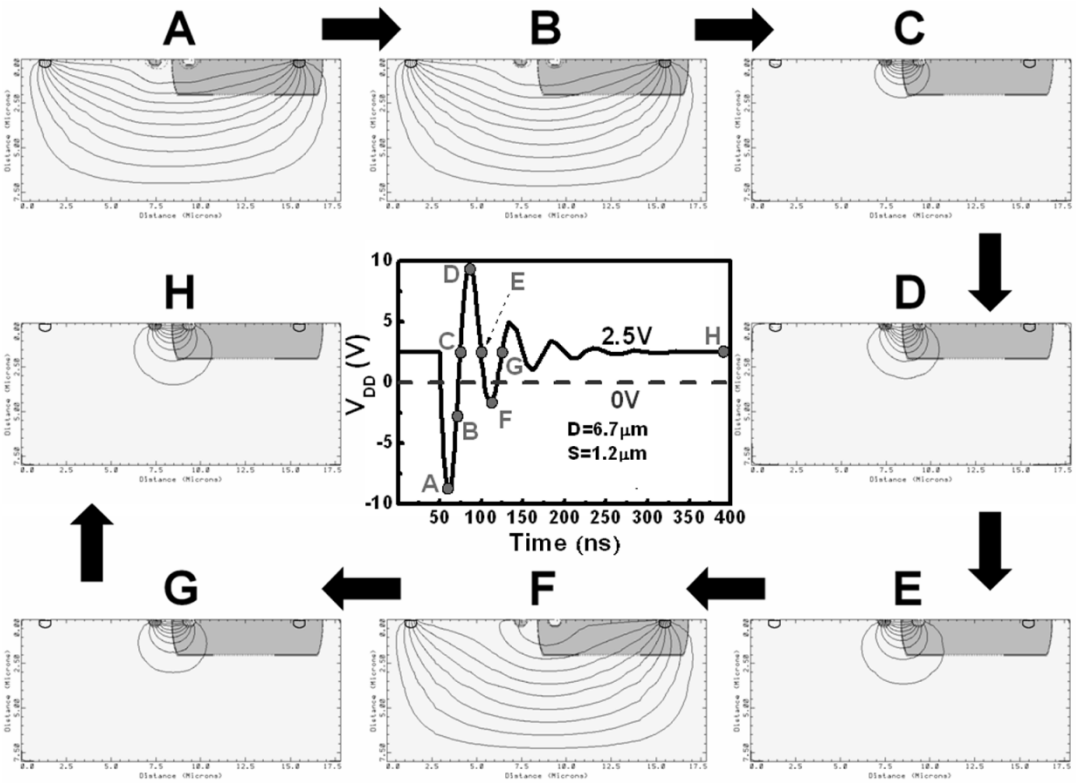

Fig. 12. Simulated 2-D current flow lines with respect to various transient timing points for TLU with a negative V_{Charge}. Forward well (substrate) contact current appears when n-well/p-substrate junction is forward-biased (timing points A, B, and F), and TLU will be triggered on due to large enough $I\mathrm{Sb}$ (timing points C-E, G, and H).

This fact results from the native limitation of device simulation tool for transient analysis in time domain. However, TLU is sure to occur because huge I_{DD} (150 mA, refer to Figs. 10, and 11) can be found when V_{DD} finally returns to its normal operating voltage, $+2.5$ V. More importantly, it is consistent with the simulated latchup dc I-V characteristics that I_{DD} is 150 mA when V_{DD} keeps at its normal operating voltage, $+2.5$ V, under a latchup state in Fig. 9.

To further judge whether TLU indeed occurs, Fig. 12 shows the corresponding simulated 2-D current flow lines with respect to various transient timing points with a negative V_{Charge}. Clearly, large forward well (substrate) contact current appears when n-well/p-substrate junction is forward-biased (timing points A, B, and F). Once the n-well/p-substrate junction quickly changes from the forward-biased state to its original reverse-biased state, TLU will be triggered on due to large enough I_{Sb} (timing points C-E, G, and H).

C. TLU Simulation With Positive V_{Charge}

With a positive V_{Charge}, Fig. 13 shows the simulated V_{DD} and I_{DD} transient responses on the SCR structure. During the period of 50 ns $\leq t \leq$ 62.5 ns, unlike the V_{DD} waveform with a negative V_{Charge} shown in Fig. 10 where V_{DD} begins decreasing rapidly at $t = 50$ ns, V_{DD} starts to increase at $t = 50$ ns and eventually reaches a positive peak voltage at $t = 62.5$ ns. Within this duration, the n-well/p-substrate junction is always reverse biased, and thus only transient displacement current caused by n-well/p-substrate junction can be found within the SCR. Such displacement current will not cause TLU unless the frequency

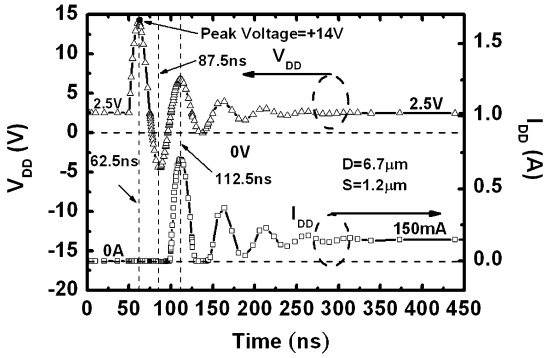

Fig. 13. Simulated V_{DD} and I_{DD} transient responses for TLU with a positive V_{Charge}. During the period of 50 ns $\leq t \leq$ 75 ns, TLU will not be triggered on by the n-well/p-substrate junction displacement current. Afterwards, during the period of 87.5 ns $\leq t \leq$ 112.5 ns, I_{Sb} will be produced to initiate TLU (I_{DD} significantly increases) when V_{DD} increase from its negative peak voltage to the normal operating voltage, $+2.5$ V.

(amplitude) of V_{DD} is large enough to induce large enough displacement current [9]. Afterwards, V_{DD} decreases from its positive peak voltage, at $t = 62.5$ ns, to its negative peak voltage, at $t = 87.5$ ns. Within this duration, n-well/p-substrate junction gradually changes from the reverse-biased state to the forward-biased state, while more and more minority electrons (holes) are injected into the p-substrate (n-well) region. Once these Q_{Stored} are subsequently (87.5 ns $\leq t \leq$ 100 ns) swept back to n-well (p-substrate) regions where they originally come from, TLU will be triggered on. As a result, I_{DD} will considerably increase during the period of 100 ns $\leq t \leq$ 112.5 ns. Obviously, TLU

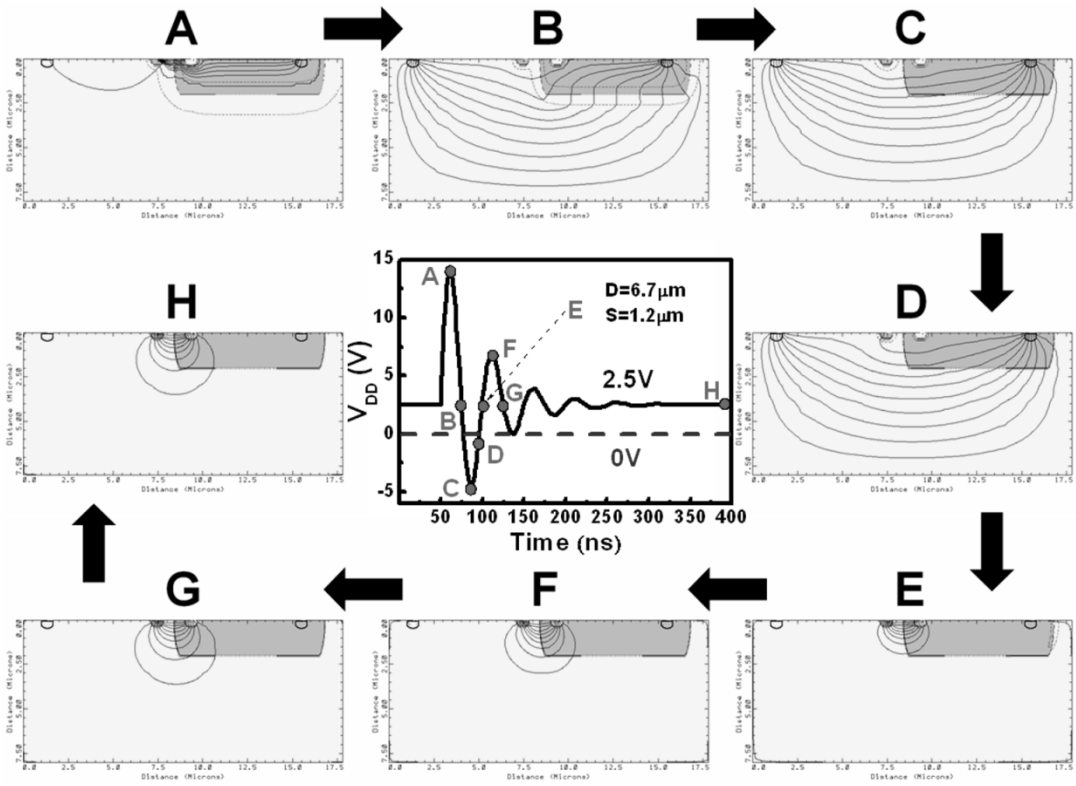

Fig. 14. Simulated 2-D current flow lines with respect to various transient timing points for TLU with a positive V_{Charge}. The n-well/p-substrate junction displacement current will not cause TLU (timing points A and B) until large enough I_{Sb} is produced (timing points E-H).

is sure to occur because the huge I_{DD} (150 mA, refer to Figs. 9 and 13) can be found when V_{DD} eventually returns to its normal operating voltage of $+2.5$ V.

Fig. 14 shows the simulated 2-D current flow lines with respect to various transient timing points with a positive V_{Charge}. The n-well/p-substrate junction displacement current will not cause TLU (timing points A and B). However, large forward well (substrate) contact current will appear when n-well/p-substrate junction is forward-biased (timing points C and D), and then TLU will certainly be triggered on if I_{Sb} is large enough (timing points E-H).

D. More Realistic Case

In real situation under the system-level ESD test, the oscillatory resonance voltage can randomly occur at both V_{DD} and GND nodes [12]–[14], but not only at the V_{DD} node. With considerations of such a realistic situation, Fig. 15 shows the simulated V_{DD}, GND, and I_{DD} transient responses on the SCR structure. Obviously, once V_{DD}-to-GND voltage is negative enough (87.5 ns $\leq t \leq$ 100 ns) to produce large enough I_{Sb} within the n-well/p-substrate junction, TLU can be easily triggered on afterwards when V_{DD}-to-GND voltage returns to a positive voltage (100 ns $\leq t \leq 112.5$ ns). Because the power and ground lines are widely distributed over the whole circuitry in a chip, such oscillatory resonance voltage can appear on some core circuitry. This fact implies that TLU can occur within the core circuitry, but not only in I/O circuitry. Thus, unlike the quasi-static latchup issue [17] which primarily concerns about latchup immunity on I/O circuitry, the latchup prevention skills such as layout optimization with additional guard rings [18],

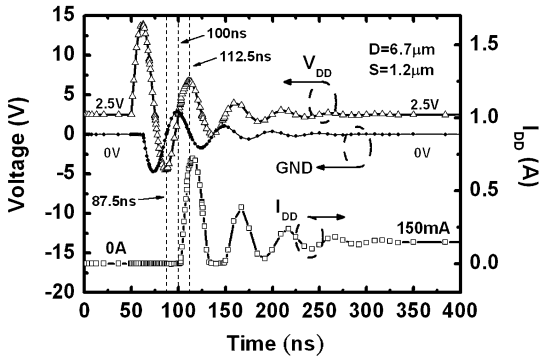

Fig. 15. Simulated V_{DD}, GND, and I_{DD} transient responses for TLU under a more realistic situation. V_{DD} and GND can be disturbed simultaneously by EMI under a system-level ESD test [12]–[14]. Once V_{DD}-to-GND voltage is negative enough (87.5 ns $\leq t \leq 100$ ns) to produce large enough I_{Sb}, afterwards TLU could be easily triggered on when V_{DD}-to-GND voltage returns to a positive voltage (100 ns $\leq t \leq 112.5$ ns).

other specific advanced process technologies, or even latchup self-stop circuit [19] may be necessary for the core circuitry to prevent TLU in CMOS ICs.

VI. Experimental Results for TLU

The component-level TLU measurement setup in Fig. 7 is used to perform the TLU test. With both positive and negative V_{Charge}, the measured V_{DD} (I_{DD}) transient response will be recorded through the voltage (current) probe to display on the oscilloscope. This will clearly indicate whether the TLU occurs (I_{DD} significantly increases) when the absolute value of positive or negative V_{Charge} gradually increases from 0 V during

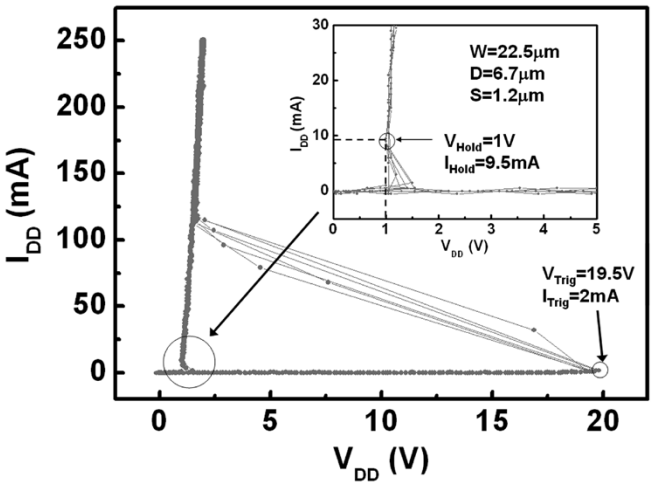

Fig. 16. Measured latchup dc I-V characteristic for the SCR structure.

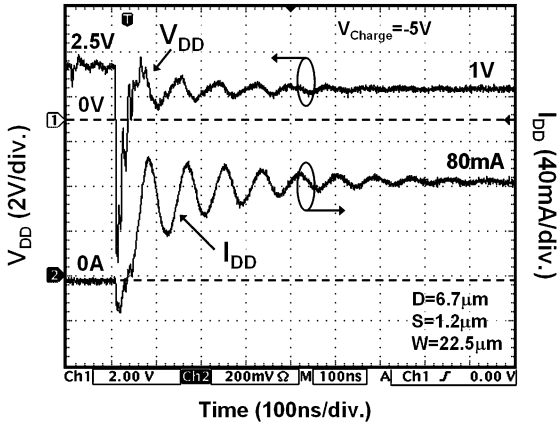

Fig. 17. Measured $V_{\rm DD}$ and $I_{\rm DD}$ transient waveforms from the TLU test with a negative $V_{\rm Charge}$ of -5 V. It is consistent with the device simulation results in Fig. 10 that TLU will be triggered on ($I_{\rm DD}$ significantly increases) when $V_{\rm DD}$ increase from its negative peak voltage to the normal operating voltage, $+2.5$ V.

the TLU test. More importantly, this will provide useful information for the comparisons between the TLU measurement and the device simulation. In addition, the specified SCR structure with layout parameters of $D = 6.7$ μm, $S = 1.2$ μm, and $W = 22.5$ μm fabricated in 0.25-μm CMOS technology is used for all the TLU measurements in this paper.

A. Measured Latchup DC I-V Characteristics

The measured latchup dc I–V characteristic for the fabricated SCR structure is shown in Fig. 16. The inset figure in Fig. 16 indicates the dc latchup trigger voltage (current), $V_{\rm Trig}$ ($I_{\rm Trig}$), is about 19.5 V (2 mA), while the dc latchup holding voltage (holding current), $V_{\rm Hold}$ ($I_{\rm Hold}$), is about 1 V (9.5 mA). Through comparing these measured dc latchup parameters with the simulated ones in Fig. 9, there is no large difference between the measured and the simulated dc latchup parameters. Thus, this noncalibrated device simulation tool is capable of performing the reasonable qualitative analysis to TLU.

B. TLU Measurement With Negative $V_{\rm Charge}$

With a negative $V_{\rm Charge}$ of -5 V, the measured $V_{\rm DD}$ and $I_{\rm DD}$ transient waveforms on the SCR structure are shown in Fig. 17. Obviously, forward $I_{\rm DD}$ current appears due to the forward-biased n-well/p-substrate junction when $V_{\rm DD}$ initially decreases below 0 V. Afterwards, $I_{\rm DD}$ will greatly increase while $V_{\rm DD}$ returns to above 0 V, and therefore TLU does occur. As a result, both $V_{\rm DD}$ and $I_{\rm DD}$ waveforms are slightly oscillatory under a low-impedance (high-current) latchup state. Finally, $V_{\rm DD}$ will eventually be pulled down to about the dc latchup holding voltage ($\sim$1 V) with the huge $I_{\rm DD}$ ($\sim$80 mA) after this transition.

Through the comparisons between the experimental and the device simulation results in Figs. 10 and 17, the experimental results are consistent with the device simulation results in time domain. For example, TLU will be triggered on due to large enough $I_{\rm Sb}$ while $V_{\rm DD}$ increases from - $V_{\rm Peak}$ to its normal operating voltage of $+2.5$ V. This can once again verify that the large number of $Q_{\rm Stored}$ can trigger on TLU while they are quickly swept back to the regions where they originally come from.

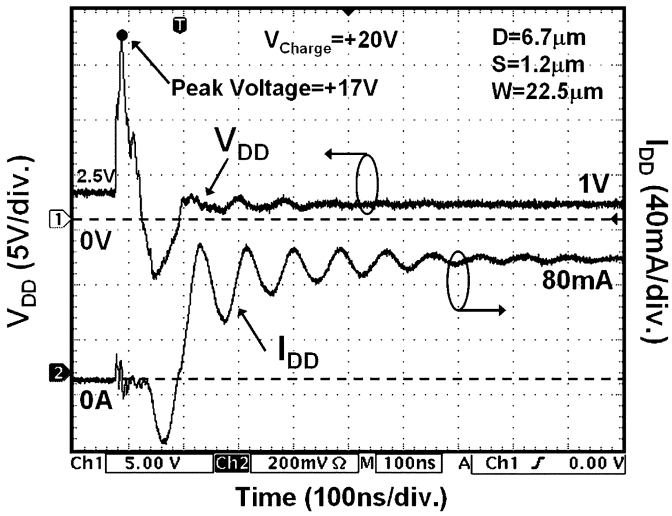

Fig. 18. Measured $V_{\rm DD}$ and $I_{\rm DD}$ transient waveforms from the TLU test with a positive $V_{\rm Charge}$ of $+20$ V. It is consistent with the device simulation results in Fig. 13 that TLU will not be initially ($V_{\rm DD} > 0$ V) triggered on by the n-well/p-substrate junction displacement current until large enough $I_{\rm Sb}$ is produced when $V_{\rm DD}$ increases from its negative peak voltage to the normal operating voltage, $+2.5$ V.

C. TLU Measurement With Positive $V_{\rm Charge}$

With a positive $V_{\rm Charge}$ of $+20$ V, the measured $V_{\rm DD}$ and $I_{\rm DD}$ transient waveforms on the SCR structure are shown in Fig. 18. $V_{\rm DD}$ begins to increase rapidly from the normal operating voltage ($+2.5$ V) to a positive peak voltage of $+17$ V. Meanwhile, the n-well/p-substrate junction is reversed biased, and thus only transient displacement current caused by the n-well/p-substrate junction can be founded within the SCR. Such junction displacement current is too small to initiate TLU because $I_{\rm DD}$ doesn't significantly increase when $V_{\rm DD}$ increases from the normal operating voltage ($+2.5$ V) to the positive peak voltage of $+17$ V. Afterwards, once large enough $I_{\rm Sb}$ is produced when $V_{\rm DD}$ increases from its negative peak voltage back to the normal operating voltage ($+2.5$ V), TLU will be initiated with large-increasing $I_{\rm DD}$. Moreover, both $V_{\rm DD}$ and $I_{\rm DD}$ waveforms are slightly oscillatory under a low-impedance (high-current) latchup state. Finally, $V_{\rm DD}$ will eventually be

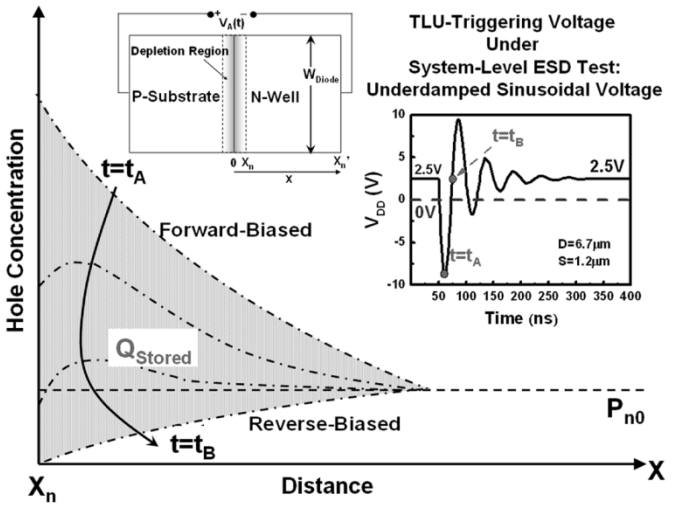

Fig. 19. Total stored minority carriers, $Q_{\rm Stored}$, causing $I_{\rm Sb}(t_A \le t \le t_B)$ inside the n-well region. The inset figure is an ideal 1-D diode used for deriving the 1-D analytical model of the averaged $I_{\rm Sb}(\equiv I_{\rm Ave})$ [15].

pulled down to about the dc latchup holding voltage (~1 V) with the huge $I_{\rm DD}$ (~80 mA) after this transition.

The physical mechanism of TLU under the system-level ESD test can be well proved once again by comparing the experimental results with the device simulation. As shown in Figs. 13 and 18, large enough $I_{\rm Sb}$ caused by the instantaneously forward-biased n-well/p-substrate junction can trigger on TLU more easily than the reverse junction displacement current does.

VII. Discussion

It has been clarified that the sweep-back current, $I_{\rm Sb}$, caused by the minority carriers stored within the parasitic pnpn structure of CMOS ICs is the major cause of TLU under the system-level ESD test. Based on a simple 1-D analytical model of $I_{\rm Sb}$ [15], the dominant parameter to initiate TLU can be identified. In addition, the minimum magnitude of the applied voltage to initiate TLU under different damping frequencies can be determined by the device simulations. By combining these 2-D device simulation results and the 1-D model of $I_{\rm Sb}$, the minimum $I_{\rm Sb}$ or the minimum number of the total stored minority carriers $(Q_{\rm Stored})$ to initiate TLU can be also estimated. To further provide the evidence that $I_{\rm Sb}$ is the major cause of TLU, the transient responses on the minority carriers stored within SCR are calculated.

A. Dominant Parameter to Induce TLU

As shown in the inset figure of Fig. 19, with the assumption that the n-well/p-substrate junction is treated as an ideal 1-D diode with step junction profile, a simple 1-D analytical model of the averaged $I_{\rm Sb}(\equiv I_{\rm Ave})$ [15] can be expressed as

$$I_{\rm Ave} \equiv \frac{Q_{\rm Stored}}{t_B - t_A} \tag{2}$$

where $t_A(t_B)$ is the initial (final) timing point of a specific duration when $I_{\rm Sb}$ exists, as shown in Fig. 19. $Q_{\rm Stored}$ represents the

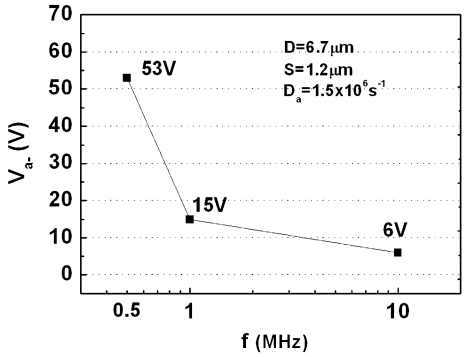

Fig. 20. Simulated V_{a-} dependences on damping frequency (f). V_{a-} is defined as the minimum magnitude of the negative applied voltage to initiate TLU.

total stored minority carriers (holes) causing $I_{\rm Sb}(t_A \le t \le t_B)$ inside the n-well region, which is given by

$$Q_{\rm Stored} = q\frac{n_i^2}{N_D}L_P\left(1 - e^{-\frac{X_{n\prime} - X_n}{L_P}}\right)\left(e^{\frac{qV(t_A)}{kT}} - e^{\frac{qV(t_B)}{kT}}\right). \tag{3}$$

From (2) and (3), $I_{\rm Ave}$ can be further simplified as

$$\begin{aligned} I_{\rm Ave} &\equiv \frac{Q_{\rm Stored}}{t_B - t_A} = \frac{Q_{\rm Stored}}{(1/f)/4} \\ &= 4fq\frac{n_i^2}{N_D}L_P\left(1 - e^{-\frac{X_{n\prime} - X_n}{L_P}}\right)\left(e^{\frac{qV(t_A)}{kT}} - e^{\frac{qV(t_B)}{kT}}\right) \\ &= Z \cdot f \cdot e^{\frac{qV(t_A)}{kT}}, \left(\because e^{\frac{qV(t_B)}{kT}} = e^{\frac{V(t_B)}{kT/q}} = e^{\frac{-2.5}{0.0259}} \cong 0\right) \end{aligned} \tag{4}$$

where

$$Z = 4q\frac{n_i^2}{N_D}L_P\left(1 - e^{-\frac{X_{n\prime} - X_n}{L_P}}\right) \tag{5}$$

is a constant and independent on damping frequency (f), applied voltage amplitude (V_a), and damping factor (D_a). By substituting $t_A = t_d + (1/f)/4$ into (1), $V(t_A)$ can be expressed as

$$\begin{aligned} V(t_A) &= V_0 + V_a \cdot \exp(-(t_A - t_d)D_a) \cdot \sin(2\pi f(t_A - t_d)) \\ &= V_0 + V_a \cdot \exp\left(-\frac{D_a}{4f}\right). \end{aligned} \tag{6}$$

From (4) and (6), it can be obviously identified that f is dominant to $I_{\rm Ave}$ (i.e., dominant to induce TLU), because there is not only a proportional exponential relationship between f and $V(t_A)$ in (6), but also a multiplication factor " f " on $I_{\rm Ave}$ in (4).

B. Minimum Applied Voltage Amplitude to Initiate TLU

The minimum V_a to initiate TLU can be determined by the device simulation results. For the underdamped sinusoidal voltage with D_a of 1.5×10^6 s^{-1}, the simulated V_{a-} dependences on

f are shown in Fig. 20. $V_{a\_}$ is defined as the minimum magnitude of the negative applied voltage to initiate TLU. Clearly, $V_{a\_}$ decreases with f. This can be demonstrated by (2) where the higher f (i.e., smaller t_B-t_A) can initiate TLU by a smaller $V_{a\_}$ (i.e., smaller $Q_{\rm Stored}$), if the critical $I_{\rm Ave}$ to initiate TLU is fixed. Thus, the critical value of D_a, V_a, or f to initiate TLU isn't fixed but correlated with each other, because D_a, V_a, and f are all correlated with $I_{\rm Ave}(I_{\rm Sb})$ to determine the occurrence of TLU [20].

C. Minimum $Q_{\rm Stored}$ or $I_{\rm Sb}$ to Initiate TLU

By combining the 2-D device simulation results and the 1-D analytical model of $I_{\rm Ave}$, the minimum $I_{\rm Ave}$ or $Q_{\rm Stored}$ to initiate TLU can be estimated. As shown in Fig. 20, for the underdamped sinusoidal voltage with D_a of 1.5×10^6 s^{-1} and f of 10 MHz, the minimum magnitude of the negative applied voltage $(V_{a\_})$ to initiate TLU is 6 V. With this trigger condition, it can be calculated from (1) that $V(t = t_A = t_d + (1/f)/4 = t_d + 25\ {\rm ns}) = 3.26$ V. However, it is improper to directly apply such a high $V(t_A)$ of 3.26 V into (3) to obtain $Q_{\rm Stored}$, because the forward-biased p-substrate/n-well junction current is dominated by the parasitic series resistance effect at a high current state $(t = t_A)$. As a result, the $V(t_A)$ considering the parasitic series resistance effect of the p-substrate/n-well diode can be defined as $V(t_A)'$ and extracted from

$$I(t_A) = J_0 \times W_{\rm Diode} \times e^{\frac{qV(t_A)'}{kT}} \tag{7}$$

where $W_{\rm Diode}$ is the distance perpendicular to X direction of the ideal 1-D p-substrate/n-well diode, as shown in the inset figure of Fig. 19. With J_0 of about 10^{-19} A/μm^2 at T = 300 K, $W_{\rm Diode}$ of about 5 μm (approximated from the 2-D SCR structure in Fig. 6), and $I(t_A)$ of 2.676×10^{-3} A/μm from the simulation result, $V(t_A)'$ of 0.95 V can be calculated from (7). Thus, with $N_D = 10^{17}$ cm^{-3}, $L_p = (D_p\tau_p)^{0.5} \cong 30$ μm at T = 300 K, V $(t = t_B) = 2.5$ V, and the assumption that the distance between the depletion region edge and the contacts of 1-D p-substrate/n-well diode is much larger than the minority carrier diffusion length (i.e., $X_{n'} - X_n \gg L_p$), the minimum $Q_{\rm Stored}$ to initiate TLU of 2.57×10^{-11} C/μm^2 can be calculated from (3). With the known $Q_{\rm Stored}$ and t_B-$t_A = (1/f)/4 = 25$ ns, the minimum $I_{\rm Ave}$ to initiate TLU of 1.03×10^{-3} A/μm^2 can be calculated from (2).

D. Transient Responses on the Minority Carriers Stored Within SCR

To further provide the evidence that $I_{\rm Sb}$ is the major cause of TLU, the transient responses on the minority carriers stored within SCR $Q_{\rm Stored}(t)$ can be estimated from (3) by using t to substitute for t_A. For the underdamped sinusoidal voltage with the same parameters (D_a, f, and V_a of 2×10^7s^{-1}, 20 MHz, -14.6 V, respectively) as those in the case with negative $V_{\rm Charge}$ of Figs. 10 and 11, the calculated transient responses of $Q_{\rm Stored}$ (hole) in the n-well region are shown in Fig. 21. Compared with the simulated TLU transient responses in Figs. 10 and 11, the minority carriers (holes) stored in the n-well region significantly increases with forward well contact current (50 ns $\leq t \leq$ 62.5 ns) when $V_{\rm DD}$ decreases from 2.5 V to $-V_{\rm peak}$. Afterwards, $Q_{\rm Stored}$ decreases because these minority holes are swept back to their original p-substrate region (62.5 ns $\leq t \leq$ 75 ns). As a result, TLU will be triggered on by these swept-back $Q_{\rm Stored}$, so the anode current will significantly increase (75 ns $\leq t \leq$ 87.5 ns). From Figs. 10, 11, and 21, the swept-back current $I_{\rm Sb}$ can be confirmed as the major cause of TLU during system-level ESD stress.

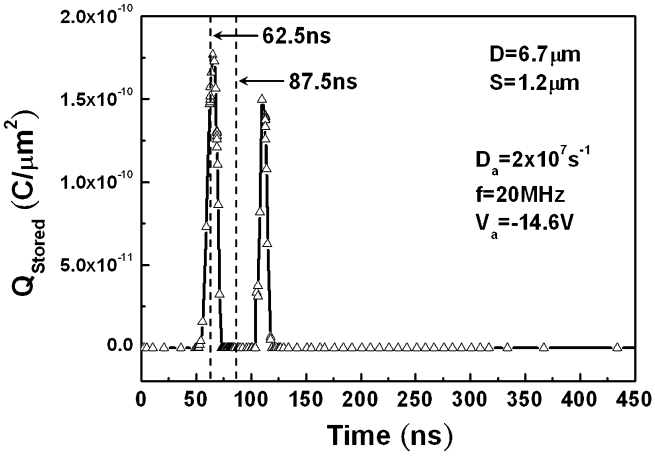

Fig. 21. Calculated transient responses of $Q_{\rm Stored}$ (hole) in the n-well region. The underdamped sinusoidal voltage has the same parameters as those used in the negative $V_{\rm Charge}$ case of Figs. 10 and 11 (D_a, f, and V_a of 2×10^7 s^{-1}, 20 MHz, and -14.6 V, respectively).

VIII. Conclusion

The underdamped sinusoidal voltage stimulus has been clarified as the realistic TLU-triggering stimulus under the system-level ESD test. With the aid of device simulation, the specific "sweep-back" current caused by the minority carriers stored within the parasitic pnpn structure of CMOS ICs has been qualitatively proved to be the major cause of TLU. Through comparisons between device simulations and experimental measurements, TLU reliability issue may still exist in a qualified CMOS IC product through quasi-static latchup test. Thus, an efficient TLU measurement setup is needed to evaluate the TLU reliability of CMOS IC products. Because TLU reliability issue potentially exists within the whole circuitry of CMOS ICs, latchup prevention skills such as layout optimization, the specific advanced process technologies, or circuit technique may be necessary to improve TLU immunity for core circuitry. Through both the understanding of physical mechanism and the proposed simulation/verification methodology on TLU, the safe design/layout rules or circuit techniques in CMOS ICs can be developed against TLU events.

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