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Characterization of polysilicon thin-film transistors with asymmetric source/drain implantation

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Abstract

The effect of asymmetry tilt angle ion implantation on polysilicon thin-film transistors (TFTs) device characteristics are investigated. This asymmetric source/drain (S/D) TFTs structure exhibits low leakage current and suppressed kink effect due to the relief of higher electric field near the drain junction side. It is shown that the optimal implantation tilt angle is 30° in our annealing condition. And the anomalous off-state current is more than two orders of magnitude lower than that of the conventional TFTs. By well controlled the LDD region, this structure can act as a conventional structure in the on-state and the turn-on current will not be degraded. Besides, the device under severe hot carrier bias stress shows better hot carrier endurance.
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1. Introduction

Polycrystalline thin-film transistors technology are promising for active matrix liquid crystal display (AMLCD) applications, the anomalous off-state leakage current represent one of important issues. It is well known that field emission via grain-boundary traps due to high electric field in the drain depletion region would dominate off-state leakage current [1]. A common method proposed to reduce the severe anomalous leakage current of polycrystalline silicon TFTs is to alleviate the electric field near the drain junction [2–4]. The LDD implant is to produce a lightly doped region near the channel. The LDD region with lower dosage is self-aligned to the gate electrode. It is useful to improve drain leakage by using LDD structure. However, the degradation of on-current due to increased parasitic resistance introduced in

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the LDD region. The required extra lithography and ion doping steps will increase the fabrication costs and make it more complicated in processing [5,6]. In this study, a new self-align top gate thin-film transistor structures can shows excellent leakage performance without additional mask. The structure is polycrystalline thin-film transistor with asymmetric source/drain implantation. By the tilt implantation of source/drain method, the offset region beside the drain junction forms the lightly doped drain. As well as the LDD TFTs structures, the light doped drain region suppresses the field effect near the drain junction. Moreover, by well controlled the lightly doped drain region, this structure can act as a conventional structure in the on-state and turn-on current will not be degraded. And the hot carrier instabilities [7] can be also improved.

2. Experimental

The fabrication procedures of these devices are described as following: Undoped amorphous silicon layers of thickness about 50 nm or 100 nm were deposited by low pressure chemical vapor deposition (LPCVD) on buried oxide at 550 °C. The amorphous silicon films were recrystallized by solid phase crystallization (SPC) method at 600 °C for 24 h in an N_2 ambient. These recrystallized polysilicon films were patterned into active region islands. After defining the active region, the TEOS gate oxide and a 300 nm polysilicon films were deposited. This polysilicon was then patterned and etched as the gate electrode. After that source and drain region were implanted in different twist and tilt angle by Arsenic. The twist angle came with the tilt angle because of the implanter machine roll wafers with three dimensions at the same time. The twist angle was fit to the tilt angle by exactly measurement. After ion implantation, the samples were annealed under the optimum condition. Then, passivation oxide was deposited and the contact hole was defined. The aluminum was sputtered and defined as the metal pad. HP-4156 was used to measure all the current–voltage (I–V) characteristics and exact device parameters.

3. Results and discussion

The current–voltage characteristics with exchanging source/drain electrode. In Fig. 1, we see subthreshold characteristics of tilt 30° sample get a better performance when the high potential was biased at the drain side. The leakage current of drain side measurement would not be exponentially increasing with gate and drain voltage increased. It means that the lightly-doped-drain region is properly formed only at the drain side and the source side junction is heavily doped. So that the electric field acts at the source side and makes leakage current increasing anomalously when bias was added at the source side. In this figure it could be informed that when gate bias at −10 V, source side leakage current would reach almost 0.1 μA. However, drain side leakage current could be suppressed to 50 pA. There is a three order of leakage current improvement. All devices with W/L = 10 μm/3 μm are measured at V_G = 5, 6 and 7 V the I_D–V_D curves have been shown in Fig. 2. When device is measured at the drain side, better kink effect [8] is performed than measured at the source side. In the tilt 30° samples, when VD was added to 5 V, source side current shows that kink effect is obviously. However, the drain side measurement was not till the drain voltage

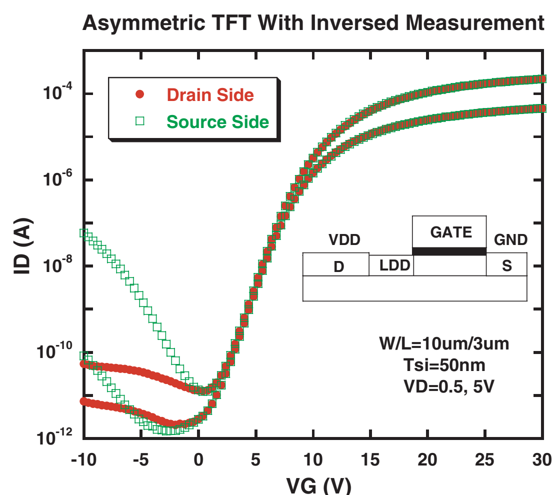

Fig. 1. The asymmetric source/drain implantation with tilt 30° subthreshold characteristics of inversion measurement.

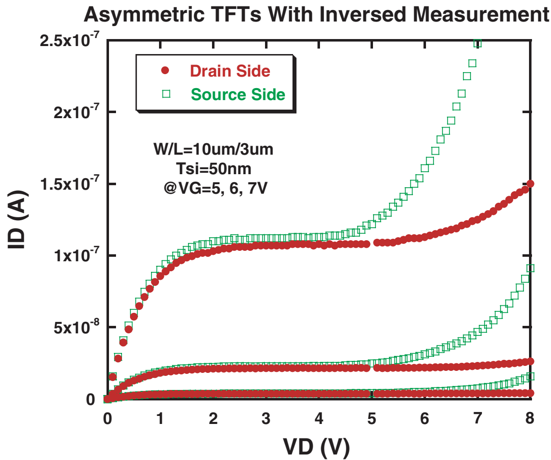

Fig. 2. The asymmetric source/drain implantation with 30° tilt I_D–V_D of inversion measurement.

increasing to 7 V. The kink effect happened in polycrystalline TFTs which caused by the high field emission and grain-boundary traps is effectively depressed by the LDD. And this lightly-doped-drain exists only at the drain. In Fig. 3, the transfer curves of conventional polycrystalline TFTs and asymmetric source/drain implantation polycrystalline TFTs are shown. Anomalous leakage current of conventional TFTs increases exponentially with difference between gate and drain voltage caused by the drain side high electric field and grain-boundary defects. However this novel asymmetric source/drain implantation polycrystalline TFTs does not show this shortcoming. This contribution is made by the LDD junction that suppresses the drain side high electric field when gate bias is strongly negative. Compare with those two devices, we can see that when gate bias to −10 V the drain leakage of conventional polycrystalline TFTs is about 0.1 μA, but asymmetric one is 50 pA. There is almost 3.5 order leakage suppressed we made in this experiment. This is a great improvement for polycrystalline TFTs. At the on-state performance, asymmetric polycrystalline TFTs have no difference with conventional ones. Since the lightly-doped region is only at drain side but not at source side. The series resistance of polycrystalline TFTs channel is much bigger than that of metal–oxide–silicon field effect transistors (MOSFETs). So the series resistance at on-state would not be so serious in polycrystalline thin-film transistors. This is why the on-state current not degraded with additional lightly-doped region. As a result, the new polycrystalline TFTs without any additional mask which show excellent leakage current performance and on-state current performance. In Fig. 4, we show the transfer curves of

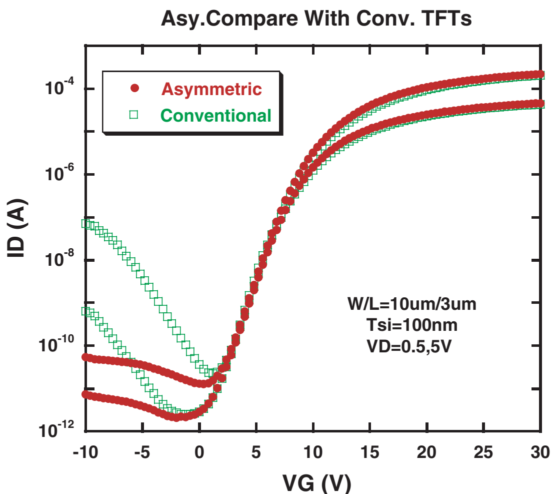

Fig. 3. The I_D–V_G curves of conventional polycrystalline TFTs and asymmetric source/drain implantation polycrystalline TFTs.

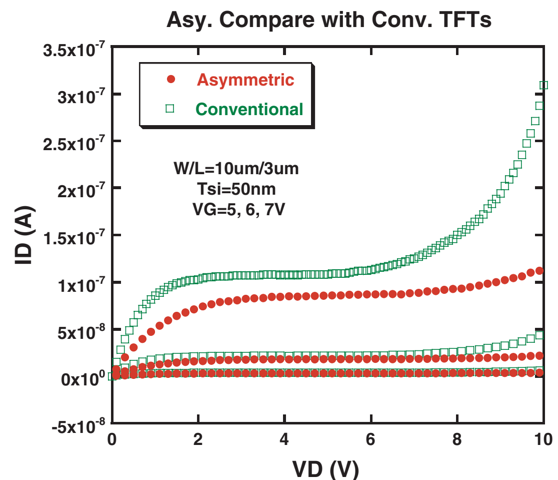

Fig. 4. The I_D–V_D curves of asymmetric polycrystalline TFTs and conventional TFTs. Asymmetric TFTs shows better kink effect than conventional ones.

asymmetric TFTs and conventional TFTs. All devices with $W/L = 10\ \mu m/3\ \mu m$ are measured at $V_G = 5$, 6 and 7 V. In this figure, asymmetric polycrystalline TFTs show better kink effect performance than conventional TFTs. In the conventional polycrystalline TFTs, when V_D was added to 5 V till the drain voltage increasing to 7 V. That means kink effect happened in polycrystalline TFTs which caused by the high field emission and grain-boundary traps is effectively depressed by the LDD. Kink effect is an important issue for device operation. Better kink effect means bigger operation range for polycrystalline TFTs and that is what the new structure asymmetric source/drain implantation polycrystalline TFTs do. The threshold voltage of each device with different channel length are measured shown in Fig. 5. For both conventional and asymmetric source/drain implantation TFTs, threshold voltage is proportional to channel length. However, conventional TFTs threshold voltage roll off is a little serious than asymmetric source/drain implantation. The reason for this phenomenon is the impact ionization in conventional TFTs is more serious than asymmetric TFTs. The impact ionization enhance the threshold voltage roll off. Hot carrier stress was used to test the long-term reliability of LTPS TFTs in this work. Fig. 6 illustrates the threshold voltage variations and the degradation in TFTs under static hot-carrier stress. ΔV_{th} is defined as the TFTs being kept at a high electric field in the drain junction. Notably, the dc stress conditions are $V_{DS} = 30$ V and $V_{GS} = 15$ V for 1000 s. This effect occurs due to the higher electric field at the drain junction. The high electric field promotes impact ionization, resulting in numerous grain-boundary traps being created in the drain junction. The large drain junction electric field during hot carrier stress resulted

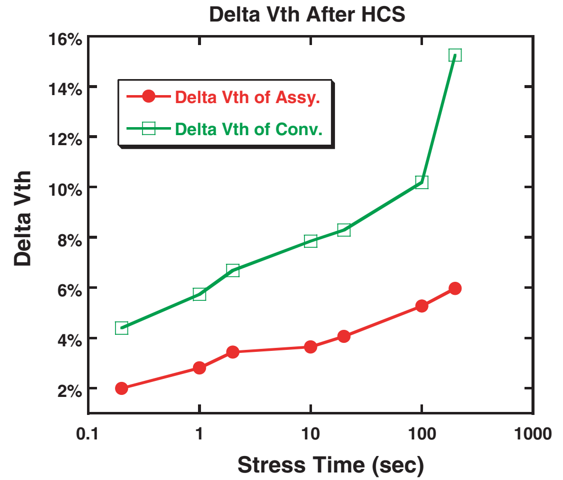

Fig. 6. Threshold voltage variation after hot carrier stress.

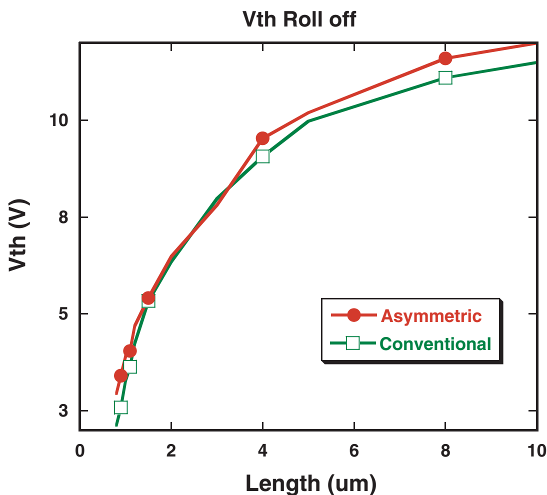

Fig. 5. Threshold voltage roll off of asymmetric source/drain implantation and conventional TFTs.

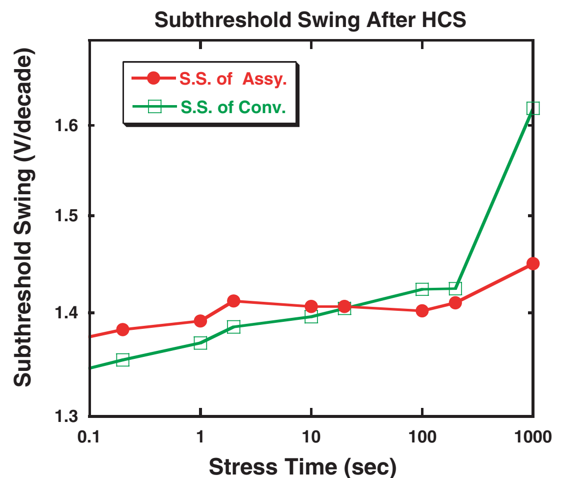

Fig. 7. Subthreshold swing variation after hot carrier stress.

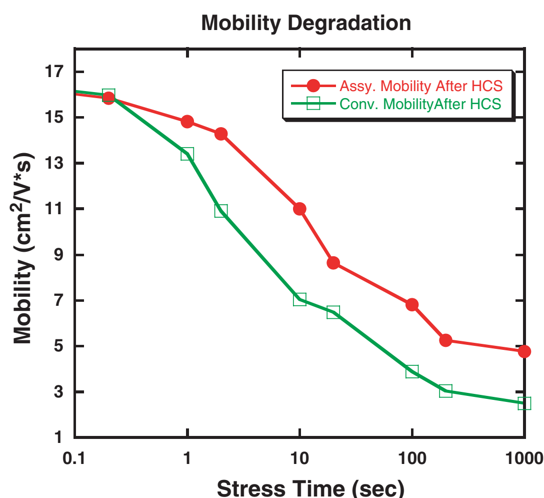

Fig. 8. Mobility degradation after hot carrier stress.

in sever degradation on conventional structure. On the other hand, the asymmetric TFTs exhibited better hot carrier endurance than conventional one due to the drain junction electric field relief. Figs. 7 and 8 show subthreshold swing and mobility degradation between asymmetric and conventional structure. Those two factors show the same results as the threshold voltage degradation. In our structure, we can effectively reduce the electric field near the drain side and obtain the optimal results in the hot carrier stress.

4. Conclusions

The anomalous leakage current appearing in conventional thin-film transistors could be suppressed obviously in this device and contributed by the lightly-doped-drain region which suppresses the drain side electric field. The on/off current ratio of asymmetric TFTs could be improved to 10^7 which is larger than conventional device. Besides, parameters such as subthreshold swing, threshold voltage, and carrier mobility show better performance than the conventional TFTs.

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