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Power and Substrate Noise Tolerance of Configurable Embedded Memories in SoC

MENG-FAN CHANG AND KUEI-ANN WEN
Institute of Electronics, National Chiao Tung University, Hsin Chu, Taiwan

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Abstract. When subject to various power and substrate noise, configurable embedded memories in multimedia SoCs are importantly affected with pattern-dependant soft failures. This work investigates the effects of such failures on memory cells, arrays and circuit design. The ground bounce reduces the memory cell current more than the supply voltage drop or the substrate bias dip. A noise track-and-filter (NTAF) architecture, which is a self-timed architecture with specific layout patterns, is presented to provide the required timing relaxation, while minimizing the speed degradation. This NTAF method provides greater noise tolerance and design for manufacturing (DFM) capability. Configurable embedded SRAM and ROM in 0.18 μm CMOS process are studied.

Keywords: ROM, SRAM, substrate noise, supply noise

1. Introduction

Since digital, mixed-signal, radio-frequency (RF), and memory blocks are integrated on a single substrate of a chip, the supply and substrate noise may not only degrade the overall system performance, but also causes sensitive blocks to suffer from functional failures. Moreover, the operating environments, which cannot be predicted by the designers of silicon-IP (SIP), vary from chip to chip across applications. Accordingly, high-quality embedded memories must be designed to operate in noisy environments in SoCs.

Previous studies have investigated the effects of supply and substrate noise on digital [1, 2], mixed-signal [3, 4], and RF [5, 6] circuits. Also, some reports [1, 7] have noted that the supply noise dominates substrate noise. Accordingly, dedicated substrate bias and guard rings have been developed and demonstrated to be highly effective in reducing substrate noise for digital and mixed-signal circuit [8–10].

The demands for higher speed, lower power and larger capacity embedded memories have defined the trends of multimedia SoCs. Design and manufacturing yield of embedded memories have become the bottlenecks for the success of SoCs associated with their unique characteristics of the circuit and the layout. A detailed study of the effects of power and substrate noise on the embedded memories is necessary. Unfortunately, few reports on this topic have been published. This study elucidates power and substrate noise in configurable embedded SRAM and ROM. The NTAF architecture is developed to improve the immunity to noise and DFM capability.

The remainder of this presentation is organized as follows. Section 2 discusses the proposed NTAF techniques. Section 3 discusses the proposed tracking cells in NTAF architecture under supply and substrate noise considerations. Section 4 compares the performance to that of conventional embedded memories. Section 5 draws our conclusions.

2. Proposed Noise Track-and-Filter Architecture

2.1. Power and Substrate Noise in Memory Cell Array

When a transient current arises in a chip, the power lines may encounter voltage drop and ground bounce

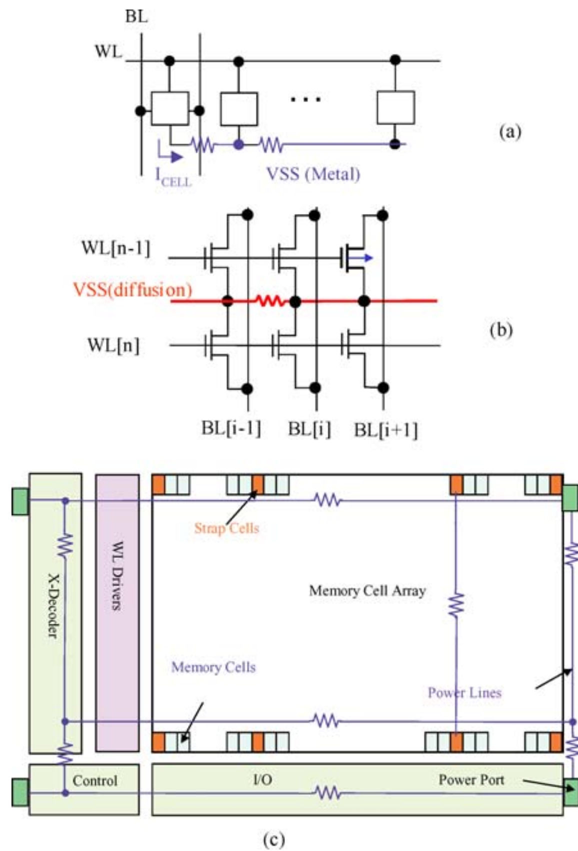

Figure 1. Ground (VSS) line structure in (a) SRAM (b) ROM, and (c) a memory architecture that incorporates strap cells for power-line mesh.

which could be oscillating or ringing, mainly in response to the parasitic resistance and inductance of interconnects and bonding wires. In popular embedded memories, including SRAM and ROM, the power lines in the cell array are normally implemented using narrow-width metal lines or diffusion strips in order to meet the tight-area constraints, as depicted in Fig. 1. Substrate contacts, which bias the substrate and prevent latch-up, are generally shared and placed outside memory cells to save silicon area. To provide the extra power mesh and substrate connections, the memory cell array is added with the strap cells. Strap cells are shared along the row (wordline) direction by every *m* memory cells, where, in practice, *m* may range from 16 to 64 for SRAM and normally exceeds 32 for ROM. Figure 1(c) illustrates the power plan and placement of the strap cells in a typical embedded memory architecture. Although the power-line mesh and strap cells improve the supply and ground uniformities, each memory cell still has different power supply conditions because the paths to the power ports in a large memory have different resistance.

During a memory access operation, when a wordline (WL) is selected, all memory cells connected to the wordline are activated, sinking current to the same ground line. More memory cells connected to the wordline constitute a larger current sink. This simultaneous current sink to a single ground line increases the voltage of the ground line and reduces the memory cell currents. Intuitively, the memory cells in the middle of the array and between the two strap cells have the worst-case wordline-induced ground bounce, because the resistance (distance) to the power connectors of an embedded memory is greatest. Hence, they suffer from the most severe cell current degradation, as presented in Fig. 2. Additionally, ROM code-pattern is another factor in determining the variation of the ground bounce, as presented in Fig. 2(b). It determines the number of memory cells on a particular row that discharge to the ground line. Clearly, the divided wordline methods [11–13] can reduce the wordline-induced ground bounce by reducing the number of activated memory cells in a row.

A wordline driver on the edge of a memory cell array typically has cascade buffers and large-size transistors to drive heavy loads on a wordline. The driver consumes a large peak current during the wordline transition. This switching activity induces a voltage drop and ground bounce on the power lines, and generates substrate noise near the driver by the current injection mechanism [8], as showed in Fig. 3. This transition-induced noise generated by the wordline drivers causes the memory cells, which are positioned close to the wordline drivers, suffer from the fluctuations in cell current.

Therefore, each memory cell may be subject to various power and substrate noise, according to its location and data pattern. This situation causes fluctuations in cell currents during the read operations and alters the bell-shape nominal distribution to a different center and/or extreme values. Figure 4 presents memory cell current degradations, which cause functional failure. This effect is stronger in larger memory cell arrays.

2.2. NTAF Architecture

In embedded memories, self-generated and external power and substrate noise lead to a variation in location-dependent voltage bias for transistors and a wide

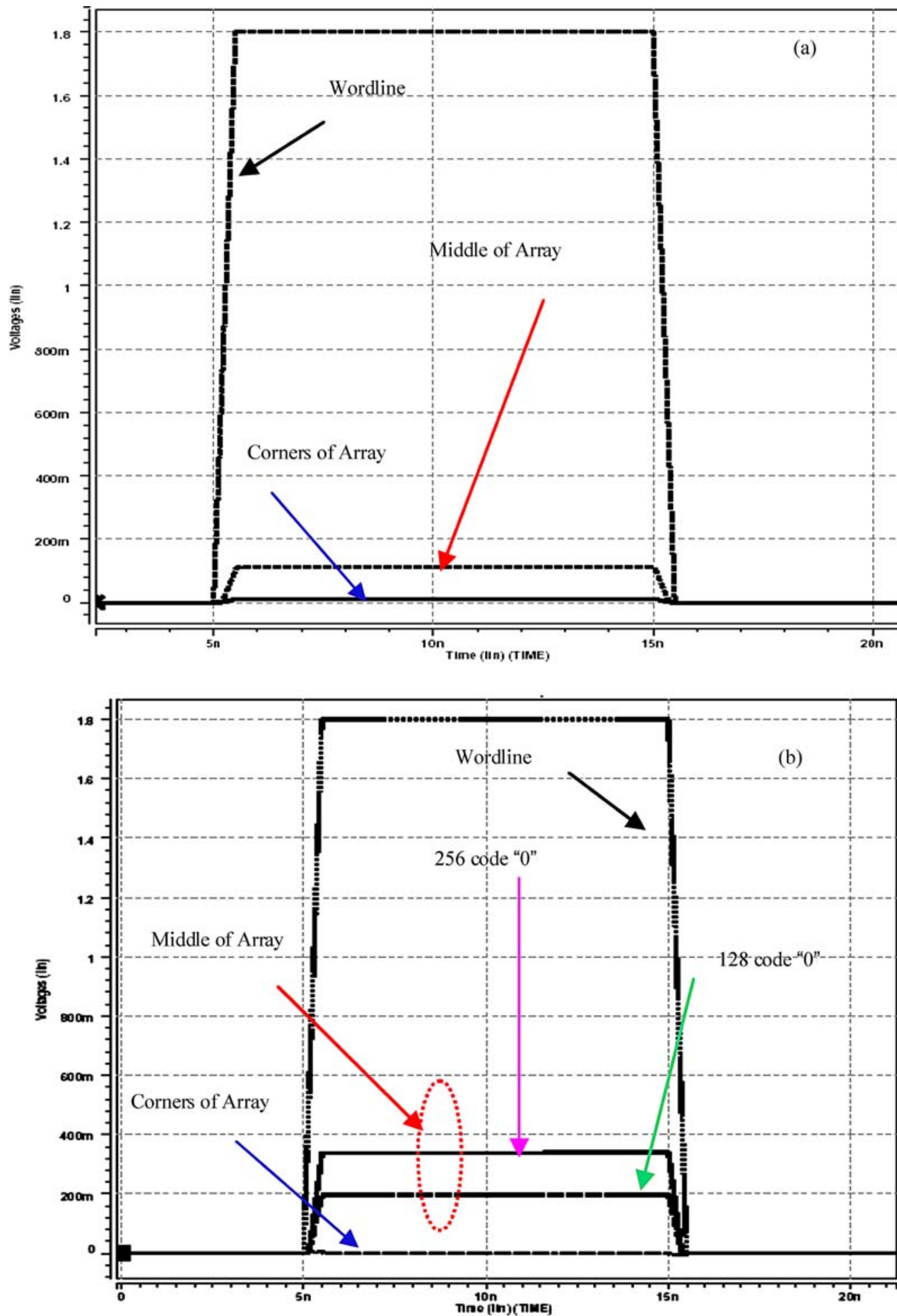

Figure 2. Self-generated ground bounces in (a) 6T-SRAM and (b) ROM with 512 and 256 cells per row, respectively.

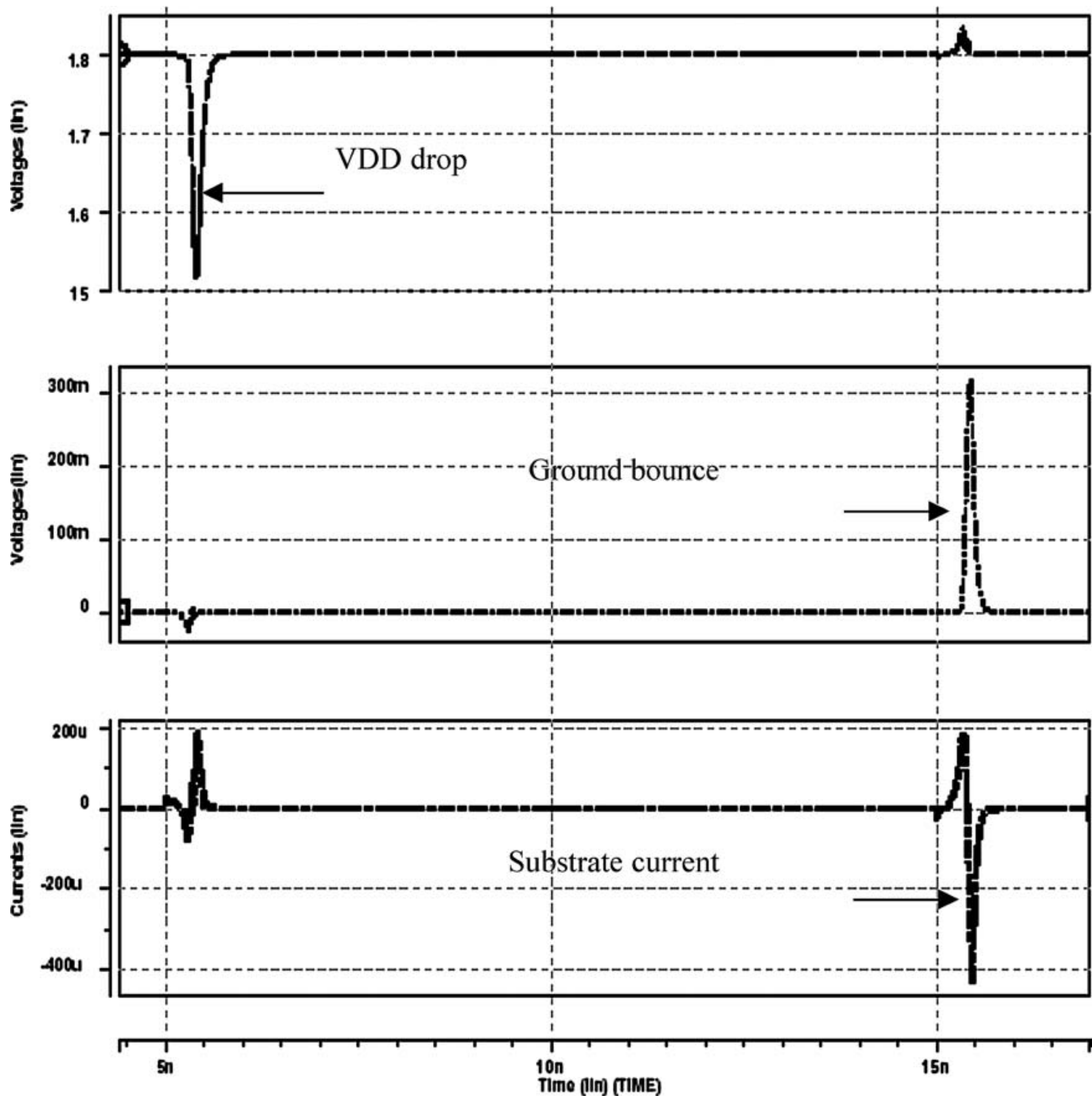

Figure 3. Power and substrate noise induced by a wordline driver in a ROM with 512 ROM cells per row.

distribution of cell currents. The degradation in the cell current, particularly in the tail bits, causes sensing failure in conventional configurable embedded memories. However, relaxing the sensing time with a fixed amount of delay may not be a realistic solution because a suitable timing margin is hard to determine during the design phase of the embedded memories. On the other hand, pessimistically reserving too much timing margin for yield improvement reduces the speed performance and increases the power consumption.

Figure 5 presents NTAF architecture. Two NTAF tracking columns are located at the left-edge and in the middle of a memory cell array. These two tracking columns are between two strap-cell columns for tracking the bulk-source voltage difference, if any. The ground lines of the proposed tracking cells in a tracking column are shared vertically and connected to those horizontal ground lines of neighboring memory cells. This physical layout pattern ensures that all active tracking cells in a tracking column have the same ground condition as their neighboring memory cells in

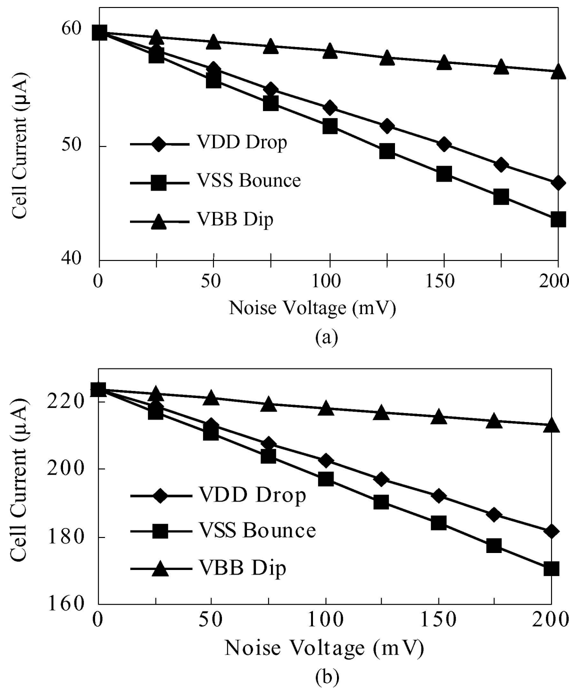

Figure 4. Fluctuations in cell current due to supply voltage (VDD) drop, ground (VSS) bounce, substrate bias (VBB) dip on (a) 6T-SRAM and (b) ROM cell in 0.18 μm logic process.

the accessed row of the memory cell array. The vertical ground lines in a tracking column occupy area and are routed using metal 2 or metal 4.

The tracking column at the left-edge of memory cell array is physically close to the wordline drivers. Therefore, this tracking column tracks the power and substrate noise injected into the memory cell array due to the switching activities of wordline drivers. The ground lines of the selected tracking cells and that of the accessed row are connected. Thus, the worst self-generated ground noise in the middle of the memory cell array also reflects in the active tracking cells in the tracking column in the middle of memory cell array. Both tracking columns in NTAF architecture can track the location-dependent supply and substrate noise in a memory cell array; they have only small area overhead.

2.3. *Tracking Column in NTAF Architecture*

A tracking column, as depicted in Fig. 5(b), in NTAF architecture consists of k active NTAF tracking cells and $n - k$ inactive NTAF tracking cells. n equals to the number of nominal memory cells on a nominal bitline. The value of k is selected according to the design tradeoff among speed, sensing margin, and coverage of the memory cell current. The active NTAF tracking cells, controlled by a "dummy wordline" signal, are positioned in the middle of a tracking column and behave as a current source that discharges the dummy bitline. The other inactive tracking cells then mimic the loading of nominal memory cells on a nominal bitline.

In conventional configurable memories with various bitline tracking schemes, the extra column (dummy bitline) for tracking the voltage swings on nominal bitlines is located at the edge of a memory cell array, as in [14, 15]. The location of the current source circuit is fixed and placed at the end of the dummy bitline. This approach works well for small memories under noiseless power conditions, given tight manufacturing process control such that all memory cells exhibit only small cell current fluctuations.

However, such conventional memories exhibit large mismatch between the voltage swing of the dummy bitline and that of the nominal bitlines under a wide range of cell current distributions and noisy power and substrate voltages, in SoC applications.

Within the width of a wordline pulse, each selected memory cell develops the bitline swing from its own cell current (I_{CELL}). Clearly, the bitline swing developed by a *tail* bit, which has a smaller cell current than the other cells, is smaller. The sensing of the tail bit is discussed below.

Assume that k active tracking cells are connected to a dummy bitline. Their cell currents are summed to develop the voltage swing on the dummy bitline, as in (1).

$$I_{\text{TRACK}} = \frac{1}{k} \sum_{i=1}^{k} I_{\text{CELL}}(i) \tag{1}$$

If the mean cell current of these active tracking cells, I_{TRACK}, on the dummy bit line is close to the mean cell current I_{TYP} of a memory cell array, then the cell current variation ΔI_{CELL} that is tolerable by the bitline tracking scheme is the difference between the cell currents of typical bits and the tail bits:

$$\Delta I_{\text{CELL}} = I_{\text{TYP}} - I_{\text{TAIL}} \tag{2}$$

The outcome of the design tradeoff between speed and manufacturability is the difference between the voltages swings of bitlines, $\Delta V_{\text{TYP-TAIL}}$. Then, a deviation in the cell current distribution of no larger than

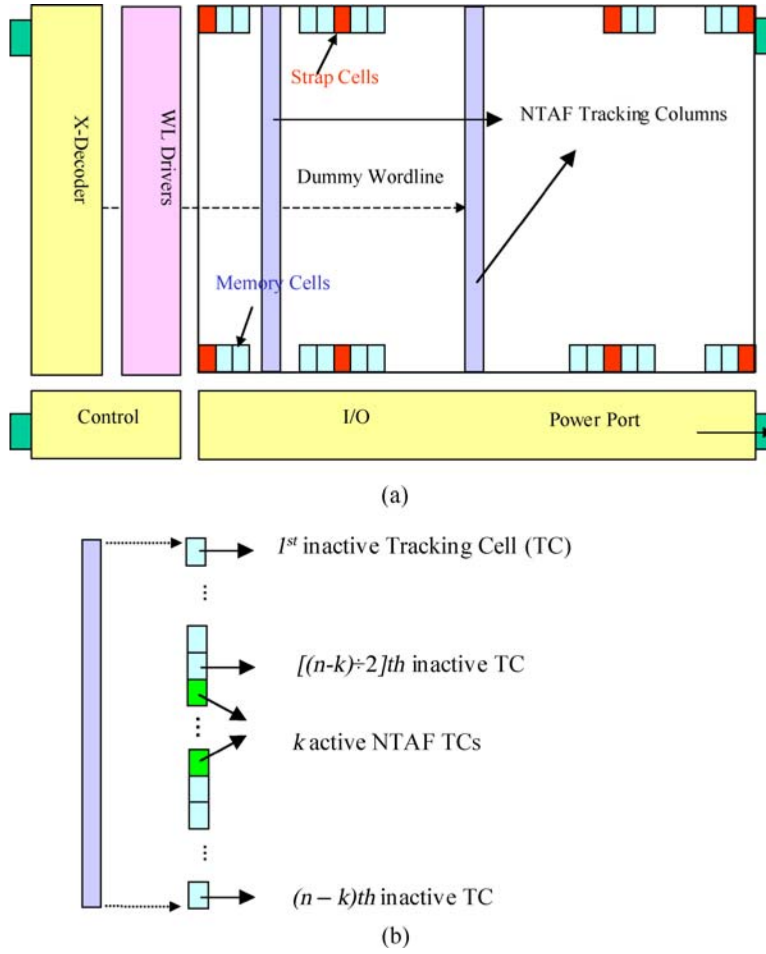

Figure 5. (a) NTAF architecture (b) NTAF tracking column.

ΔI_{CELL} is covered. As a smaller $\Delta V_{\text{TYP-TAIL}}$ is targeted, a smaller ΔI_{CELL} can be tolerated in correctly sensing the tail bit.

$$\Delta V_{\text{TYP-TAIL}} = \Delta I_{\text{CELL}} \times T \tag{3}$$

where T is the width of wordline pulse or the delay that enables the sense amplifier. The bitline capacitance is normalized to unity.

T is determined by the voltage swing on the dummy bitline. The requirement of high speed leave little room for further timing relaxation, so the accuracy of tracking of the bitline voltage as well as the cell current coverage, becomes critical.

The capacitance-ratio tracking scheme activates only one tracking cell ($k = 1$), while the current-ratio scheme activates numerous tracking cells ($k > 1$) simultaneously.

The minimum cell current I_{SENSE}, which can be sensed correctly, varies with I_{TRACK}.

$$I_{\text{SENSE}} = I_{\text{TRACK}} - \Delta I_{\text{CELL}} \tag{4}$$

That is, a large I_{TRACK} leads to fast sensing timing but small cell current coverage. However, a small I_{TRACK} leads to large cell current coverage but slow sensing time. Table 1 presents some examples.

Table 1. Tail-bit sensing of 6T-SRAM IP.

Case	I_{TYP} (μA)	I_{TAIL} (μA)	I_{TRACK} (μA)	I_{SENSE} (μA)	Tail-bit sensing
$I_{\text{TRACK}} = I_{\text{TYP}}$	79.5	59.9	79.5	59.9	Pass
$I_{\text{TRACK}} > I_{\text{TYP}}$	79.5	59.9	85.6	64.4	Fail
$I_{\text{TRACK}} < I_{\text{TYP}}$	79.5	59.9	73.6	55.4	Pass

The fluctuations in the cell current of the tracking cells raise a new DFM problem. Combining (2) and (4) yields,

$$I_{\mathrm{SENSE}} = I_{\mathrm{TAIL}} + (I_{\mathrm{TRACK}} - I_{\mathrm{TYP}}) \tag{5}$$

with respect to the nature of semiconductor manufacturing process, a tracking cell can have a cell current even at the opposite end of the distribution to the tail bit. This situation is overcome by simultaneously activating a sufficiently large number of tracking cells. Consequently, the current-ratio scheme can more accurately track the mean cell current of a given memory cell array, and exhibits better die-to-die or lot-to-lot tracking consistency than the capacitance ratio scheme.

In this NTAF architecture, the current ratio method is adopted in the tracking columns with the proposed NTAF tracking cells. The method dynamically tracks the severest cell current degradation associated with power noise and the least favored ground-substrate conditions for each cycle, rather than adding fixed timing margin to sensing time for all cycles. Accordingly, noise immunity and manufacturing yield can be increased by accurately tracking the degradation of the cell current caused by pattern-dependent power and substrate noise in a system.

3. Tracking Cells in NTAF Architecture

3.1. Tracking Cells in NTAF Architecture

The conventional tracking cells for 6T-SRAM are typically featured with similar cell current as that of nominal memory cells but smaller areas. The tracking cells in Fig. 6(a) has smaller area overhead than any other tracking cells, but cannot reflect the degradation in the cell current because of the voltage bump inside a SRAM cell during a read operation, as presented in Fig. 7. Another popular tracking cell, as shown in Fig. 6(b) [18], is larger than that shown in Fig. 6(a) but can reflect the voltage bump during a read cycle. It is smaller than a nominal memory cell and because it removes the

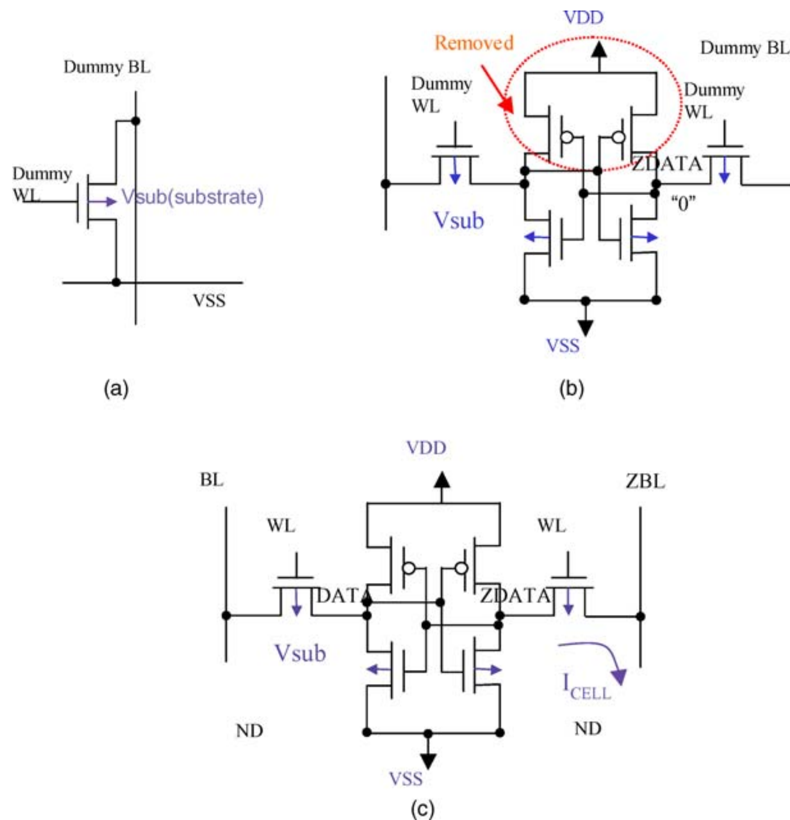

Figure 6. Conventional (a) one-transistor tracking cell, (b) removed-PMOS tracking cell, [18], and (c) nominal memory cell for 6T-SRAM.

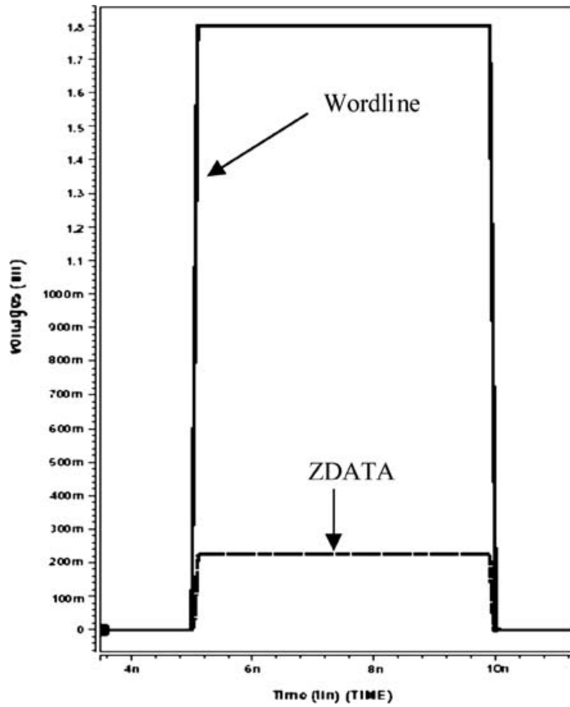

Figure 7. Voltage bump at “ZDATA” in a 6T-SRAM cell.

PMOS transistors. Unfortunately, because the pattern density and layout style of layer poly and diffusion is different from that of nominal memory cells, any misalignment and etching effects of these two layers during manufacturing enlarges the difference between the cell current of this tracking cell and that of nominal memory cells. Also, an extra operational phase is required to pre-store the logic “0” at the node “ZDATA” in this tracking cell before each read operation is begun.

The proposed tracking cells used in NTAF architecture are implemented using a pair of diode-connected native-NMOS transistors on both sides of a modified 6T-SRAM cell, or one on one side of a replica ROM cell, as depicted in Fig. 8. The poly and active regions of the modified SRAM and replica ROM cells have exactly the same layout pattern as the nominal cells. Therefore, any process variation results in similar cell current variation for both tracking cells and nominal memories cells. The wire “a”, which is implemented only in metal-1 layer, of the proposed tracking cell for 6T-SRAM connects the gates of transistor $P0$ and $N0$ to the supply voltage (VDD). This set logic “0” is stored at the node “ZDATA” in the tracking cell. This circuit and layout design avoids the need for an extra operational phase to pre-store the data in tracking cells for

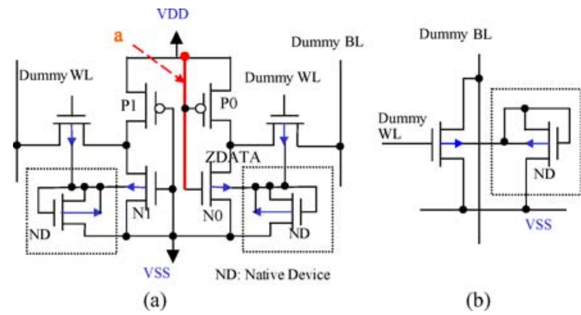

Figure 8. NTAF tracking cells for (a) 6T-SRAM and (b) ROM.

high-speed applications. It also does not change the electrical parameters in the device level (transistors) and maintain the DFM capability.

Therefore, the proposed tracking cells with specific ground line patterns in NTAF tracking columns completely reflect the cell current degradation effects of the voltage bump both inside the SRAM/ROM cell and on the array ground line. The layout style minimizes the cell current mismatch between the nominal memory cells and the tracking cells.

3.2. Tracking Cells vs. Power and Substrate Noise

Any voltage difference between its ground line and local substrate in a nominal memory cell affects its cell current as plotted in Fig. 9. The higher resistance in the substrate than in the metal wires and the different paths of noise propagation cause the substrate noise exhibit a phase delay that varies with location in the memory cell array. For the memory cells that have unequal distances to the strap cells on their left and right sides, the ground noise couples through the substrate ties of strap cells causes various mixing in those cells.

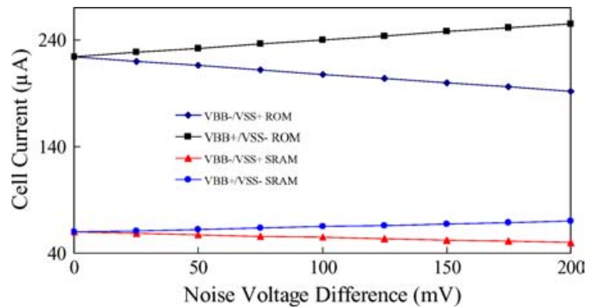

Figure 9. Cell current (tail bit) fluctuations due to positive (VBB+/VSS−) and negative (VBB−/VSS+) bulk-source voltage difference on 6T-SRAM and ROM cells.

The location-dependent phase shift in the noise and the accompanying mixing effects induce various bulk-source voltage differences of the NMOS transistors in the memory cells, causing their cell currents to fluctuate under the influence of the body effect. This variation in cell current due to this differential noise voltage is presented not only in nominal memory cells but also in tracking cells. This effect enlarges the mismatch between the cell currents of the tracking cells and those of the nominal memory cells. The accuracy of tracking in configurable memories is degraded and the manufacturing yields suffer, as discussed in the previous section.

In conventional tracking schemes, substrate ties are at the side of tracking cells, which are typically on the edge of a memory cell array. This layout style has the advantage on superior latch-up prevention and zero differential voltage between the ground line and local substrate of the tracking cells. However, it cannot tolerate a cell current degradation due to a positive difference between the noise voltage of the ground line and that of the substrate in nominal memory cells.

Separating the substrate bias from noisy ground lines is attractive for the reducing substrate noise in many applications. It tends to make the power lines and substrate bias less relevant. However, the difference between the voltages is unpredictable for embedded memories in various SoCs, since the ground and substrate noise varies with data pattern. Variations in the bulk-source voltage difference thus widen the distribution of cell current, although such variations may not change the mean cell current of the memory cell array. Therefore, separated substrate bias is not preferred in memory cell arrays.

The MOS-diode in NTAF tracking cells can pass the negative part of the ground noise but block the positive part in the local substrate. The positive part of the substrate noise is filtered out near the diode area. This circuit ensures that the local substrate bias does not exceed the local ground voltage near the tracking cells (see Fig. 10, for 200 mV noise). Therefore, NTAF tracking cells effectively track the cell current degradation in those memory cells with negative bulk-source voltage difference.

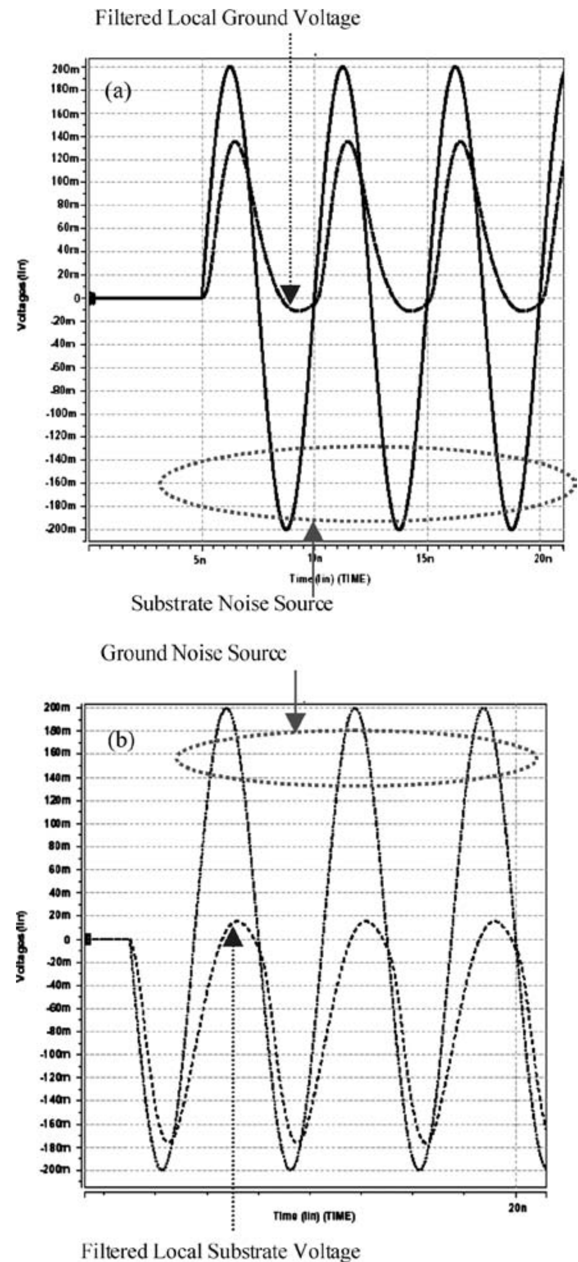

Figure 10. Filtering effects in NTAF tracking cells with noise from (a) substrate and (b) ground.

4. NTAF Architecture vs. Conventional Configurable Memories

As discussed earlier, the external and self-generated power and substrate noise, and their location-dependent voltage differences in embedded memories result in a wide cell current distribution. The degradation in cell current, particularly in the tail bits, causes sensing failure when the conventional bitline tracking scheme employed.

Table 2 gives examples for a 256 Kb 6T-SRAM SIP operating with a ground or substrate noise of 100 mV,

Table 2. Tail-bit sensing in a conventional 256 Kb embedded 6T-SRAM SIP.

Case	I_{TRACK} (μA)	I_{TAIL} (μA)	$I_{\text{TRACK-NOISE}}$ (μA)	$I_{\text{SENSE-NOISE}}$ (μA)	Tail-bit sensing
VSS+	79.5	51.6	69.7	52.5	Fail
VSS−	79.5	68.2	89.6	67.4	Pass
VBB+	79.5	61.6	81.6	61.5	Pass
VBB−	79.5	58.1	77.5	58.4	Fail
VBB+/VSS−	79.5	64.9	85.6	64.5	Pass
VBB−/VSS+	79.5	54.8	73.6	55.4	Fail

using conventional bitline tracking. The tracking cells, acting as a static current source, do not seem to handle the noise very well. Consequently, the tail bit is not sensed correctly. Equation (7) clearly demonstrates that $I_{\text{TRACK-NOISE}}$ must be actively reduced further, so as to lower $I_{\text{SENSE-NOISE}}$ and extend the cell current coverage.

Under extreme condition, in which the tracking cells encounter the most negative voltage difference between the ground and substrate noise while the tail bits encounter the most positive voltage difference, separating the substrate bias would worsen immunity to the power and substrate noise.

Table 3 presents examples of an 256 Kb embedded 6T-SRAM silicon IP using the NTAF architecture and operating with ground and/or substrate noise of 100 mV with an area overhead of 0.35%. The examples can be compared to those in Table 2. The self-generated ground bounce of 114 mV was observed in the middle of the memory cell array with 512 bit cells per row. The proposed NTAF architecture provides more accurate timing relaxation and increases the coverage of the cell current variation.

The worst memory cell current degradation is always tracked in the NTAF architecture at any memory size; the tradeoff is a decline in speed. The maximum memory size is limited by the specifications of the design target and the nature of manufacturing technology. The tolerable noise range is not limited by the NTAF technique, itself, but by the allowed speed degradation of embedded memories in a given system. The two NTAF tracking columns represents the only area overhead, so a larger number of columns in the memory cell array, the smaller the area overhead of the NTAF architecture.

Table 3. Tail-bit sensing using NTAF in a 256 Kb embedded 6T-SRAM SIP.

Case	I_{TRACK} (μA)	I_{TAIL} (μA)	$I_{\text{TRACK-NOISE}}$ (μA)	$I_{\text{SENSE-NOISE}}$ (μA)	Tail-bit sensing
VSS+	79.5	51.6	59.6	44.9	Pass
VSS−	79.5	68.2	78.1	58.8	Pass
VBB+	79.5	61.6	69.3	52.2	Pass
VBB−	79.5	58.1	68.1	51.3	Pass
VBB+/VSS−	79.5	64.9	74.2	55.9	Pass
VBB−/VSS+	79.5	54.8	63.5	47.8	Pass

5. Conclusion

This investigation has studied the effects of supply and substrate noise on configurable SRAM and ROM. Both self-generated and external supply and substrate noise influence tail-bit sensing. The ground line routing in the memory cell array is important for minimizing the variations in the cell current. NTAF architecture was developed to track the noise-induced degradation of the cell current under conditions of supply and substrate. It provides timing relaxation necessary for correct sensing, and does not require that a large fixed timing margin be added to ensure wide coverage of unpredictable system noise. This architecture achieves better noise immunity and DFM capability than conventional configurable embedded memories.

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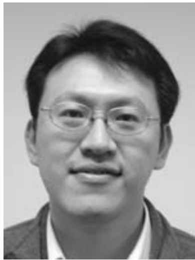

Meng-Fan Chang received the B.S. degree in electrical engineering from National Cheng-Kung University in 1991. He received the M.S. degree in electrical engineering from The Pennsylvanian State University, University Park, PA, in 1996. He is currently working toward the Ph.D. degree at the Institute of Electronic Engineering, National Chiao Tung University, Hsin-Chu, Taiwan.

During 1991–1993, he joined Army of Taiwan as second lieutenant in electronic communication. From 1993 to 1994, he designed motherboards in ABIT Computer Corp., Taipei, Taiwan. During 1996–1997, he designed SRAM/ROM compilers in Mentor Graphics Corp., Warren, New Jersey. From 1997 to 2001, he designed SRAM and managed the IP Validation Program in Design Service Division (DSD) of TSMC, Hsin-Chu, Taiwan. Since 2001, he jointed Intellectual Property Library Company (IPLib), Hsin-Chu, Taiwan. He is in charge of Silicon-IP Division. He is engaged in the research and development of embedded Flash, SRAM/ROM compilers, flat-cell mask ROM and mixed-signal IPs.

His research interest included embedded memories, low-power circuit, integration issues of silicon-IP in SoC, CMOS RF and LTCC RF circuit.

mfchang.ee89g@nctu.edu.tw

Kuei Ann Wen was born in Keelung, Taiwan, R.O. China in 1961. She received the B.E.E., M.E.E. and Ph.D. degrees from the Dept. of Electrical and Computer Enginerring a National Cheng-Kung University, Taiwan, R.O. China in 1983, 1985 and 1988, respectively. She is currently a professor in the Dept. of EE at national Chiao-Tung University, Taiwan, R.O. China. At the present time, she is also involved in several research projects from Wireless Communication Consortium (http://wireless.eic.nctu.edu.tw) and Academic Center of Excellence (http://www.eic.nctu.edu.tw/ace/), which is under supervision of Dept. of Higher Education, Council of Academic Reviewer & Evaluation of R.O. China. Dr. Kuei-Ann Wen’s interests are in the areas of wireless communication system, RF circuit design, video signal processing & transmission.