Code-pattern insensitive embedded ROMs using dynamic bitline shielding technique

M.-F. Chang, L.-Y. Chiou and K.-A. Wen

A dynamic bitline shielding (DBS) technique is proposed for high-speed via-programming ROMs, to eliminate code-pattern-dependent crosstalk-induced read failure (CIRF) and increase code-pattern coverage. Fabricated 256 Kb conventional and DBS ROMs demonstrated that the DBS technique can eliminate the CIRF and operate with a small sensing margin.

Introduction: Via-programming read only memories (ROMs) are commonly embedded in SoCs to store programs and data with short manufacturing time after code modification. Unlike other memories (diffusion-ROM, SRAM and DRAM), various contents/code-patterns cause large fluctuations in bitline capacitance and coupling noise in via-programming ROMs. In high-speed ROMs, the wordline pulse width (T_{WL}) is short, and the sensing margin becomes small and vulnerable to noise. The code-pattern-dependent crosstalk-induced read failure (CIRF) limits the coverage of applicable code-patterns for via-programming ROMs. Previous reports [1–4] have improved the performance of ROMs, but have not addressed the issue with respect to CIRF. To the authors' knowledge, this work is the first to investigate code-pattern-dependent CIRF, and we present a solution on a circuit for via-programming ROMs.

Crosstalk-induced read failure: Failure to sense 1 is the major shortcoming of the crosstalk effects for high-speed via-programming ROMs. In typical synchronous NOR-type via-programming ROMs, a bit cell with a via layer that connects its transistor to its bitline stores a 0 (0-cell), and a bit cell without such a layer stores a 1 (1-cell). All bitlines are precharged to a targeted voltage, V_{PRE}, prior to the sensing phase of a cycle. In the sensing phase, a bitline is discharged to develop a voltage swing (V_0) for reading a 0-cell or remains at V_{PRE}, for reading a 1-cell. A reference voltage, V_{REF}, is chosen between $V_{PRE}-V_0$ and V_{PRE} to differentiate between a 0-cell and a 1-cell. If a coupled noise drop (V_X) on a bitline exceeds $V_{PRE}-V_{REF}$, read 1 failure may occur in a ROM.

Coupling capacitance between bitlines (C_C), intrinsic bitline load (C_{BL}) and V_0 on neighbouring bitlines are the key parameters that determined CIRF, as derived in (1). The unselected bitlines BL[$j-1$] and BL[$j+1$], which are the neighbouring bitlines of the selected one BL[j], act as the aggressors in crosstalk effects. $C_{C[j-1]}/C_{C[j]}$ is the coupling capacitance between BL[j] and BL[$j-1$]/BL[$j+1$]. Unfortunately, C_C increases as the technology node shrinks:

$$V_X = V_{0[j-1]} \times \frac{C_{C[j-1]}}{C_{BL[j]} + C_{C[j-1]}} + V_{0[j+1]} \times \frac{C_{C[j]}}{C_{BL[j]} + C_{C[j]}} \quad (1)$$

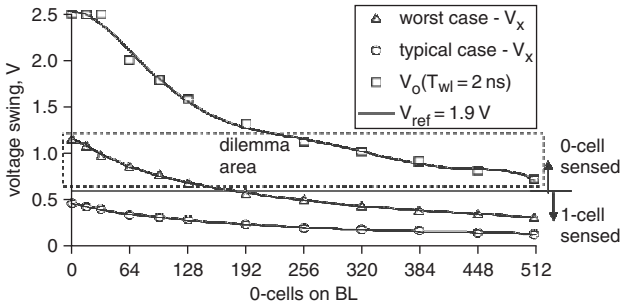

Fig. 1 *Simulated V_X and V_0 against number of 0-cells on bitline across various code-patterns*

C_{BL} and V_0 on a bitline are code-pattern dependent in via-programming ROMs [4]. Accordingly, V_X also depends on the code-pattern of a victim bitline and its neighbouring bitlines. Fig. 1 plots the simulated V_0 and V_X on a bitline with 512 cells; the supply voltage (V_{DD}) is 2.5 V and $V_{PRE}=V_{DD}$. The V_0 ranges from a full swing of V_{PRE} for a bitline with a light load to a few hundred mV for a bitline with a heavy load. The neighbouring bitlines have small V_0 in the typical case (high probability), which have 220 to 292 0-cells. The neighbouring bitlines in the worst case have a light load and $V=V_{PRE}$. Regardless of the code-pattern of a victim bitline, sensing is accurate when $V_{REF}=1.9$ V with its neighbouring bitlines in a typical case on. However, the maximum V_X in the worst case exceeds the smallest V_0 of a selected bitline (see the dilemma area in Fig. 1). Accordingly, no V_{REF} supports correct sensing across all possible code-patterns.

Therefore, a bitline with a small intrinsic load, a large coupling capacitance and a large V_0 on its neighbouring bitlines suffers a large V_X.

Dynamic bitline shielding technique: The coupling capacitance and the fluctuation in the intrinsic load on bitlines across various code-patterns are inevitable in via-programming ROMs. Restricting the voltage swing of the aggressors can reduce the coupled voltage on the victim bitlines. The dynamic bitline shielding (DBS) technique is proposed for ROMs to eliminate the coupling noise source and prevent CIRF.

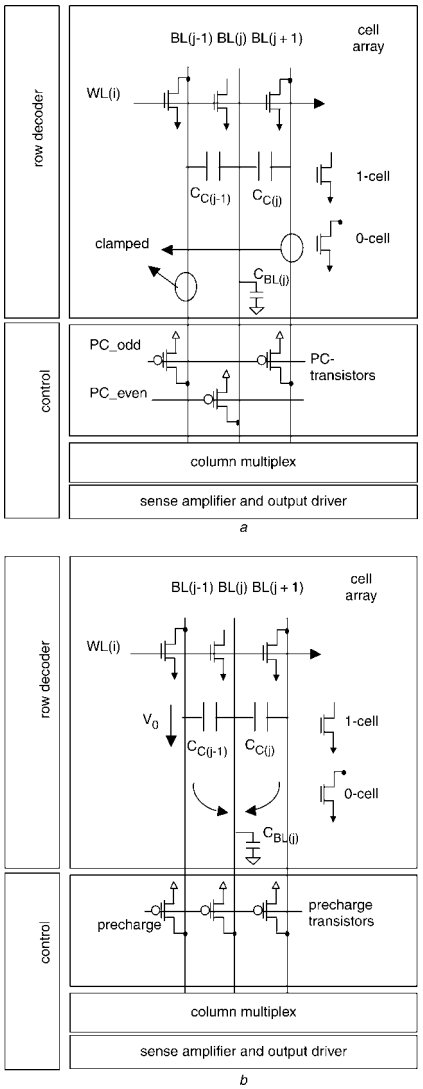

Fig. 2 *Simplified architecture of DBS and conventional ROMs*
a DBS ROMs *b* Conventional ROMs

In both the DBS and conventional ROMs, as displayed in Fig. 2, all bitlines are precharged using precharge-clamped (PC) transistors and precharge-transistors prior to the sensing phase, respectively. However, the behaviours of DBS ROMs in the sensing phase differ from that of conventional ROMs.

In DBS ROMs, half of the bitlines, including the neighbouring bitlines (both left and right sides) of the selected bitlines, are clamped to V_{PRE} during the sensing phase. These neighbouring bitlines, clamped by the PC-transistors, shield the selected bitlines and are dynamically specified according to the input address of each cycle. In conventional ROMs, the

neighbouring bitlines are not clamped and are in the unselected reading state. If the bitline BL[j] is selected, then the PC_odd signal enables the clamping function on odd bitlines (BL[$j \pm 1$], and so on). This clamping scheme results in no voltage swing on those odd bitlines, during the sensing phase. However, the other unselected even bitlines (i.e. BL[$j \pm 2$] and so on) still exhibit a voltage swing, as in conventional ROMs if 0-cells are activated during the sensing phase. This clamping behaviour eliminates the coupling noise source for the selected bitlines, and thus eradicates the coupled voltage drop on selected bitlines and CIRF. An alternative technique, which involves clamping only the nearest neighbouring bitlines of the selected bitlines can be implemented, but requires a more complex control scheme and larger area overhead.

The signals for controlling PC-transistors are encoded with the least significant bit of the column addresses to control separately the odd and even bitlines. However, the number of PC-transistors in DBS ROMs is the same as the number of precharge-transistors in conventional ROMs. Accordingly, no area overhead is associated with the PC-transistors, and the control block has a negligible area overhead for generating the PC_odd and PC_even signals.

In summary, a bitline during the sensing phase in DBS ROMs is in one of the three states: selected reading, unselected reading or clamped state. In the clamped state, the bitlines that neighbour the under-access bitline enter the crosstalk-elimination mode. The clamped bitlines (even or odd ones) are dynamically selected according to the input address.

Experimental results: A testchip with 256 Kb DBS and conventional ROMs were designed and fabricated using a 0.25 μm 1P5M CMOS logic process. The CIRF of these fabricated ROMs was analysed using two adjustable V_{REF} values, 2.15 and 2.35 V, at a supply voltage of 2.5 V.

A designated code-pattern, X-pattern, was applied to the fabricated ROMs to analyse the CIRF with various crosstalk effects. Nine bitline loads (0-cells) on the aggressor bitlines and the victim bitlines were implemented in the X-pattern to explore the minimum, typical and maximum C_{BL} and V_0 on bitlines. Table 1 presents the measured results concerning the fabricated ROMs. The conventional ROM failed the X1, X4 and X7–X9 at $V_{REF} = 2.35$ V, or the X1, X7 and X8 at $V_{REF} = 2.15$ V. The DBS ROM passed all patterns for both V_{REF} values. These measurements demonstrate that DBS eliminated the CIRF and provided room for a ROM to have a higher V_{REF} value or smaller sensing margin than conventional ROMs.

Table 1: Measurement results of fabricated ROMs

ROM type			Conventional		DBS	
Capacity, bits			256 Kb		256 Kb	
Area, mm^2			0.53		0.53	
X-pattern	0-cells		V_{REF} (V) at $V_{DD} = 2.5$ V			
	Aggressor	Victim	2.15	2.35	2.15	2.35
X1	512	0	Fail	Fail	Pass	Pass
X2	512	256	Pass	Pass	Pass	Pass
X3	512	511	Pass	Pass	Pass	Pass
X4	256	0	Pass	Fail	Pass	Pass
X5	256	256	Pass	Pass	Pass	Pass
X6	256	511	Pass	Pass	Pass	Pass
X7	1	0	Fail	Fail	Pass	Pass
X8	1	256	Fail	Fail	Pass	Pass
X9	1	511	Pass	Fail	Pass	Pass

The area and speed performance of the 256 Kb DBS ROM is the same as that of the conventional ROM. The power consumed by the X-pattern of the 256 Kb DBS ROM is 6.8% greater than that consumed by the conventional ROM.

Conclusion: The code-pattern-dependent CIRF in via-programming ROMs was eliminated by removing the coupling noise source in DBS. The fabricated 256 Kb conventional and DBS ROMs demonstrated the effectiveness of DBS in eliminating CIRF under both typical and extreme code-patterns with a small sensing margin.

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References

1 Chang, C.-R., Wang, J.-S., and Yang, C.-H.: 'Low-power and high-speed ROM modules for ASIC applications', *IEEE J. Solid-State Circuits*, **36**, 2001, pp. 1516–1523
2 Yang, B.D., and Kim, L.S.: 'Low-power charge sharing ROM using dummy bit lines', *Electron. Lett.*, **39**, 2003, pp. 1041–1042
3 Chang, M.-F., Wen, K.-A., and Kwai, D.-M.: 'Supply and substrate noise tolerance using dynamic tracking clusters in configurable memory designs'. Proc. IEEE Int. Symp. Quality Electronic Design, March 2004, pp. 297–302
4 Chang, M.-F., Chiou, L.-Y., and Wen, K.-A.: 'A low supply noise content sensitive ROM architecture for SoC'. Proc. IEEE Asia-Pacific Conf. on Circuits and Systems, December 2004, pp. 1021–1024