2012 International Conference on Solid State Devices and Materials Science

Nearly Dislocation-free Ge/Si Heterostructures by Using Nanoscale Epitaxial Growth Method

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Abstract

The selective growth of germanium into nanoscale trenches on silicon substrates was investigated. These nanoscale trenches—the smallest size of which was 50 nm—were fabricated using the state-of-the-art shallow trench isolation technique. The quality of the Ge films was evaluated using transmission electron microscopy. It was found that the formation of threading dislocations (TDs) was effectively suppressed when using this deposition technique. It was considered that for the Ge grown in nanoscale Si areas (e.g., several tens of nanometers), the TDs were readily removed during cyclic thermal annealing, predominantly because their gliding distance to the SiO_2 sidewalls was very short. Therefore, nanoscale epitaxial growth technology can be used to deposit Ge films on lattice-mismatched Si substrates with a reduced defect density.

Keywords: germanium; dislocations; nano treches; epitaxy.

1. Introduction

Because of higher mobility of its carriers and its narrower band gap relative to that of silicon (Si) [1], germanium (Ge) is now emerging as a viable candidate to supplement Si in CMOS device and 1.3–1.55

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µm optoelectronic applications   [2]; therefore, is it essential to develop new methods for the heteroepitaxial growth of Ge on Si. This growth process is not straightforward, however, because the large lattice mismatch (4%) between Ge and Si limits the quality of the epitaxially grown layers. After reaching a critical thickness, the Ge layer usually contains many misfit and threading dislocations (TDs), making it unusable for any practical applications. Although several techniques have been proposed to alleviate this problem [3], the TD densities in the grown Ge layers remain too high for device applications. Using patterned growth and cyclic thermal annealing (CTA), the dislocation density in Ge can be reduced to ca. $10^6/cm^2$ as a result of thermally induced dislocation gliding [4]. Any further reduction remains a big challenge because the dislocations cannot glide over the long distances in large patterns. Based on the selective growth of Ge in narrow, deep SiO_2 trenches having sizes of several hundreds of nanometers, it was recently reported that the generated TDs in Ge could be effectively trapped to the sidewalls of SiO_2 through an aspect ratio trapping (ART) mechanism [5]; the resulting top area of Ge was claimed to be dislocation-free. In that paper, the authors considered that the TDs formed at a 45° angle to the underlying Si(001) surface. Thus, for trenches having an aspect ratio of greater than unity, the TDs will meet the SiO_2 sidewalls and terminate there when they penetrate up in the Ge film. In such as a case, the surface of the Ge would be dislocation-free, with TDs being confined only to the bottom of the trenches.

In this study, following the similar process scheme, we selectively grew Ge layers in SiO_2 trenches having dimensions as low as 50 nm. After CTA, we found that the formation of TDs in the Ge layers grown in these ultra-small trenches was further suppressed. Our results are slightly different from those expected for the ART mechanism [5], where there are still a few TDs at the bottom of Ge layer. In our case, the dislocations at the bottom of trenches were also suppressed—quite advantageous for the fabrication of Si-based Ge-channel devices, such as Ge FinFET devices.

2. Experimental

The state-of-the-art shallow trench isolation (STI) technique was used to fabricate the patterns on p-type (100)-oriented Si wafers having a resistivity of 15–25 Ω•cm. The Si area was recessed using reactive ion etching (RIE) to form trenches for selective epitaxial growth (SEG) of Ge. The trenches were aligned along the [110] direction; they were formed with dimensions of 50 nm× 600 nm and 320 nm×1.4µm, respectively. The narrowest width of the trenches was 50 nm, a reasonable dimension for 22-nm technology nodes. The finished 50-nm trenches are displayed in Fig. 1. After trench fabrication, the Si substrates were subjected to standard wet cleaning and dipping in
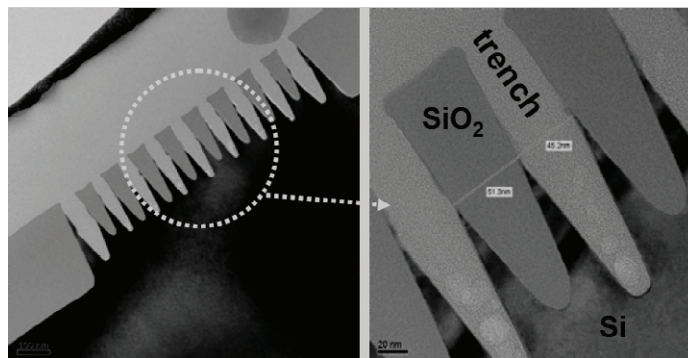

Fig.1 Cross-sectional TEM images of the 50-nm SiO_2 trenches fabricated using the STI process.

dilute HF for 30 s to remove the native oxide on the exposed Si surface; they were then loaded into an ultrahigh-vacuum chemical vapor deposition (UHV-CVD) chamber. After thermal pre-baking at 900 °C for 10 min, Ge layers having a thickness of 150–200 nm were selectively grown inside the trenches at 400 °C under a germane flow rate of 10 sccm and a growth pressure of 0.5 mtorr. Finally, the wafers were in situ annealed over three cycles; each cycle included high temperature annealing at 900 °C for 5 min and low temperature annealing at 400 °C for 5 min. Because the thermal expansion coefficients of Ge and Si are different, annealing can generate extra thermal stress that can cause movement of the TDs in the grown Ge layer. For CTA, an increase in the number of cycles will result in greater dislocation reduction [4,7]. In this study, considering the trade-off between the thermal stress effect and the experimental efficiency, three-cycle annealing was adopted.

3. Results and discussion

Figure 2 presents cross-sectional transmission electron microscopy (XTEM) and plan-view TEM images of Ge grown in 50-nm trenches. In these three figures, no TDs are evident in the Ge, even at its bottom; only misfit systems can annihilate or combine to form a new one; (d) threading segments from different sources on intersecting slip systems can annihilate or combine to form a new one through gliding, climbing, or a combination of the two. Because Ge and Si have a 4% lattice mismatch, the original TD density should be same for any pattern size. Here, the major factor determining the TD density should be the propagation distance. In the nanoscale patterns, many of the dislocations could readily glide to the sidewalls of the trenches with a low probability of being blocked or combing to form a sessile dislocation because of the very small propagation length; in contrast, dislocations in larger patterns had greater difficulty arriving at the sidewalls and, therefore, they tended to become trapped in the Ge film. Additionally, although the trench was aligned along the [110] direction and had a length of 600 nm, the TD
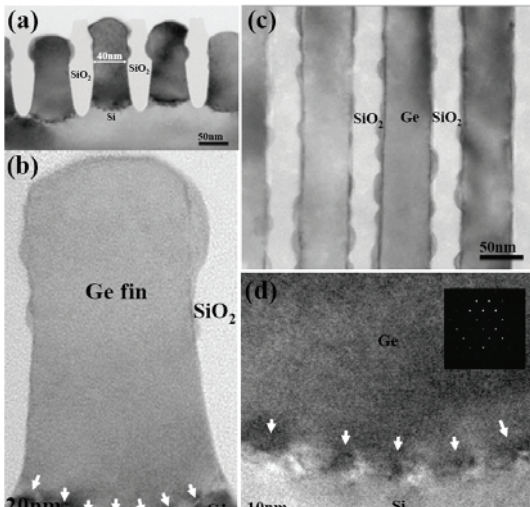

FIG. 2. (a) Cross-sectional TEM image of Ge in trenches having a width of 50 nm; (b) magnified cross-sectional TEM image. (c) Plan-view TEM image; (d) magnified cross-sectional TEM image. The MDs at the Ge/Si interface are indicated by arrows.
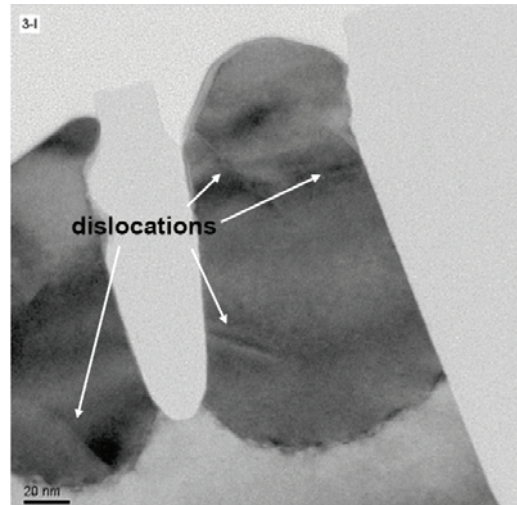
FIG. 3. Cross-sectional TEM image of Ge in 50-nm trenches for the sample prepared without CTA

density still remained low. Because the TDs in the $(1\bar{1}1)$ and (111) slip planes along the width direction of the trench (i.e. [110] direction) have glided to the SiO_2 sidewalls, the interactions between TDs from different sources on intersecting slip systems [e.g. between $(1\bar{1}1)$ and $(1\bar{1}1)$ slip planes] are suppressed. This case facilitates the annihilation of TDs on the same slip plane or on the parallel slip systems (e.g. the (b) and (c) annihilation processes of TDs described above) to work better along the direction of the length of the trench. As a result, the TD density in 50nm trenches can still be reduced, albeit the length of trenches is long.
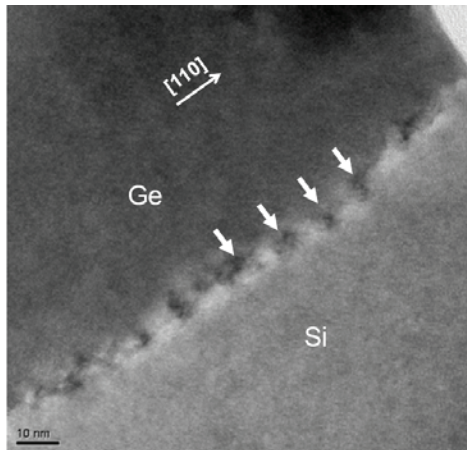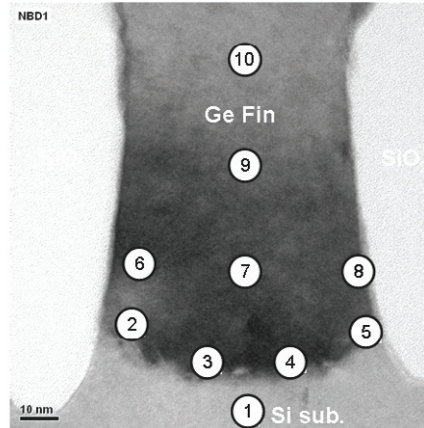

FIG. 4. Cross-sectional TEM image of Ge in 50-nm trenches, recorded along the direction of the length of the trenches. MDs are clearly evident at the Ge/Si interface (some are indicated by arrows).

Point	Lattice Constant
Ge	5.646 Å
10	5.623 Å
9	5.645 Å
8	5.633 Å
7	5.630 Å
6	5.636 Å
5	5.430 Å
4	5.440 Å
3	5.560 Å
2	5.461 Å
1	5.431 Å
Si	5.431 Å

FIG. 5. Nano-beam diffraction analysis of Ge fin. The radius of electron beam is ca. 10 nm

Recent publications [9] suggest that, for SiGe films grown selectively on recessed Si, a decrease in the trench width will cause the strain of the SiGe film to be released preferably through elastic relaxation in the direction of the width of the trench. We found, however, that the strain in our Ge film was released mainly through plastic relaxation in the directions of both the width and the length. In Figures 2(b) and 2(d), uniformly distributed MDs appear at the Ge/Si interface. For comparison, we also present a magnified XTEM image of the 50-nm sample along the direction of the length of the trenches. Similarly, the MDs are clearly observable at the Ge–Si interface in Figure 4. The distances between the MDs in Figures 2(b) and 2(d) are almost the same as that in Figure 4, indicating that the strain in Ge was relaxed biaxially and plastically. This result differs from that reported by Ref. [9]—most likely because we applied a high-temperature CTA process to the Ge layer, causing the Ge layer to relax adequately. In Fig. 5, nano-beam diffraction analysis of TEM showed that the Ge fins were fully relaxed and the lattice constant close to Si surface was Si-rich SiGe alloy, arising from the interaction of surface Si atoms with Ge during CTA process.

4. Conclusions

The hetero-epitaxial growth of Ge into nanoscale trenches on Si substrates was demonstrated. Through mechanisms involving gliding and annihilation, the TDs in nanoscale Ge were readily removed through CTA. In addition, the strain in the Ge films grown using this technique was released mainly through

plastic relaxation in the directions of both the width and length of the trenches. We think that this hetero-structural Ge on Si has potential applications in the integration of Ge-channel devices onto Si CMOS platforms.

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