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Dielectric and electrical properties of $SrTiO_{(3\pm y)}$–$(SiO_2)_x$ thin films

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Abstract
110 nm thick $SrTiO_{(3\pm y)}$–$(SiO_2)_x$ thin films with $x = 0$–0.45 were prepared on $Pt/Ti/SiO_2/Si$ substrates using the chemical solution deposition method and then annealed at temperatures ranging from 600˚C to 900˚C for 1 min. The dielectric and electrical properties of the $SrTiO_{(3\pm y)}$–$(SiO_2)_x$ were obviously affected by the annealing temperature and composition. The dielectric constant of the thin films increased with increasing annealing temperature and decreased with an increase in Si content while the leakage current density decreased with an increase in Si content. The 700˚C annealed $SrTiO_{(3\pm y)}$–$(SiO_2)_x$ thin film with $x = 0.25$ has a suitable dielectric constant of 94.8 and a low leakage current of 1.27×10^{-8} A cm^{-2}. The time-dependent dielectric breakdown curve of the 700˚C and 800˚C annealed $SrTiO_{(3\pm y)}$–$(SiO_2)_x$ films with $x = 0.25$ have an expected lifetime of over 10 years at electric fields higher than 0.6 MV cm^{-1}.

1. Introduction

Dielectrics are used as core components of the two types of devices that represent the heart of the silicon semiconductor industry. One type of device acts as the capacitor dielectric used for the storage of information in dynamic random-access memories (DRAM) and another as the transistor gate dielectric in complementary metal-oxide semiconductor (CMOS) field-effect transistor (FET) logic devices. In both cases, the thickness of the present dielectric is becoming sufficiently thin such that the leakage of currents arising from electron tunnelling through the dielectrics poses a problem. One solution to the problem is the replacement of SiO_2 by an alternative insulator with a higher dielectric constant. Therefore, adopting high-k dielectric materials seems to be an alternative way of providing for good electrical performances, increasing circuit density and reducing the cost as well. The high-k materials for gate dielectric application should satisfy various requirements such as low leakage current, thermodynamic stability on Si, low interface defect density, and so on. Many metal oxides with high dielectric constants from 10 to 80 have been proposed, such as Ta_2O_5 [1], Al_2O_3 [2], $SrTiO_3$ [3], ZrO_2 [4] and HfO_2 [5,6]. However, some problems still remain to be solved for practical applications. In practice, the interfacial reaction still exists between oxide materials and Si. Even in the ideal case of completely eliminating interfacial reaction by using barrier layers, the structure still contains several dielectrics in series, where the lowest capacitance layer will dominate the overall capacitance and also set a limit on the equivalent oxide thickness (t_{ox}) value.

Perovskite-oxide films with high dielectric constants have found various applications such as capacitor dielectrics in integrated circuits, semiconductor memories, gate insulators in submicron integrated circuits, electro-optic devices and electroluminescent displays. Strontium titanate, $SrTiO_3$ (STO) is a cubic, perovskite-type crystal with a lattice constant of 3.905 Å. It is electrically an insulator, and its dielectric constant is as high as 300 at room temperature. The STO thin film is a potential candidate for many electronic applications owing to its large dielectric constant, high breakdown strength and good chemical stability. STO is a possible candidate for replacing silicon dioxide as the gate dielectric material for memory and logic devices [7]. However, STO tends to crystallize at low temperature, which leads to the formation of a polycrystalline

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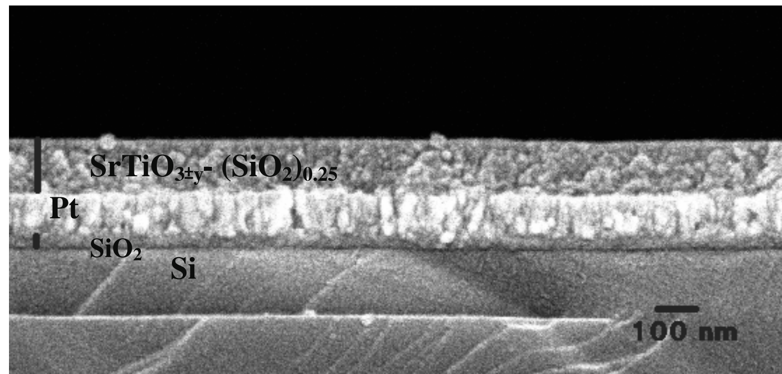

Figure 1. SEM cross-section image of $SrTiO_{(3\pm y)}$–$(SiO_2)_x$ thin film with $x = 0.25$ annealed at 800˚C.

film with crystalline grains serving as high leakage paths and with interface roughness. The retardation of the crystallization temperature has recently been demonstrated in the systems of HfO_2–SiO_2 [8] and ZrO_2–SiO_2 [9]. Such silicate dielectrics are also stable in direct contact with Si and have lower leakage current and better interfacial control in comparison with HfO_2 and ZrO_2. Keeping in mind the requirements of later generations, it is worth investigating the STO with SiO_2 content in order to obtain a better understanding of its electrical and physical properties. In this paper, the electrical and dielectric properties of $SrTiO_{(3\pm y)}$–$(SiO_2)_x$ thin films synthesized using the chemical solution deposition (CSD) method are investigated. The method shows that the leakage current density and dielectric constant of STO thin films are strongly affected by the SiO_2 content.

2. Experimental

The $SrTiO_{(3\pm y)}$–$(SiO_2)_x$ thin films with $x = 0$–0.45 were prepared on Pt/Ti/SiO_2/Si substrates by the CSD method. The precursor solution was made by alkoxide–carboxylate complexes. High purity strontium acetate [$Sr(CH_3COO)_2$], silicon ethoxide [$Si(OC_2H_5)_4$] and titanium ethoxide [$Ti(OC_2H_5)_5$] were selected as starting materials and acetic acid and ethylene glycol as solvent. Strontium acetate was initially dissolved in dehydrated acetic acid and ethylene glycol solution, which was then sealed in a reflux flask under nitrogen gas. The solution was heated to 120˚C for 1 h, and then titanium ethoxide and silicon ethoxide were added to the solution to form a clear and stable precursor solution at 70˚C for 1 h. The mole ratio of strontium to titanium was maintained at 1.0 and that of silicon to strontium was varied from 0 to 0.45. The precursor concentration used in the study was 0.25 mol l^{-1}.

After preparation, the precursor solution was spin-coated on Pt/Ti/SiO_2/Si substrate. The films were spin-coated on the substrates first at 2000 rpm for 10 s and then at 4500 rpm for 30 s. The coated thin film was dried at 150˚C for 10 min, and then 400˚C for 60 min in a conventional furnace to remove organic complex. This step was repeated twice until the desired film thickness was obtained. The thickness of the film obtained in a single spinning was about 50 ± 5 nm. The films with various SiO_2 contents were heat treated in a rapid thermal annealing furnace at temperatures ranging from 600˚C to 900˚C in an oxygen atmosphere for 1 min with a heating rate of 150˚C min^{-1} and cooled with the same rate. The films thickness on the basis of the observation of scanning electron microscopy (SEM) is about 110 ± 10 nm (figure 1). The 50 nm thick Pt top electrodes were then deposited on the films by sputtering through a shadow mask of an area of 9.6×10^{-4} cm^2.

The capacitance of the films was measured at 100 kHz as a function of voltage from negative to positive in a metal–insulator–metal capacitor configuration with an HP 4284A impedance analyser. The dielectric constant of $SrTiO_{(3\pm y)}$–$(SiO_2)_x$ thin films was calculated from the capacitance measured at zero bias voltage. The leakage current characteristics of $SrTiO_{(3\pm y)}$–$(SiO_2)_x$ thin films were measured with a voltage step of 0.01 V and elapsed time of 30 s using an HP 4146C semiconductor parameter analyser. The cross-section and surface morphology of the thin films annealed at various temperatures were observed by transmission electron microscopy (TEM) and a field emission SEM (FESEM, Hitach S4700), respectively. The x-ray diffraction (XRD) patterns were recorded using a Hitachi x-ray diffractmeter with Cu Kα radiation and Cu filter operating at a power level of 30 kV, 20 mA in order to investigate the crystallinity and the phase of $SrTiO_{(3\pm y)}$–$(SiO_2)_x$ thin films. The x-ray photoelectron spectroscopy (XPS) measurements were carried out in a Physical Electronics ESCA PHI 1600 spectrometer at the constant pass energy of 23.5 eV. An Ar^+ ion beam was used to etch the films to obtain their profiles.

3. Results and discussion

Figure 2 shows the XRD patterns of STO thin films annealed at various temperatures in an oxygen atmosphere. It indicates that the STO exhibits diffraction peak (110) for the thin film annealed at above 800˚C. The starting crystalline temperature of STO thin films is about 800˚C. The XRD patterns of $SrTiO_{(3\pm y)}$–$(SiO_2)_x$ thin films with various x values as deposited at 400˚C in air indicates that no diffraction peaks of STO phase exist in the films (not shown here). Figures 3(*a*) and (*b*) show the XRD patterns of $SrTiO_{(3\pm y)}$–$(SiO_2)_x$ thin films with $x = 0.25$ and 0.45 annealed at the temperatures indicated, respectively. The crystalline phase of $SrTiO_{(3\pm y)}$–$(SiO_2)_x$ thin films with $x = 0.25$ and 0.45 appears at annealing temperatures of about 800˚C and 700˚C, respectively. Therefore, the crystalline temperature of $SrTiO_{(3\pm y)}$–$(SiO_2)_x$ thin films decreases with increasing x value.

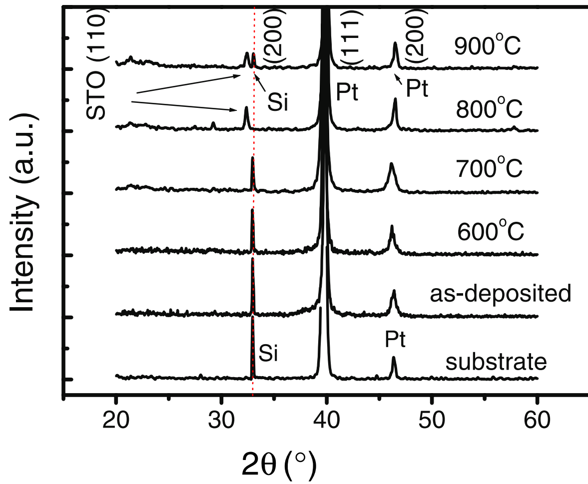

Figure 2. XRD patterns of STO thin films annealed at various temperatures.

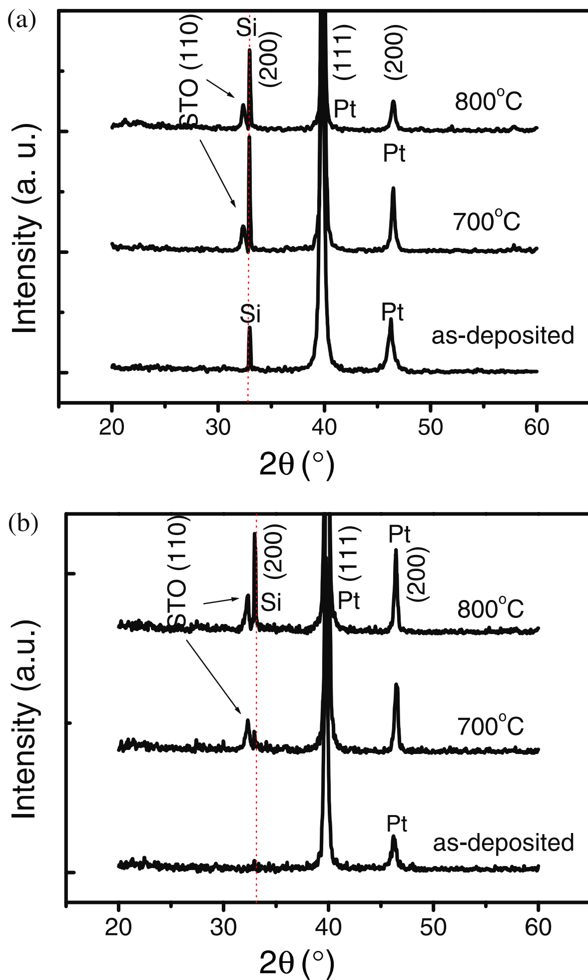

Figure 3. XRD patterns of $SrTiO_{(3\pm y)}$–$(SiO_2)_x$ thin film with (*a*) $x = 0.25$ and (*b*) $x = 0.45$ as-deposited at 400˚C and annealed at the temperatures indicated.

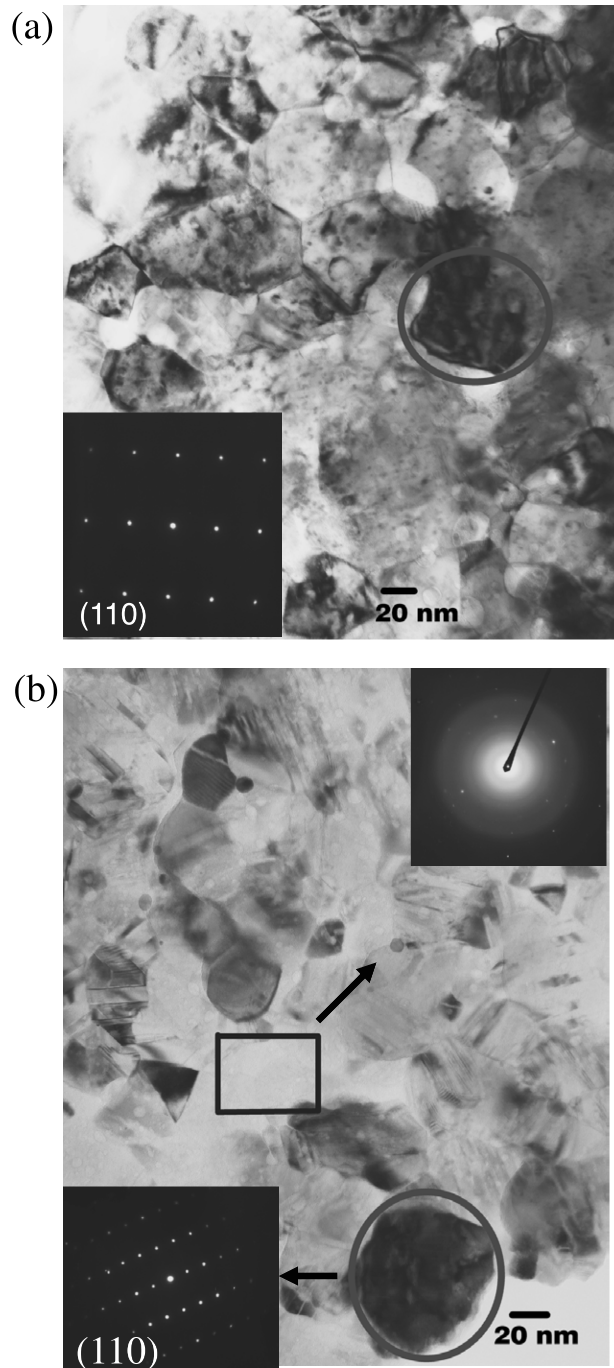

Figure 4. Typical TEM microstructure of the thin films, (*a*) $SrTiO_3$, SAED pattern in inset showing (110) plane of the circle region shown in (*a*), (*b*) $SrTiO_{(3\pm y)}$–$(SiO_2)_x$ thin film with $x = 0.25$ annealed at 800˚C, SAED pattern in inset showing (110) plane of the circle region indicated in (*b*); while another SAED pattern in inset showing amorphous structure of the boxed region indicated in (*b*).

Figure 4 shows the typical TEM microstructure of $SrTiO_3$ and $SrTiO_{(3\pm y)}$–$(SiO_2)_x$ ($x = 0.25$) thin films annealed at 800˚C, indicating the growth of the crystalline grains in both films. The selected area electron diffraction (SAED) patterns in the insets of figures 4(*a*) and (*b*) illustrate that the circled areas in these figures are (110) plane, which are coincident with the XRD patterns shown in figures 2 and 3. There are a smaller number of crystalline grains grown in $SrTiO_{(3\pm y)}$–$(SiO_2)_x$ film than those grown in an STO film at the same annealing temperature. The grain sizes of STO films are larger than those of $SrTiO_{(3\pm y)}$–$(SiO_2)_x$ ($x = 0.25$) films

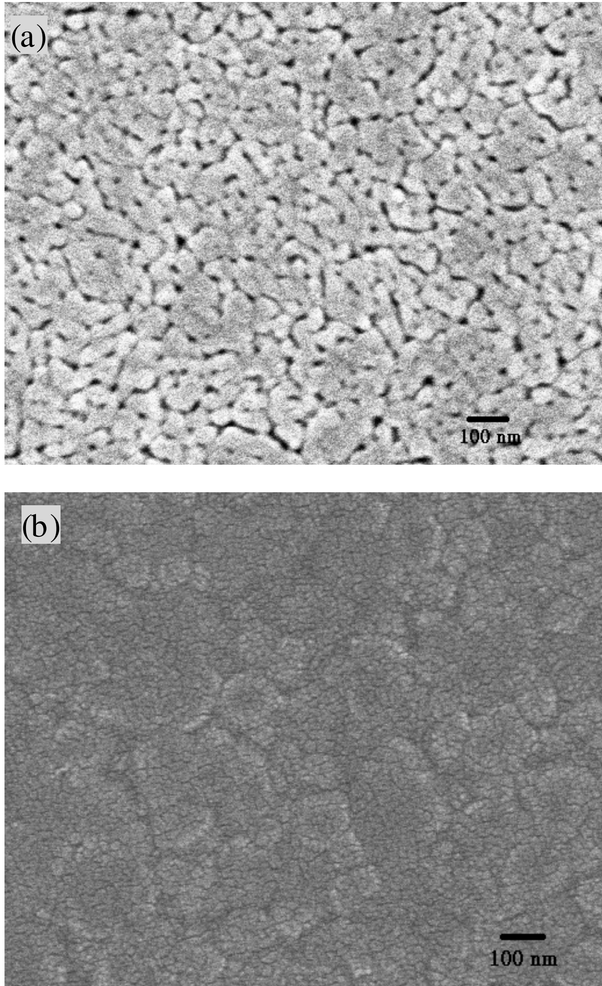

Figure 5. SEM micrographs of surface morphology of (*a*) STO and (*b*) $SrTiO_{(3\pm y)}$–$(SiO_2)_x$ thin films annealed at 800°C.

(figures 4(*a*) and (*b*)). Figure 4(*b*) also shows the coexistence of crystalline and amorphous phases (SAED pattern in the inset of this figure shows square area is amorphous phase) in the $SrTiO_{(3\pm y)}$–$(SiO_2)_x$ thin films. Obviously, the addition of SiO_2 into the films retards their crystallization.

Figures 5(*a*) and (*b*) show the SEM surface images of STO and $SrTiO_{(3\pm y)}$–$(SiO_2)_x$ thin film with $x = 0.25$ annealed at 800°C, indicating that the addition of Si content would depress the growth of the grain size and improve the density of $SrTiO_{(3\pm y)}$–$(SiO_2)_x$ thin film. Surface morphology is an important physical property which may affect the electrical properties of dielectric thin films. The $SrTiO_{(3\pm y)}$–$(SiO_2)_x$ thin films show smoother surfaces than the STO film.

Figure 6 shows the plots of dielectric constant versus x in $SrTiO_{(3\pm y)}$–$(SiO_2)_x$ thin films annealed at various temperatures. The dielectric constant of the $SrTiO_{(3\pm y)}$–$(SiO_2)_x$ thin films decreases with an increase in Si content at the same annealing temperature. However, the dielectric constant increases with increasing annealing temperature owing to the improved crystallinity of the films at higher temperature.

The addition of a low dielectric material, SiO_2, into a higher dielectric matrix material, STO, results in the dielectric

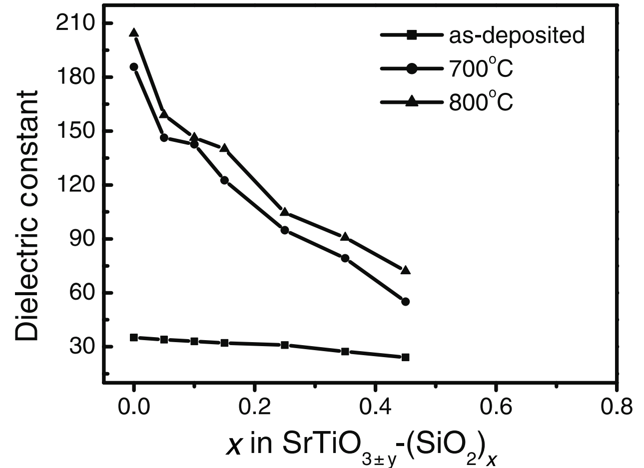

Figure 6. Dielectric constant at zero bias as a function of x in $SrTiO_{(3\pm y)}$–$(SiO_2)_x$ thin films annealed at various temperatures indicated.

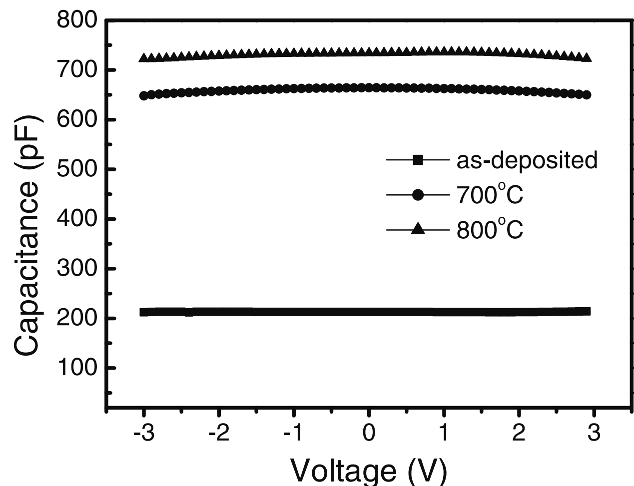

Figure 7. Capacitance versus applied voltage for $SrTiO_{(3\pm y)}$–$(SiO_2)_x$ thin film with $x = 0.25$ annealed at various temperatures indicated.

constant of the $SrTiO_{(3\pm y)}$–$(SiO_2)_x$ thin films decreasing with increasing Si content.

The variation of capacitance of $SrTiO_{(3\pm y)}$–$(SiO_2)_x$ thin films with $x = 0.25$ deposited at 400°C and annealed at various temperatures with bias voltage is shown in figure 7. The capacitance values keep constant with various sweep bias voltages which indicate a paraelectric property [10, 11].

Figure 8 depicts the leakage current density at $100\,\mathrm{kV\,cm^{-1}}$ as a function of x in the $SrTiO_{(3\pm y)}$–$(SiO_2)_x$ thin films annealed at various temperatures indicated. The leakage current density of the films decreases with increasing x at the same annealing temperature. The Si added films with the smaller sized grains have more grain boundaries with more resistive regions than larger size grains, leading to lower leakage current. It was shown that the grain resistivity of $SrTiO_3$ ceramic was several ohmcentimetre while that of the grain boundary was about several megaohm centimetre [12]. The grain sizes of the films with $x = 0.45$ annealed at 700°C and 800°C are about 12.21 nm and 13.27 nm, respectively, which were calculated by the Scherrer equation. It was also

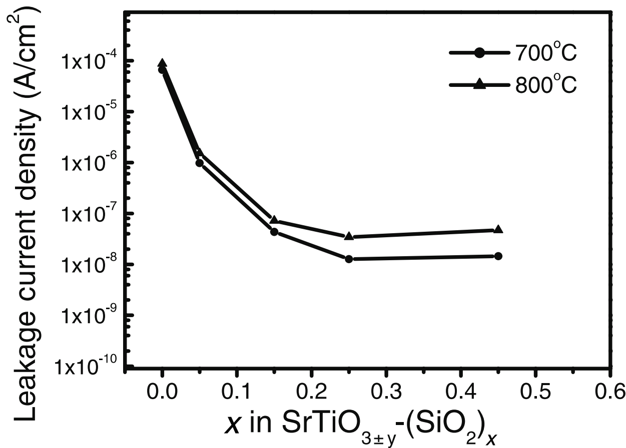

Figure 8. Leakage current density as a function of x in $SrTiO_{(3\pm y)}$–$(SiO_2)_x$ thin films annealed at 700˚C and 800˚C.

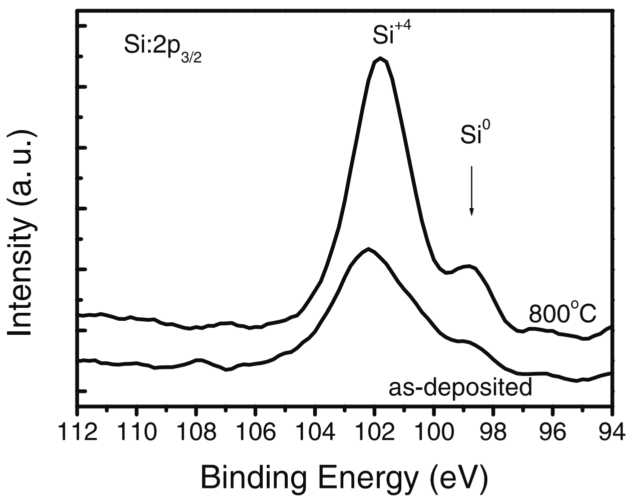

Figure 9. XPS spectrum of the Si 2p 3/2 for the $SrTiO_{(3\pm y)}$–$(SiO_2)_x$ thin film with $x = 0.45$ annealed at 800˚C.

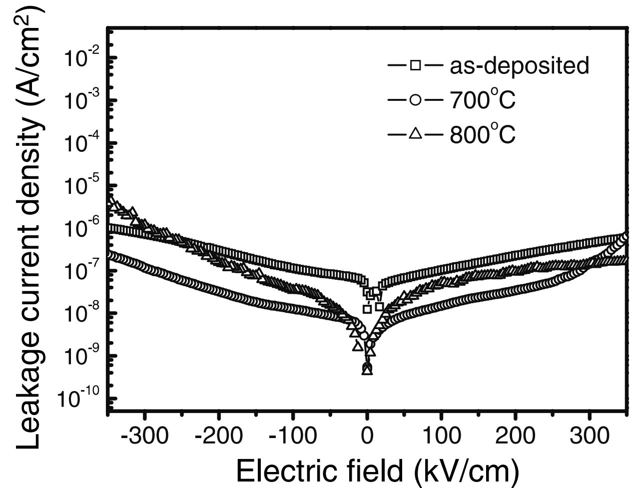

Figure 10. Curves of leakage current density versus electric field for $SrTiO_{(3\pm y)}$–$(SiO_2)_x$ thin film with $x = 0.25$ annealed at various temperatures indicated.

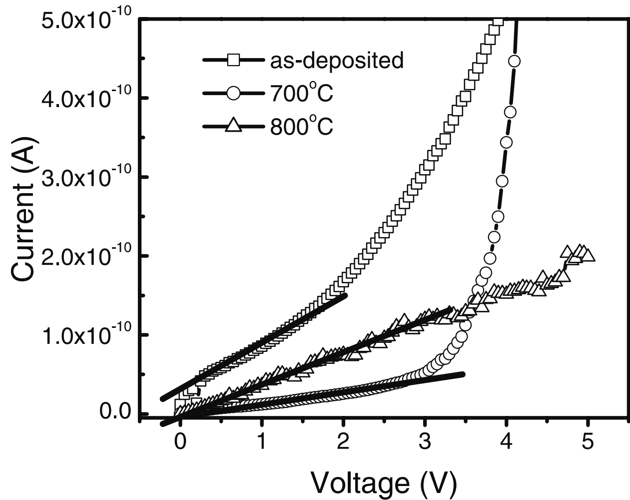

Figure 11. Current versus voltage plots of $SrTiO_{(3\pm y)}$–$(SiO_2)_x$ thin films at various temperatures indicated.

indicated that the films with fine grain size had lower leakage current density than films with coarse gain size [13]. The leakage current density of the $SrTiO_{(3\pm y)}$–$(SiO_2)_x$ thin film increases with increasing annealed temperature at the same Si content owing to the improved crystallinity and larger grain size in higher temperature annealed film. The leakage current of the films with x value over 0.25 annealed at the same temperature does not decrease, but instead slightly increases with increasing x. This could be due to the segregation of the conductive Si. This explanation can be supported by the XPS spectrum of the Si 2p peak obtained from $x = 0.45$ thin film deposited at 400˚C and annealed at 800˚C (as shown in figure 9). The spectrum clearly shows the Si^{+4} and Si^0 peak simultaneously. The Si^{+4} peak represents the Si–O bonding, but the Si^0 peak comes mainly from segregation. The segregation of conductive Si leads to the leakage current density increase.

The relation of leakage current density versus electric field of $SrTiO_{(3\pm y)}$–$(SiO_2)_x$ thin films with $x = 0.25$ and annealed at various temperatures is shown in figure 10. The films annealed at 700˚C have a leakage current of lower than 10^{-7} A cm^{-2} at 100 kV cm^{-1}. The as-deposited film has a higher leakage current, probably owing to carbon residue. The leakage current density of the thin film annealed at 700˚C is lower than that annealed at 800˚C, which is attributed to larger size grains that existed in the higher-temperature annealed film.

Figure 11 shows the plots of positive I (current) versus V (voltage) characteristics of the films annealed at various temperature in the MIM capacitor. It indicates the linear relationship between I and V existed at the low voltage part of those plots of as-deposited, 700˚C and 800˚C annealed films, which means that the conduction of this region is an ohmic behaviour. In general, the Schottky or/and Poole–Frenkel mechanisms are used to explain current transportation in ferroelectric films at moderate and high fields [14–16]. If the carrier transport obeys the Schottky model the logarithm of the current depends linearly on the square root of the applied voltage. If the current is governed by the Poole–Frenkel model, then $\log(I/V)$ varied with the square root of the

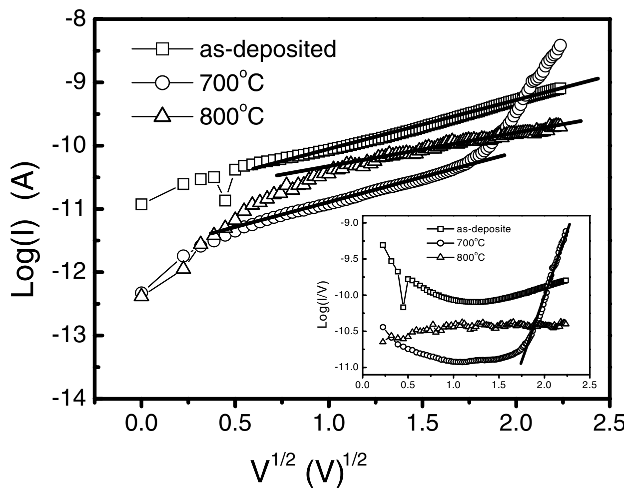

Figure 12. Log (I) and log (I/V) versus $(V)^{1/2}$ plots of $SrTiO_{(3\pm y)}$–$(SiO_2)_x$ thin film annealed at various temperatures indicated.

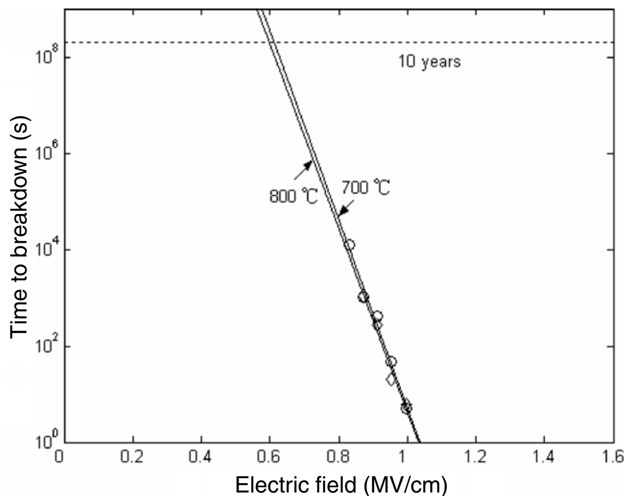

Figure 13. TDDB plots for $SrTiO_{(3\pm y)}$–$(SiO_2)_x$ thin films with $x = 0.25$ annealed at 700°C and 800°C.

voltage is a linear function [17]. To identify the current conduction mechanism, log(I) (current) and log(I/V) versus $V^{1/2}$ (electric field) relationships of $SrTiO_{(3\pm y)}$–$(SiO_2)_x$ thin films with $x = 0.25$ are plotted and shown in figure 12. The as-deposited and 800°C annealed films at high voltage and 700°C annealed films at moderate voltage indicate a good linear relationship between log(I) and $V^{1/2}$, which suggests that the leakage current mechanism in these regions is Schottky emission. The leakage current of the film annealed at 700°C at high voltage indicate a good linearity in Poole–Frenkel plot (inset of figure 12), therefore, the mechanism in this region is the Poole–Frenkel emission.

The time-dependent dielectric breakdown (TDDB) plots (figure 13) indicate that the films operated at an electric field of above 0.6 MV cm^{-1} have a lifetime over 10 years. This reliability test also indicates that the lower the annealing temperature of the $SrTiO_{(3\pm y)}$–$(SiO_2)_x$ thin films, the higher the breakdown field of the films. In spite of different leakage currents there are comparably small deviations in the TDDB behaviour.

4. Conclusions

The 110 nm thick $SrTiO_{(3\pm y)}$–$(SiO_2)_x$ thin films were successfully prepared on a Pt/Ti/SiO_2/Si substrate by using the CSD method and then annealing at various temperatures. The Si content and annealing temperature of $SrTiO_{(3\pm y)}$–$(SiO_2)_x$ thin films play an important role in determining the state of crystallinity and electrical and dielectric properties. The crystallization temperature of the $SrTiO_{(3\pm y)}$–$(SiO_2)_x$ thin films decreases with increasing x value. The Si content of $SrTiO_{(3\pm y)}$–$(SiO_2)_x$ thin film depresses the grain growth and improves the density of the thin film. The crystalline phase and dielectric constant of STO thin film all gradually increase with annealing temperature. The leakage current density and dielectric constant of $SrTiO_{(3\pm y)}$–$(SiO_2)_x$ thin films decrease with increasing Si content. $SrTiO_{(3\pm y)}$–$(SiO_2)_x$ thin films with $x = 0.25$ annealed at 700°C have high dielectric constant and low leakage current of 94.8 and 1.27×10^{-8} A cm^{-2}, respectively. The TDDB curve indicates that the $SrTiO_{(3\pm y)}$–$(SiO_2)_x$ films with $x = 0.25$ annealed at 700°C and 800°C operated at an electric field of 0.6 MV cm^{-1} have an expected lifetime of over 10 years.

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