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A detailed study of soft breakdown modes for hafnium oxynitride (HfON) gate dielectrics under stress is investigated. Two types of soft breakdown, digital and analog modes, are observed in HfON gate dielectrics, featuring gate voltage fluctuation accompanying random telegraph noise and nonswitching $1/f$ noise, respectively. The dependence of gate area, oxide thickness, and stress current density on breakdown modes is also studied. Thin oxide thickness and small gate area contribute to the enhancement of charge to breakdown (Q_{bd}). Large Joule heat damage generated under stress inducing the analog soft breakdown for thick hafnium oxynitride films is proposed to clearly understand the breakdown of HfON gate dielectrics. © *2005 American Institute of Physics*. [DOI: 10.1063/1.1977198]

I. INTRODUCTION

The ultrathin oxide breakdown is an important issue for ultralarge scale integration (ULSI) integrated circuits (ICs). According to the International Technology Roadmap for Semiconductors (ITRS) projection,[1] the 70-nm node technology will require a gate dielectric with an effective oxide thickness (EOT) of 0.7–1.2 nm, approaching the limit of practical oxide thickness.[2] This is a fundamental limit which cannot be overcome by technological improvement. Nevertheless, since scaling of SiO_2 and oxynitride below 1 nm is not acceptable due to tunneling leakage,[3,4] nonuniformity[5] and intrinsic reliability concerns,[6,7] the gate dielectrics of a high dielectric constant (high k) are much requested. Of all the dielectric materials, hafnium dioxide (HfO_2)[8,9] and its silicate ($HfSi_xO_y$),[10,11] aluminate ($HfAl_xO_y$),[12,13] and oxynitride[14,15] (HfON) have gained much more attention in recent years.

It is widely studied that the breakdown degradation of ultrathin oxide (<5 nm) is quite serious when it is subjected to electrical stress.[16,17] Soft breakdown (SBD) or quasibreakdown is defined by an abrupt increase of oxide conductance which is several orders of magnitude smaller than that associated with the hard breakdown (HBD). It is related to the generation of a critical number of traps in the gate dielectric layer and the interface which forms a weak localized percolative cluster between the gate electrode and substrate,[18–22] while dielectric breakdown (hard breakdown) is considered to result from the amounts of electron fluence through the gate dielectrics.[23–25] Besides, two main types of quasibreakdown modes were investigated recently.[16,26,27] Digital soft breakdown (D-SBD) was reported to be due to the creations of electron trappings accompanied with lattice reconstruction to reduce the local strain.[26] The discrete level fluctuations are attributed to the slow trapping and emission of electrons at the traps located near the conductive path. On the other hand, analog soft breakdown (A-SBD) has various ranges of hopping process as a result of the existence of various leakage paths in the oxide with high density of localized states, affecting the bulk conductance of the film[28,29] and damaging the oxide lattice by the large Joule heat.[17,30]

However, for high-k gate dielectrics, little is known about the soft breakdown itself and the conduction properties after the breakdown. It was only reported that the Weibull slopes, area scaling factors, and lifetime projection for SBD and HBD were quite different.[31–34] In this work, we investigate the breakdown modes of hafnium oxynitride (HfON) gate dielectrics under stress. The dependence of gate area, oxide thickness, and stress current density on breakdown modes is also studied. Possible leakage paths of soft breakdown are proposed to clearly understand the breakdown of HfON gate dielectrics. The paper is organized as follows. The device fabrication and characterization processes used in the study are described in Sec. II. Section III presents the characteristics of soft breakdown. The emphasis is on the dependence of gate area, oxide thickness, and stress current density on breakdown modes. Finally, Sec. IV draws a conclusion.

II. EXPERIMENT

Al/TaN/HfO_2/p-Si capacitors with areas of 6.36×10^{-5} and 2.54×10^{-4} cm^2 were fabricated on 4-in. p-type Si wafers. First, the 5- and 12-nm-thick HfO_2 films were deposited by an electron-beam evaporation. After the gate dielectric had been formed, some of the samples were treated by NH_3 plasma at 20 W for 5 min (PNH_3) to form the HfON.[35] A TaN film of 25 nm was then deposited by a sputter. Thereafter, a 500-nm-thick Al film was deposited on the TaN film by a thermal coater. The gate of the capacitor was then defined lithographically and etched. Finally, a 500-nm-thick Al film was also deposited on the backside of the wafer

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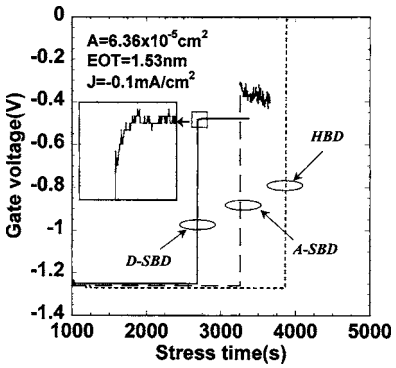

FIG. 1. Measured gate voltage under a -0.1 mA/cm^2 constant current stress of HfON gate dielectrics. Hard breakdown (HBD) and two types of soft breakdown (SBD), digital and analog modes, were observed. The inset shows the random telegraph switching noise (RTSN) of D-SBD.

to form the ohmic contact. The EOTs of 1.53 nm for 5 and 4.65 nm for 12-nm-thick HfO_2 films were estimated from the strong accumulation region of the high-frequency (0.1 MHz) capacitance-voltage (*C-V*) curves without deducting the quantum confinement effect. The *C-V* characteristics and stress test were measured by using a HP4284A precision *LCR* meter and a HP4156B semiconductor parameter analyzer, respectively.

III. RESULTS AND DISCUSSION

Figure 1 shows the gate voltage versus stress time characteristics of the 1.53-nm HfON gate dielectrics observed during a constant -0.1 mA/cm^2 current stress. The nearly constant gate voltage before the breakdown indicates that a small density of charge is trapped in the dielectric film. The HfON dielectrics breakdown properties are classified into three modes in accordance with their voltage-time characteristics after breakdown. Normal hard breakdown is observed with an obvious voltage change of the dielectrics. A relatively small voltage drop, called soft breakdown, gives rise to an important reliability issue for future metal-oxide-semiconductor (MOS) device with high-*k* gate dielectrics.[36,37] After soft breakdown, voltage fluctuation like nonswitching $1/f$ noise is called the A-SBD, while random-telegraph-switching-noise-like fluctuation (RTSN) shown in the inset of Fig. 1 is the D-SBD. A difference between analog and digital modes is also seen in the *J-V* characteristics of the postbreakdown HfON dielectric film. Figure 2 shows the gate current density versus gate voltage characteristics of the 1.53-nm HfON gate dielectrics under a -0.1 mA/cm^2 constant current stress. For a 10-s stress, the stress-induced leakage current (SILC) is found to be similar to the fresh sample. After the soft breakdown, the gate current increases dramatically. The characteristics of analog mode SBD are quite different from that of digital mode, which the gate current is found to be much smaller.

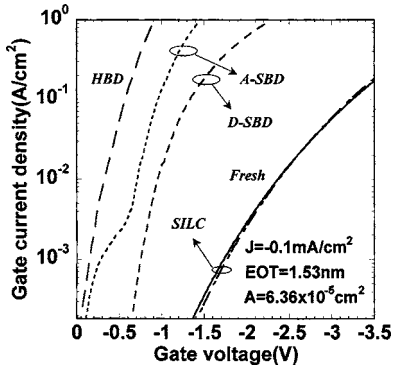

FIG. 2. Current density vs gate voltage (*J-V*) characteristics of fresh and degraded HfON gate dielectrics with an oxide thickness of 1.53 nm. The stress current density is -0.1 mA/cm^2.

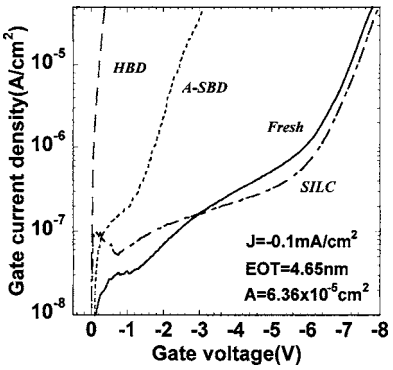

FIG. 3. Current density vs gate voltage (*J-V*) characteristics of fresh and degraded HfON gate dielectrics with an oxide thickness of 4.65 nm. The stress current density is -0.1 mA/cm^2.

Figure 3 shows the gate current density versus gate voltage characteristics of the 4.65-nm HfON gate dielectrics under a -0.1 mA/cm^2 constant current stress. Gradual increase of SILC is observed in the initial stage and called the low-voltage peak current (LVPC) owing to the hole injection to traps in the vicinity of HfON/interfacial layer (IL) interface through the interfacial layer.[38] Unlike the thin HfON film, analog mode soft breakdown is preferred to occur at the thick HfON gate dielectrics after the breakdown. This breakdown will increase the gate leakage current greatly. Figure 4 shows the generation probability of each mode as a function of stress current density, capacitor area, and dielectric thickness.

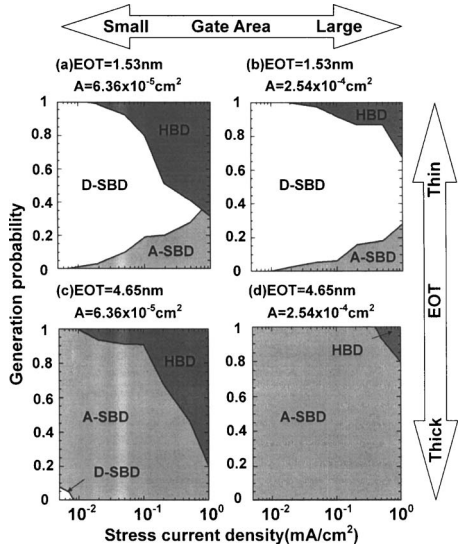

FIG. 4. Generation probability of HBD, digital soft breakdown (D-SBD), and analog soft breakdown (A-SBD) as a function of stress current density, capacitor area, and oxide thickness.

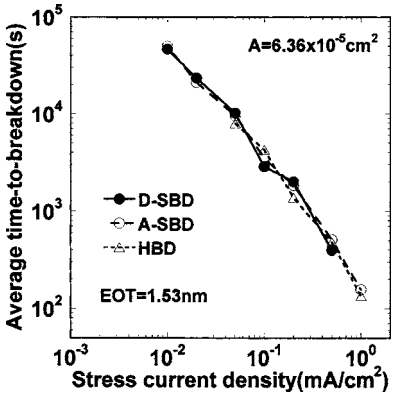

FIG. 5. Stress current-density dependence of time to breakdown for hard breakdown and two modes of soft breakdown. Averaged values are obtained using 20 samples with EOT of 1.53-nm HfON gate dielectrics for each stress condition.

We carried out the breakdown experiments using 20 samples for each stress condition. Digital and analog modes of SBD occur mainly in thin and thick gate dielectrics, respectively, and the generation probability of SBD increases with capacitor area. Note that the digital SBD can be observed in thick HfON film when gate area and stress current density are sufficiently small. Moreover, hard breakdown becomes dominant at high stress current both in thin and thick dielectric films.

Figure 5 shows the stress current density versus average time-to-breakdown characteristics of 1.53-nm HfON gate dielectrics with a gate area of 6.36×10^{-5} cm^2. The time to breakdown (t_{BD}) has a strong relationship with the stress current density. It should be noticed that all the data lie on a universal line, indicating that t_{BD} is a unique function of the stress current density regardless of the breakdown modes, which have been observed at the ultrathin silicon dioxide.[26,27] Figure 6 shows the Weibull distribution of charge to breakdown (Q_{bd}) of HfON gate dielectrics with EOTs of 1.53 and 4.65 nm and gate areas of 6.36×10^{-5} and 2.54×10^{-4} cm^2. A constant current-density stress of -0.2 mA/cm^2 is applied to the dielectric films. Large charge to breakdown is obtained at thin HfON gate dielectrics and small gate area. We can also obtain the breakdown charge up

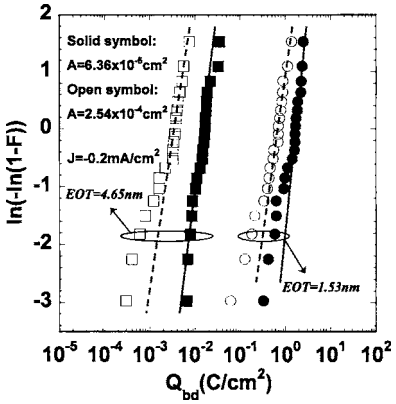

FIG. 6. Weibull distribution of charge to breakdown (Q_{bd}) of HfON gate dielectrics with EOT, of 1.53 and 4.65 nm and gate areas of 6.36×10^{-5} and 2.54×10^{-4} cm^2. Constant current stress (-0.2 mA/cm^2) is applied to the gate.

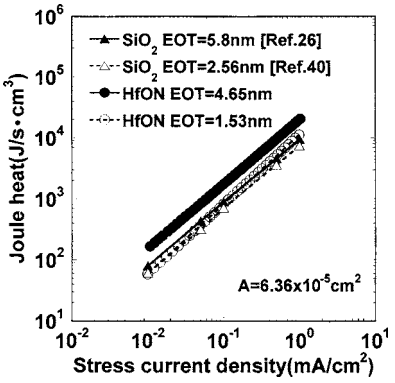

FIG. 7. Average Joule heat vs stress current density of HfON and SiO_2 films with different EOTs. The circular and triangular symbols represent the HfON and SiO_2 films, respectively. The gate area is 6.36×10^{-5} cm^2.

to 2.5 C/cm^2 from the 1.53-nm HfON gate dielectrics with the gate area of 6.36×10^{-5} cm^2. To determine the lifetime dependence on area scaling, we then investigate the Weibull slope β of HfON film with different gate areas. The Weibull slope β of thin and thick HfON films with small areas are about 1.85 and 2.4, respectively, whereas that with large areas are about 1.44 and 1.2, respectively. For intrinsic breakdown, the Weibull slope β of thin and thick oxide films was almost the same and exhibited small thickness dependence for gate injection. It was suggested that the breakdown of dielectric films was determined by process-induced defects, causing weak points in oxide.[33,39] However, for high-k/IL-stacked structure, interfacial layer between the high-k film and silicon substrate plays an important role on the breakdown, especially on soft breakdown. The decrease of Weibull slope β with gate area increasing for the thick HfON films is much larger than that for the thin one owing to the high probability of SBD occurrence, as shown in Fig. 4. Note that digital and analog modes of SBD occur mainly in thin and thick HfON films, respectively, meaning the D-SBD exhibits smaller area dependence of Weibull slope β than the A-SBD.

Figure 7 shows the average Joule heat versus stress current density of HfON and SiO_2 films with different EOTs. Obviously, the Joule heat increases with the stress current density. Hafnium oxynitride with thick oxide thickness exhibits larger Joule heating under stress than that with the thin one. However, the Joule heats of thin and thick SiO_2 films from Ning and Tomita *et al.*,[40,26] respectively, are almost the same, which are much smaller than that of the thick HfON film. It is reported that the Joule heat is directly related to the thermal conductivity of the dielectric films.[41,42] For ultrathin dielectric films, the thermal conductivity is determined by the deposition method and interface thermal resistance (R_I). The HfON films deposited by physical vapor deposition (PVD) exhibit high void density and high interface thermal resistance, resulting in the low thermal conductivity as compared to the thermal SiO_2 films. The low thermal conductivity will contribute to the high Joule heating in the local conductive path, leading to lateral propagation of the leakage spots and the dielectrics are more easily broken down. Moreover, large current flows through the leakage path, and the additional traps create to enlarge the leakage more laterally.

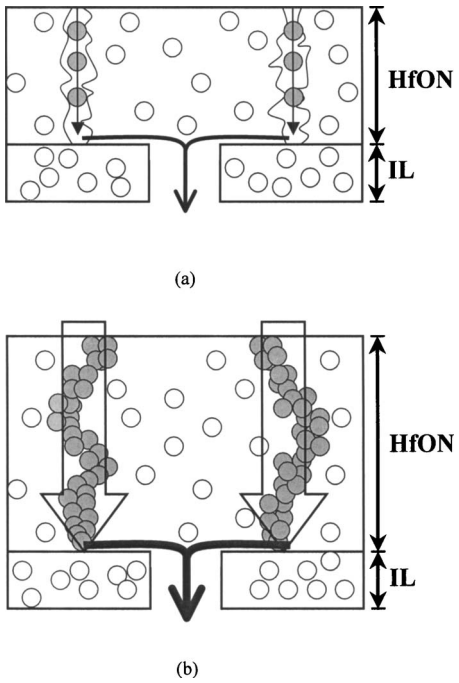

FIG. 8. Schematic view of leakage paths of soft breakdown for HfON/interfacial layer-stacked structure with (a) thin and (b) thick oxide thicknesses. Prior breakdown of interfacial layer (IL) owing to the high field applied leads to the soft breakdown of the hafnium oxynitride gate dielectrics.

When the current on the occurrence of pre-SBD is large enough to damage the HfO_2 lattice, current conduction characteristics are changed,[27] resulting in the significant A-SBD of thick hafnium gate dielectrics. For thin dielectric films, D-SBD is quite easy to happen (shown in Fig. 4) owing to the low Joule heat generated as compared with the thick one. Besides, we can also find that the electrical conductivity increases enormously after the analog SBD, which is larger than that after the digital SBD, as shown in Fig. 2. Previous research[43] has proposed that Joule heating will lead to the increase of electrical conductivity of gate dielectrics after the soft breakdown. Figure 8 shows the schematic views of leakage paths of soft breakdown for HfON/IL-stacked structure with (a) thin and (b) thick dielectric thicknesses. Prior breakdown of interfacial layer owing to the high electric field applied is proposed,[33,44,45] leading to the apparent soft breakdown effect of the hafnium oxynitride gate dielectrics. The low-energy dissipation in the oxide layer and trapping and emission of electrons at the traps located near the conductive path in the gate dielectrics contribute to the digital soft breakdown of thin HfON film shown in Fig. 8(a). On the other hand, as shown in Fig. 8(b), the existence of various leakage paths in the dielectric film with high density of localized traps owing to the large Joule heating under stress is responsible for the obvious analog soft breakdown in thick HfON film.

IV. CONCLUSION

In this work, characterization of soft breakdown modes for HfON gate dielectrics under stress was proposed. We have observed that soft breakdown can be classified into two different modes, digital and analog SBD, for HfON gate dielectrics. Digital SBD featured gate voltage fluctuation accompanying random telegraph noise and analog mode showed a nonswitching $1/f$ noise-like fluctuation. The dependence of gate area, oxide thickness, and stress current density on breakdown modes was investigated, and thin oxide thickness and small gate area contributed to the enhancement of charge to breakdown (Q_{bd}). We have also proposed that large Joule heat damage induced the analog soft breakdown for thick hafnium oxynitride film, and the breakdown of HfON gate dielectrics was clearly understood.

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