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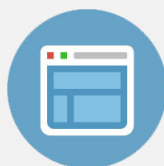
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# Substrate-bias-dependent dielectric breakdown in ultrathin-oxide *p*-metal-oxide-semiconductor field-effect transistors

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An explanation of the breakdown behavior of ultrathin-gate-oxide (1.6 nm) *p*-metal-oxide-semiconductor field-effect transistors under a reverse substrate bias is presented. A significant degradation in lifetime induced by a positive substrate bias and a decrease in the power-law exponent ( $n$ ) were observed. The quantitative hydrogen-based model [J. Sune and E. Wu, Digest of Technical Papers, 2001 Symposium on VLSI Technology, Kyoto, Japan, 12–14 June 2001 (unpublished), p. 97] is used to explain this observation while taking the channel quantization effect into consideration. Using this model, the stress voltage dependence of time-dependent dielectric breakdown in our experiment fits well with simulation results. This indicates that the degradation is due to the channel hole quantization-enhanced dissipation energy of injected electrons at the anode interface. © 2005 American Institute of Physics. [DOI: 10.1063/1.1980529]

## I. INTRODUCTION

Gate oxide breakdown has been considered to be one of the most important issues for aggressive oxide thickness scaling. In ultrathin-gate-oxide devices, high fields applied to oxides result in bulk defect generation, interface state formation, and eventually breakdown. The most widely accepted theories to address the defect generation are the anode hole injection (AHI) model<sup>1</sup> and the anode hydrogen release (AHR) model.<sup>2</sup> However, neither AHI nor AHR can explain the recent observations of voltage-dependent voltage acceleration of oxide breakdown for ultrathin oxides. Either the analytical formulation of AHI does not seem to be viable or the contribution of AHI is very small while stressed under low voltage in an ultrathin oxide.<sup>3,4</sup> Accordingly, a power-law extrapolation with a quantitative hydrogen-based model for the degradation and breakdown of ultrathin gate oxides is proposed.<sup>5,6</sup> It has been shown that this quantitative hydrogen-based model can successfully explain the decoupled plasma nitridation (DPN) pressure dependence of oxide breakdown behavior in ultrathin-oxide *p*-metal-oxide-semiconductor field-effect transistors (*p*MOSFETs).<sup>7</sup>

Although the substrate bias dependence of oxide breakdown in *p*MOSFETs under negative gate bias stress has been discovered,<sup>8</sup> the additional impact ionization induced by the positive substrate bias ( $V_b$ ) at the substrate bulk, which was proposed to be the main cause of lifetime degradation in Ref. 8, could not precisely explain the lifetime versus applied gate bias ( $V_g$ ) characteristics in ultrathin-oxide *p*MOSFETs. In

this paper, we further discuss the time-dependent dielectric breakdown (TDDB) behavior of ultrathin-oxide *p*MOSFETs ( $p^+$  polysilicon gate and *n*-type silicon substrate) biased in inversion under various reverse substrate biases. A significant decrease in the substrate-bias-induced power-law exponent will be shown. Finally, a modified quantitative hydrogen-based model with channel quantization effect and its simulation results are used to explain these observations.

## II. EXPERIMENT

The  $p^+$  poly gate *p*MOSFETs used in this work were fabricated with a 90-nm standard complementary metal-oxide semiconductor (CMOS) process on an *n*-type silicon substrate. The gate length is 0.09  $\mu\text{m}$ , the gate width is 10  $\mu\text{m}$ , and the physical oxide thickness is 1.6 nm. The nitrided gate oxide was grown by a 1.4-nm *in situ* steam generation (ISSG) followed by UMC's standard decoupled plasma nitridation (DPN) process. All devices were stressed using constant voltage stress (CVS) at 140 °C. The stress gate voltage varies from  $-2.5$  to  $-2.9$  V for inversion mode TDDB stress (electron injection is from  $p^+$  polysilicon with an *n*-type silicon substrate biased in inversion). The stress substrate biases were 0, 4, and 7 V, with the source and drain grounded. The initial breakdown event (a 20% jump in gate current) was defined as an oxide breakdown regardless of the soft or hard breakdown. The sample size was about 20–30 samples per stress voltage.

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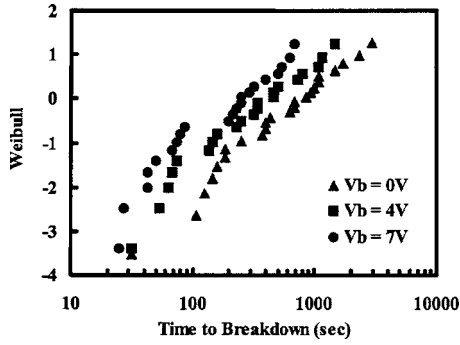


FIG. 1. Weibull distribution of time to breakdown (TBD) on *p*MOSFETs with  $T_{ox}=1.6$  nm. The stress gate bias is  $-2.9$  V with  $V_b=0, 4,$  and  $7$  V.

III. RESULTS AND DISCUSSION

In order to investigate the role of the substrate bias in time-dependent dielectric breakdown of *p*MOSFETs under inversion mode stress, we simply stressed the devices under various  $V_b$ . The results are shown in Fig. 1. Apparently, a reverse substrate bias aggravates defect generation and consequently decreases the time to breakdown. The stress voltage dependence of breakdown lifetime is depicted in Fig. 2. The stress gate bias varies from  $-2.5$  to  $-2.9$  V. We clearly see a decrease of the power-law exponent ( $n$ ) as  $V_b$  increases when the power-law model was used. This decreases the TDDB lifetime at the operating voltage, which is extrapolated from the TDDB lifetime under stress voltage for some applications under a reverse substrate bias.

It was proposed that the degradation of time to breakdown ( $T_{BD}$ ) and the decrease of the power-law exponent might be due to the additional impact ionization at the substrate bulk with reverse  $V_b$ ,<sup>8</sup> as illustrated in Fig. 3. In this mechanism, applying a positive substrate bias increases the potential drop in the depletion region (anode) without changing the gate field or direct tunneling electron injection from the  $p^+$  poly gate. The initial electrons are accelerated more with a larger  $V_b$  and generate hotter holes that are accelerated to even higher energies by an increased depletion field as they drift back to the oxide. It is noticeable that a larger impact ionization current, which signifies a higher impact ionization rate and results in larger substrate current ( $I_b$ ) as marked in Fig. 3, increases the defect generation in gate oxide. However, our work shows that the additional anode hot

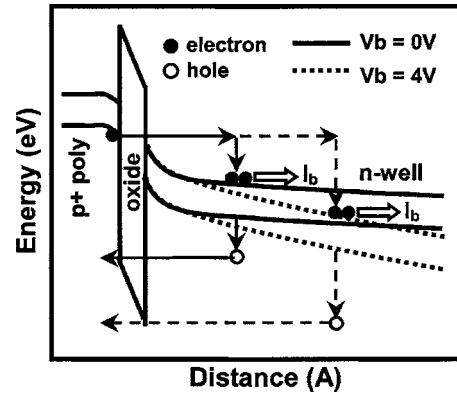


FIG. 3. Band diagram of a *p*MOSFET with and without a substrate bias, showing the generation and acceleration of hot holes. The impact ionization electrons contribute to the substrate current. It was recently proved that this phenomenon could not explain our observations in Fig. 2.

hole generation from substrate impact ionization has an opposite trend with what we have seen in Fig. 2. In Fig. 4, the substrate current was used to monitor the rate of anode hole generation under various substrate biases since each impact ionization results in an additional conduction-band electron, which contributes to the substrate current. In other words, the larger the substrate current measured, the shorter the TDDB lifetime should be, if the model presented in Fig. 3 of Ref. 8 is appropriate for our experiment. However,  $1/I_b$ , which is inversely proportional to the rate of anode hole generation and defect generation and hence directly proportional to  $T_{BD}$ , showed a dependence between  $V_g$  and TDDB that contradicts the data, as shown in Fig. 2. The junction leakage current between the drain (or source) and bulk has been eliminated by measuring the forward biased  $n^+-p$  junction current with  $V_b=0, 4,$  and  $7$  V. It suggests that the degradation of the power-law exponent cannot be well explained by this conventional AHI-based model.

According to the above result, a quantitative hydrogen-based model incorporating channel quantization was proposed to explain the phenomenon. The model is based on two processes related to chemical reactions involving protons.<sup>5</sup> Firstly, electrons, which are injected from the  $p^+$  poly gate in the direct tunneling regime, dissipate energy at the anode Si/SiO<sub>2</sub> interface and release protons ( $H^+$ ) from interface suboxide bonds, as shown in Fig. 5. Secondly, the

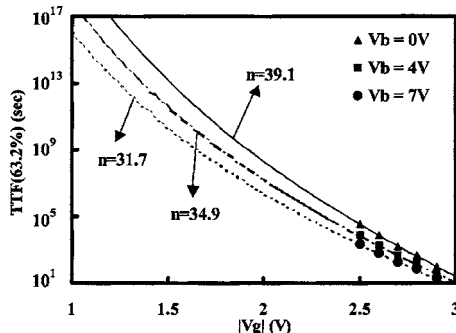


FIG. 2. Stress gate bias dependence of TDDB lifetime for devices in which width/length= $10 \mu\text{m}/0.09 \mu\text{m}$ . The symbols are experimental data and the curves are extrapolated by the power-law model.

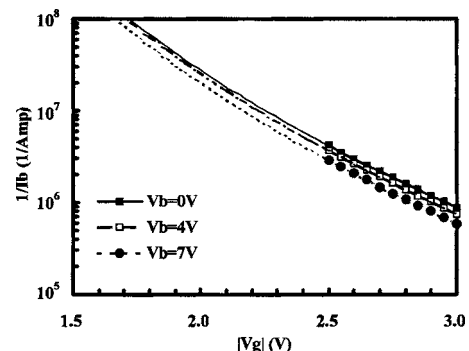


FIG. 4.  $1/I_b$  vs gate bias characteristic curves with  $V_b=0, 4,$  and  $7$  V. The inverse of the substrate current shows a slightly weaker  $V_g$  dependence at  $V_b=0$  V as compared with  $V_b=4$  and  $7$  V.

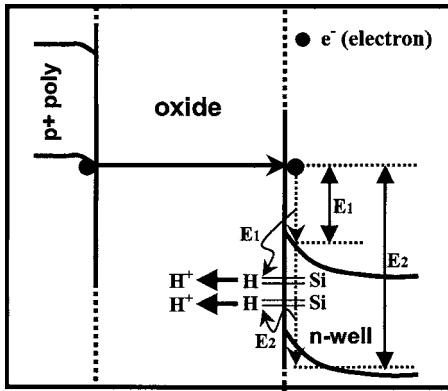


FIG. 5. Illustration of electron energy dissipation at the anode interface and the release of protons ( $H^+$ ) from interface suboxide bonds.

released protons react with oxygen vacancies ( $Si-Si$ ), as shown in Fig. 6. The rate of proton release from the interface,  $\xi_1(V, T)$ , is modeled as an electron-energy-assisted proton tunneling through an energy barrier [Eq. (1) and Fig. 7(a)]. The reaction of a proton with  $Si-Si$  is also described in quantum-mechanical terms by considering the tunneling of a proton through the potential barrier, which separates the two microscopic configurations before and after the reaction [Fig. 7(b)].<sup>5</sup> The description of chemical reactions in terms of potential barriers is a common practice in the field of quantum chemistry and is also considered in Refs. 9 and 10.

$$\xi_1(VT) = \frac{K_1}{1 + \exp[(E_{th1} + q\phi_B - qV)/E_0]}, \quad (1)$$

$$\xi_2(VT) = K_2 V^2 \exp\left(-\frac{B}{V}\right); \quad B = \frac{4(2m_H)^{1/2} t_{ox} E_{th2}^{3/2}}{3q\hbar}, \quad (2)$$

where  $V$  refers to the electron dissipation energy and the other parameters have the same definitions as in Ref. 5. The total defect generation rate is given by  $1/\xi = 1/\xi_1 + 1/\xi_2$ , and the bottleneck for the whole process is the slowest reaction. A detailed explanation of this quantitative hydrogen-based model is described in Ref. 5.

Taking the channel hole quantization effect into consideration, the energy-band diagram and the dissipation energy of valance band tunneling electrons at the anode  $Si/SiO_2$

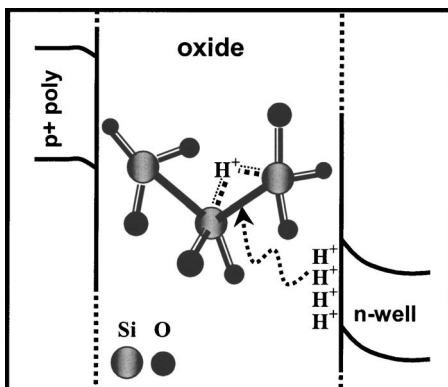


FIG. 6. Illustration of the released protons ( $H^+$ ) reacting with oxygen vacancies ( $Si-Si$ ). The solid and dashed bonds represent the state before and after the reaction, respectively.

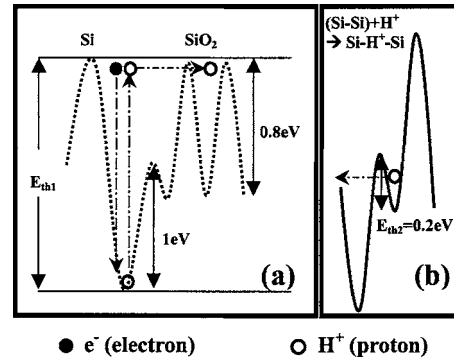


FIG. 7. Schematics of two processes involved in breakdown (Ref. 1). (a) Electron-assisted proton release from suboxide bonds at the interface,  $\xi_1$ . (b) Reaction of hydrogen bridge formation modeled by proton tunneling through an  $\sim 0.2\text{-eV}$  barrier.

interface are illustrated in Fig. 8. A larger positive substrate bias results in more serious channel quantization and hence the first hole subband energy at the channel region increases. It was then supposed that the TDDDB lifetime degradation under a reverse substrate bias might be due to the higher electron dissipation energy at the anode interface.

The maximum available energy ( $E_{max}$ ) is defined as the energy of electrons at the oxide/anode interface as measured with respect to either the anode conduction band or the anode valence band, depending on the availability of empty states in the silicon substrate valence band.<sup>11</sup> Under ballistic direct tunneling injection,  $E_{max} = V_{ox} + E_{h1}$  for  $p$ MOSFETs stressed in the inversion mode, where  $V_{ox}$  is the oxide voltage and  $E_{h1}$  is the first subband energy of channel holes (Fig. 8), while channel holes are mainly distributed at the first subband at temperatures under  $140^\circ\text{C}$ .<sup>12</sup> Figure 9 shows the simulated  $E_{h1}$  vs  $V_g$  characteristic curve for various substrate biases. The simulation results are calculated by solving the effective-mass Schrödinger equation (in the oxide and silicon regions) and the Poisson equation (in the polysilicon, oxide, and silicon regions) self-consistently [13,14]:

$$\left[ -\frac{\hbar^2}{2} \frac{d}{dz} \frac{1}{m_i^*} \frac{d}{dz} + V(z) - E_{ij} \right] \varphi_{ij}(z) = 0 \quad (3)$$

and

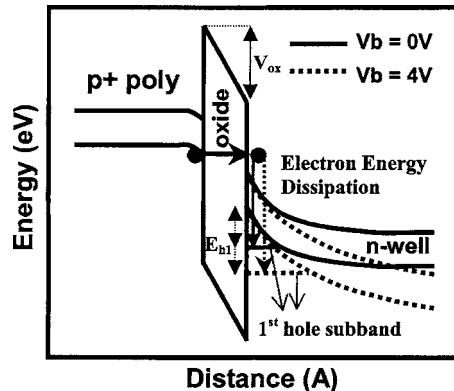


FIG. 8. Illustration of band diagram showing the electron dissipation energy at the anode interface with/without a reverse substrate bias. The electrons dissipate more energy when  $V_b = 4\text{ V}$ .

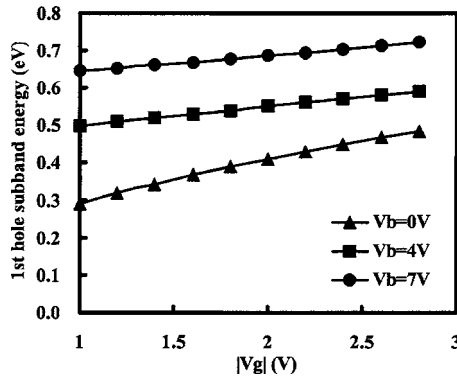


FIG. 9. Simulation of the first channel hole subband energy at various  $V_g$  with  $V_b=0, 4,$  and  $7$  V. A stronger  $V_g$  dependence of subband energy was observed at  $V_g=0$  V.

$$\frac{d}{dz} \left[ \varepsilon(z) \frac{d}{dz} \right] \phi(z) = \frac{q}{\varepsilon_0} [n(z) - p(z) + N_A^- - N_D^+], \quad (4)$$

where  $z$  is the direction perpendicular to the channel,  $m_i^*$  is the electron or hole effective mass in the  $i$ th valley,  $\varphi_{ij}$  is the envelope wave function for the  $j$ th subband in the  $i$ th valley,  $V$  is the potential energy, and  $N_A^-$  and  $N_D^+$  are the ionized acceptor and donor concentrations respectively. The potential energy  $V(z)$  in Eq. (3) is related to the electrostatic potential  $\phi(z)$  in Eq. (4) as follows:

$$V(z) = -q\phi(z) + \Delta E_c(z), \quad (5)$$

where  $E_c(z)$  is the energy due to the band offset at the Si/SiO<sub>2</sub> interface. The wave function  $\varphi(z)$  in Eq. (3) and the electron density  $n(z)$  in Eq. (4) are related by

$$n(z) = \frac{k_B T}{\pi \hbar^2} \sum_i g_i m_i^* \sum_j \ln \left[ 1 + \exp \left( \frac{E_f - E_{ij}}{k_B T} \right) \right] \varphi_{ij}^2(z), \quad (6)$$

where  $g_i$  is the  $i$ th valley degeneracy and  $m_i^*$  is the  $i$ th density-of-states effective mass.

The parameters used in simulation are  $m^*(\text{Si})=0.67m_0$ ,  $m^*(\text{SiO}_2)=0.55m_0$ ,  $\phi_h$  (hole barrier height at the SiO<sub>2</sub> interface) = 4.25 eV,  $t_{\text{ox}}=1.6$  nm, and  $N_B$  (substrate doping concentration) =  $1 \times 10^{18}$  cm<sup>-3</sup>. The higher the substrate bias, the weaker is the  $V_g$  dependence of  $E_{h1}$ . This simulation result is similar to our experimental results, which showed a weaker  $V_g$  dependence of  $T_{\text{BD}}$  at higher  $V_b$ .

Replacing the  $V$  value of Eqs. (1) and (2) by  $V \sim E_{\text{max}} = V_{\text{ox}} + E_{h1}$ , the experimental breakdown data fit very well, as shown in Fig. 10. The other model parameters obtained from the fit are  $E_{\text{th1}}=1.8$  eV,  $E_{\text{th2}}=0.2$  eV,  $E_0=0.07$  eV,  $B=100$  V, and  $K_1/K_2=0.04$  V<sup>-2</sup>. These values are the same as those in Ref. 5. This gives an important piece of support to our model. It implies that the decrease of the power-law exponent under a reverse substrate bias for  $p$ MOSFETs

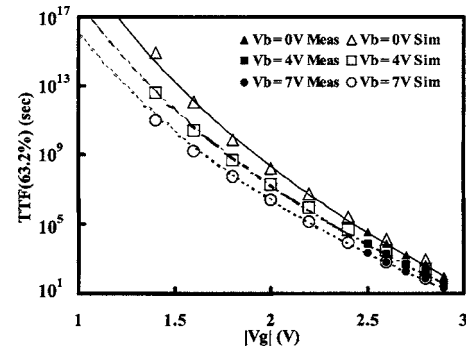


FIG. 10. Lifetime vs  $V_g$  plot of measurement and simulation data with various  $V_b$ . The filled symbols represent the measurement data and the open symbols represent the simulation data. The lines are the extrapolation curves from the measurement data.

stressed in inversion might be due to the variation of the first hole subband energy, which is related to the electron dissipation energy at the anode interface.

#### IV. CONCLUSION

A significant degradation of TDDDB lifetime and a decrease of the power-law exponent when a reverse substrate bias is applied on ultrathin-oxide  $p$ MOSFETs were shown in this paper. We discovered that the conventional model, in which the substrate bias influences only the impact ionization at the substrate bulk, could not explain this phenomenon. Accordingly, a quantitative hydrogen-based model incorporating the channel hole quantization effect is presented to explain this breakdown behavior. Using this model, the simulation results are in agreement with the experiments. The excellent agreement between the model and the experimental data suggests that the lifetime degradation under reverse  $V_b$  might be due to the channel-quantization-enhanced electron dissipation energy, which is the energy supply of defect generation, at the anode interface.

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