Formation of dual-phase Hf O 2 – Hf x Si 1 x O 2 dielectric and its application in memory devices

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Formation of dual-phase $HfO_2-Hf_xSi_{1-x}O_2$ dielectric and its application in memory devices

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In this paper, we studied the phase-separation phenomenon of $Hf_{0.5}Si_{0.5}O_2$ film deposited on SiO_2 or sandwiched by SiO_2, by x-ray photoelectron spectroscopy and transmission electron microscopy. The $Hf_{0.5}Si_{0.5}O_2$ film underwent phase separation to form a doublet-phase $HfO_2-Hf_xSi_{1-x}O_2$ ($x<0.5$) film, and was used as a trapping layer in a metal-blocking oxide-silicon nitride-tunnel oxide-silicon-type memory structure, where the dual-phase $HfO_2-Hf_xSi_{1-x}O_2$ (DPHSO) film replaces the conventional silicon nitride (Si_3N_4) trapping layer. The charge storage properties of the DPHSO film were investigated and compared with HfO_2 and Si_3N_4. It was found that for a given electric field applied to the tunnel oxide, the programming speed of memory devices using a DPHSO or HfO_2 film as a trapping layer is faster than that using Si_3N_4. This indicates the higher electron-capture efficiency of the DPHSO and HfO_2 films. In addition, the double-phase microstructure of the DPHSO film also provided better retention property than pure HfO_2. © *2005 American Institute of Physics*. [DOI: 10.1063/1.1954870]

I. INTRODUCTION

The polycrystalline silicon- or metal-oxide-nitride-oxide-silicon (SONOS or MONOS, respectively) nonvolatile memory structure has received considerable attention for application in electrically erasable and programmable read only memory (EEPROM) devices.[1–3] The attractiveness of the MONOS flash memory, compared to the current commercial floating gate memory, lies in its low programming/erasing voltage, immunity to drain-induced turn on,[4] and improved retention and endurance properties because the local defect-related charge leakage can be significantly reduced.[2,3] Recently, materials such as high-permittivity (high k) dielectrics, e.g., Ta_2O_5, HfO_2, and Al_2O_3, have been explored to replace silicon nitride in the SONOS or MONOS structure to improve both the programming and retention properties.[1–3]

Hafnium silicate dielectric film is an attractive trapping material in MONOS memory application due to its process compatibility with the conventional complementary metal-oxide semiconductor (CMOS) process. In addition, hafnium silicate is known to undergo phase separation[5–8] to form a crystalline hafnium oxide (HfO_2) phase and an amorphous-silica-rich phase when annealed at temperatures above 900 °C, giving rise to a unique microstructure comprising HfO_2 nanocrystals that could be suitable for memory applications. Therefore, a memory device with a hafnium silicate trapping layer could combine the benefits of the MONOS structure and the nanocrystal memory. Recently, Lin *et al.*[9] demonstrated memory devices comprising HfO_2 dots formed by the phase separation of the hafnium silicate film. In this article, we focus on the materials analysis of the dielectric stack in the memory device structure (silicate film deposited on SiO_2 or sandwiched by SiO_2) because the top and bottom SiO_2 may impact the thermal stability of the silicate film. We also provided experimental comparison of the trapping properties of the dual-phase $HfO_2-Hf_xSi_{1-x}O_2$ (DPHSO) film with those of the HfO_2 and Si_3N_4 films in MONOS-type memories, in order to better evaluate the advantage of each material in MONOS-type memory applications. The programming and retention properties are also compared. The relation between the device performance and material property is analyzed.

II. DEVICE FABRICATION

Memory devices with the $TaN/SiO_2/X/SiO_2/Si$ structure were fabricated, where X represents the charge-trapping layer which can be DPHSO, HfO_2, or Si_3N_4. A schematic of the device structure is shown in Fig. 1. Tantalum nitride (TaN) is selected as the gate material, instead of n^+ polysilicon, because the midgap work function of TaN has been reported to contribute to an enlarged memory window by reducing electron injection from the gate through the blocking oxide during erase operation.[10]

P-type Si (100) substrates were used as the starting materials. After a standard pre-gate clean, a 4-nm-thick SiO_2 tunnel oxide was grown by dry oxidation at a temperature of

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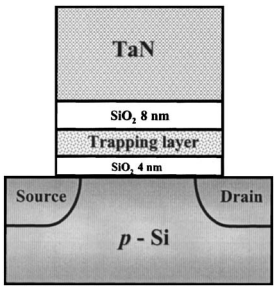

	$Hf_{0.5}Si_{0.5}O_2$	HfO_2	Si_3N_4
Trapping layer thickness (nm)	6	8	9
Capacitance effective thickness t_{eff} (nm)	13.9	13.6	17.8

FIG. 1. Schematic diagram showing the cross section of the memory device. The inset shows the thicknesses of the trapping layer and the capacitance effective thickness (t_{eff}) of the entire dielectric stack which is calculated for the accumulation regime.

800 °C. On one wafer, a $Hf_{0.5}Si_{0.5}O_2$ film was deposited on the SiO_2 tunnel oxide by the cosputtering of Hf and Si targets in an argon and oxygen ($Ar+O_2$) ambient at a pressure of 3 mTorr. On the first control wafer, the HfO_2 film was formed on the tunnel oxide by reactive sputtering of a Hf target in the $Ar+O_2$ ambient. On the second control wafer, a Si_3N_4 film was formed on the tunnel oxide by sputtering Si in an ambient containing argon and nitrogen. The thicknesses of the $Hf_{0.5}Si_{0.5}O_2$, HfO_2, and Si_3N_4 films were controlled by adjusting the sputter-deposition rate. The physical thicknesses of the $Hf_{0.5}Si_{0.5}O_2$, HfO_2, and Si_3N_4 charge-trapping layers (Fig. 1) were measured by an ellipsometer and a profiler. The thicknesses were different as no process optimization to match the thicknesses was made. Next, all the charge-trapping layers were capped with an 8-nm-thick SiO_2 which was formed by low-pressure chemical vapor deposition (LPCVD) using a $Si(OC_2H_5)_4$ (TEOS) precursor at a deposition temperature of 700 °C. Subsequently, a 150-nm-thick TaN metal gate was formed by sputtering a Ta target in an $Ar+N_2$ ambient with a dc power of 450 W at a pressure of 3 mTorr, followed by gate patterning and etching. Finally, As^+ implantation and activation anneal at 1000 °C were performed to form the source/drain regions.

III. MATERIALS CHARACTERIZATION

X-ray photoelectron spectroscopy (XPS) and transmission electron microscopy (TEM) were utilized to investigate the material properties of the $Hf_{0.5}Si_{0.5}O_2$ film, paying particular attention to phase transformation and distribution.

The $Hf_{0.5}Si_{0.5}O_2$ film employed for XPS characterization was formed by the same process as that used for device fabrication. The $Hf_{0.5}Si_{0.5}O_2$ film was then annealed at various temperatures in an inert ambient, and XPS was used to reveal the change of the chemical composition of the $Hf_{0.5}Si_{0.5}O_2$ film as the anneal temperature increases. The ratio of Hf and Si in the film was found to be 1:1 from compositional XPS analysis. Figure 2 shows the spectra of the O 1*s* core level of the $Hf_{0.5}Si_{0.5}O_2$ films as deposited and after annealing at 900 and 1000 °C. The O 1*s* binding energies of SiO_2 and HfO_2 are 533.4 and 530.6 eV, respectively,[11] as indicated in Fig. 2. The O 1*s* binding energy of an amorphous hafnium silicate with a composition of $Hf_6Si_{29}O_{65}$ is about 532.4 eV,[12] and this is also indicated in Fig. 2. Considering the fact that Zr and Hf have similar electronic configurations, one may refer to Ref. 13 for an interpretation of the XPS spectra. Reference 13 gives a detailed analysis of the XPS spectra shape and peak positions of Zr silicate films. In our experiment, the difference between the XPS spectra of as-deposited samples and samples annealed at high temperatures confirms phase separation, showing two types of chemical composites in the annealed $Hf_{0.5}Si_{0.5}O_2$ films. By fitting the XPS spectra using two Gaussian profiles as shown in Fig. 2, it is determined that the two components in the annealed (900 or 1000 °C) samples are HfO_2 and hafnium silicate. The difference between the 900 and 1000 °C annealed samples is that the ratio of O atoms associated with HfO_2 is larger in the 1000 °C annealed sample, indicating further phase separation of $Hf_{0.5}Si_{0.5}O_2$ film at 1000 °C. Hence, the XPS study reveals HfO_2 and silica-rich Hf silicate phases in the $Hf_{0.5}Si_{0.5}O_2$ film after high-temperature annealing.

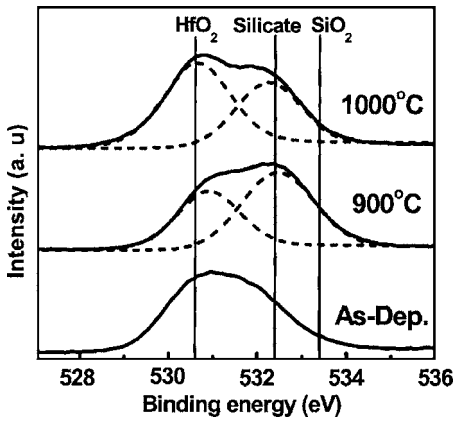

FIG. 2. XPS spectra showing the O 1*s* core level of the as-deposited (As-Dep.) $Hf_{0.5}Si_{0.5}O_2$ film after annealing at 900 and 1000 °C. High-temperature anneal leads to the formation of two phases, including the HfO_2 phase and the Hf-silicate phase.

A cross-sectional TEM picture of a $SiO_2/Hf_{0.5}Si_{0.5}O_2/SiO_2$ sandwich structure annealed at 900 °C is shown in Fig. 3. Microstructures showing crystalline phases embedded in an amorphous matrix are clearly observed. The size of the crystals is in the range of 5–10 nm. Since the kinetic-energy barrier needed to form a crystalline hafnium silicate is large, the crystalline silicate phase can never be observed under normal annealing conditions,[5–8] thus we believe that the crystals in Fig. 3 should be HfO_2. In addition, the lattice constant measured from TEM is about 0.31 nm, which is close to the (111) lattice constant of a monoclinic HfO_2 crystal. The amorphous phase in Fig. 3 is considered to be a hafnium silicate matrix with a significant brightness contrast from that of the underlying SiO_2. For the sample which was annealed at 1000 °C, two phases were also observed in the trapping layer by TEM, but the size of the crystals is larger than that observed in the sample annealed at 900 °C, and the brightness constrast between the amorphous phase and the underlying SiO_2 layer is also lower. This indicates that further phase separation had occurred with annealing at a higher temperature.

The XPS and TEM analyses consistently indicate that the following reaction occurred when the $Hf_{0.5}Si_{0.5}O_2$ film was annealed at high temperatures:

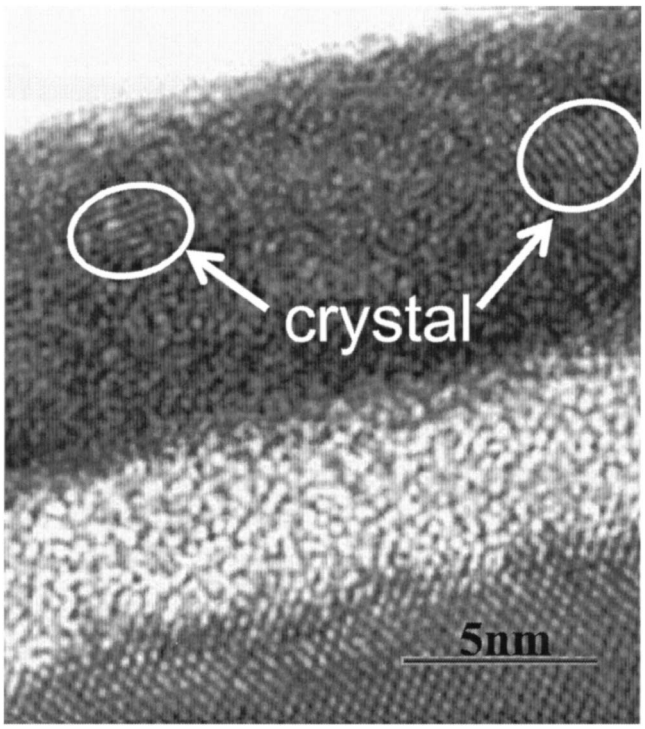

FIG. 3. TEM image of a $SiO_2/Hf_{0.5}Si_{0.5}O_2/SiO_2$ dielectric stack structure that was annealed at 900 °C, revealing the microstructure of crystals embedded in an amorphous matrix.

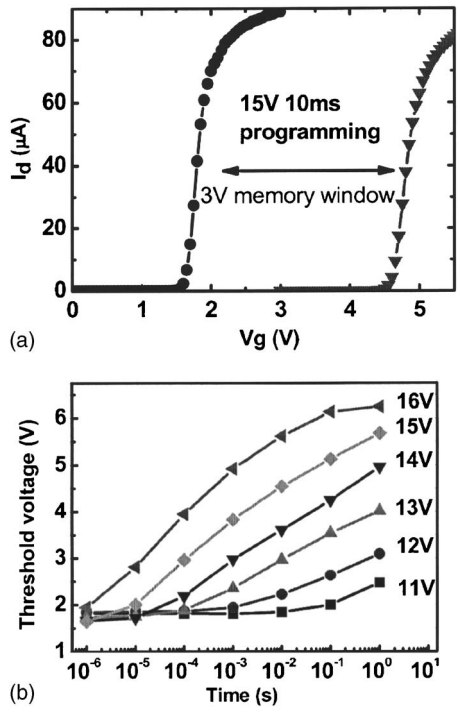

FIG. 4. (a) Memory window and (b) threshold voltage change as a function of programming time and programming voltage of the memory device with the dual-phase $HfO_2-Hf_xSi_{1-x}O_2$ (DPHSO) trapping layer.

$$Hf_{0.5}Si_{0.5}O_2 \rightarrow \frac{0.5-x}{1-x}HfO_2 + \frac{0.5}{1-x}Hf_xSi_{1-x}O_2,$$

where $0<x<0.5$. Lin *et al.* reported a phase separation of $Hf_xSi_{1-x}O_2$ into crystalline HfO_2 and amorphous SiO_2,[9] which can be expressed by $Hf_xSi_{1-x}O_2 \rightarrow xHfO_2+(1-x)SiO_2$, where the $Hf_xSi_{1-x}O_2$ film was in contact with the Si substrate. Their different observations from the results of this work could be due to the different initial material compositions or the different layer structures employed in materials characterization.

IV. MEMORY OPERATION AND RESULTS DISCUSSION

A. Memory effect and programming characteristics

Figure 4(a) shows the memory effect of a MONOS-type device employing $Hf_{0.5}Si_{0.5}O_2$ as a trapping layer. Since the devices underwent a source-drain activation anneal at 1000 °C, the $Hf_{0.5}Si_{0.5}O_2$ film has a DPHSO structure. After applying a positive voltage pulse to the gate electrode while keeping the source, drain, and substrate terminals grounded, the threshold voltage (V_{th}) shifts to a higher value since net negative charge is injected from the Si substrate. The threshold voltage was determined by the intercept of a tangent of the I_d-V_g curve (measured at $V_{ds}=0.2$ V) at the point where the transconductance is the maximum. The threshold voltage as a function of stress time is shown in Fig. 4(b). According to the International Technology Roadmap for Semiconductors (ITRS) 2004,[14] the requirement of memory window for non-volatile flash memory is larger than 3 V. In our device, 3 V can be attained by stressing at 15 V for 10 ms.

The programming properties of the device with the DPHSO trapping layer were compared with devices employing HfO_2 and Si_3N_4 trapping layers. It was found that the devices with DPHSO and HfO_2 trapping layers offer higher programming speeds with lower programming voltages than the device with Si_3N_4 trapping layer.

Figure 1 lists the capacitance effective thickness (t_{eff}), which was calculated using $t_{eff}=A\varepsilon_{ox}/C_{eff}$,[15] where C_{eff} is the capacitance obtained from the capacitance-voltage (C-V) characteristics in the accumulation region, ε_{ox} is the permittivity of SiO_2, and A is the gate area. The t_{eff} of the devices with HfO_2 and DPHSO trapping layers are about the same, but smaller than that of the device with a Si_3N_4 trapping layer. This is partly due to the higher dielectric constants of HfO_2 and $Hf_xSi_{1-x}O_2$. The electric field in the tunneling oxide of the fresh device can be estimated by $E_{ox}=(V_g-V_{fb}-\varphi_s)/t_{eff}$,[15] where E_{ox} is the electric field in the tunnel oxide and V_g, V_{fb}, and φ_s are the applied gate voltage, the flatband voltage, and the surface potential, respectively. Therefore, for a given electric field in the tunneling oxide, the applied gate voltage is smaller for the HfO_2 and DPHSO devices compared to the Si_3N_4 device.

Figure 5 compares the programming properties of the three devices, with a V_g of 14 V applied to the devices with a HfO_2 or DPHSO trapping layer, and 18 V applied to the devices with a Si_3N_4 trapping layer. At this bias condition, the value of E_{ox} is about 10 MV/cm and electrons should be injected from the substrate to the trap layer via Fowler-Nordheim (FN) tunneling, as illustrated in Fig. 6. The FN tunneling current density is given by $J_{FN}=AE_{ox}^2\exp((-B/E_{ox}))$, where E_{ox} is the electric field through the tunneling oxide, and A and B are constants as given by

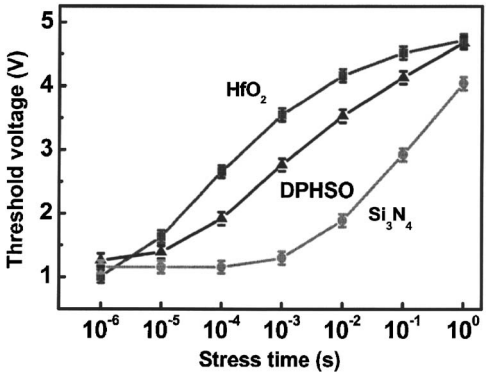

FIG. 5. Comparison among memory devices with dual-phase DPHSO, HfO_2, and Si_3N_4 as trapping layers. An electric field E_{ox} of 10 MV/cm was applied across the tunneling oxide in all three devices. Each data point was obtained by measuring five devices and the error is within 0.1 V across the chip.

$A=q^3(m/m_{ox})/8\pi h\Phi_B$ and $B=8\pi\sqrt{2m_{ox}\Phi_B^3}/3qh$.[16] Hence the tunneling current is only determined by the electric field, and the injection current from substrate to trapping layer should be the same for all the three devices.

The programming speed was determined by $d\Delta V_{th}/dt = \eta J_{inj}/C_g$,[17] where η is the capture efficiency, J_{inj} is the injection current, C_g is the capacitance between a centroid of a trapped charge and the gate, and $C_g=\varepsilon_{ox}/d$, where d is the equivalent oxide thickness (EOT) between the trapped charge and the gate electrode. If the centriod of the trapped charge is in the middle of the trapping layer, the values of d for the devices with DPHSO, HfO_2, and Si_3N_4 trapping layers would be 9.0, 8.8, and 10.9 nm, respectively; thus $C_g(HfO_2)>C_g(DPHSO)>C_g(Si_3N_4)$. As stated before, the injection currents of the three devices are nearly the same in Fig. 5. Therefore, the faster threshold voltage shift $(d\Delta V_{th}/dt)$ of the devices with a HfO_2 or DPHSO trapping layer compared with the device with a Si_3N_4 trapping layer at the early stage of the programming indicates that the HfO_2 and DPHSO films have a higher capture efficiency (η) than Si_3N_4.

B. Retention properties

It is reported that although employing HfO_2 as a trapping layer can lower the programming voltage in comparison with Si_3N_4, the retention property of HfO_2 is poor.[3] The lateral migration of electrons in HfO_2 degrades the retention property, because the grain boundaries can act as lateral conduction paths.[3] In our experiment, we compared the retention properties of the Si_3N_4, HfO_2, and DPHSO films by tracing the flatband voltage (V_{fb}) shift of the programmed device as a function of time. Figure 7 shows the gradual shift of the flatband voltage of the three devices with time. Si_3N_4 shows the best retention. DPHSO retains the charge slightly better than HfO_2, showing a 0.1-V-smaller decay in V_{fb} after 10^5 s. The improvement of DPHSO over HfO_2 is attributed to the presence of the amorphous phase in the film. The amorphous structure does not contain any grain boundaries and could effectively suppress lateral migration of trapped charges.

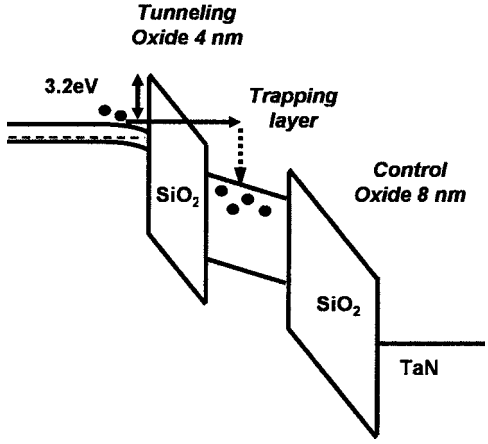

FIG. 6. Energy-band diagram of the MONOS-type device during programming.

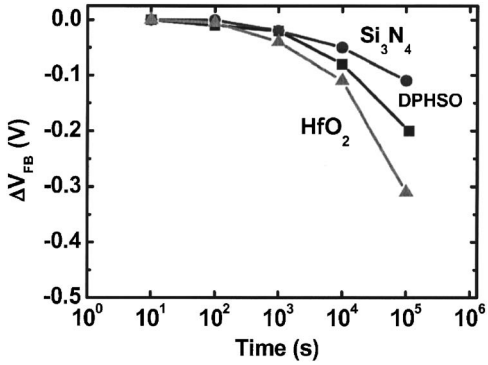

FIG. 7. Retention characteristics of memory devices with Si_3N_4, dual-phase DPHSO, and HfO_2 trapping layers.

V. CONCLUSION

The phase separation of the $Hf_{0.5}Si_{0.5}O_2$ film in the $SiO_2/Hf_{0.5}Si_{0.5}O_2/SiO_2$ sandwich dielectric structure was demonstrated. A dual-phase structure comprising crystalline HfO_2 and amorphous $Hf_xSi_{1-x}O_2$ was observed after the $Hf_{0.5}Si_{0.5}O_2$ film was annealed at 900 and 1000 °C. The $HfO_2-Hf_xSi_{1-x}O_2$ trapping layer was found to provide a faster programming speed at a lower programming voltage than Si_3N_4 because of its higher dielectric constant and higher trap efficiency. Meanwhile, the $HfO_2-Hf_xSi_{1-x}O_2$ also provided better retention property than HfO_2 because the presence of the amorphous phase suppressed the formation of grain boundary effectively, thereby reducing lateral migration. This dual-phase $HfO_2-Hf_xSi_{1-x}O_2$ film with good trapping properties is a promising trapping material for the MONOS-type flash memory application.

ACKNOWLEDGMENTS

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