A New Schmitt Trigger Circuit in a 0.13-μm 1/2.5-V CMOS Process to Receive 3.3-V Input Signals

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***Abstract*—A new Schmitt trigger circuit, which is implemented by low-voltage devices to receive the high-voltage input signals without gate-oxide reliability problem, is proposed. The new proposed circuit, which can be operated in a 3.3-V signal environment without suffering high-voltage gate-oxide overstress, has been fabricated in a 0.13-μm 1/2.5-V 1P8M CMOS process. The experimental results have confirmed that the measured transition threshold voltages of the new proposed Schmitt trigger circuit are about 1 and 2.5 V, respectively. The new proposed Schmitt trigger circuit is suitable for mixed-voltage input–output interfaces to receive input signals and reject input noise.**

***Index Terms*—Gate-oxide reliability, input–output (I/O), mixed-voltage interface, Schmitt trigger.**

I. Introduction

As THE semiconductor process is scaled down, the thickness of gate oxide becomes thinner in order to decrease the core power-supply voltage (VDD) [1]. However, the board voltage (VCC) is still kept as high as 3.3 V (or 5 V), such as PCI-X interface [2]. There are three problems on a MOSFET when the operating voltage is higher than its normal voltage. Higher drain-to-source voltage ($V_{\rm ds}$) may cause the serious hot-carrier effect which results in the long-term lifetime issue [3]. The drain-to-bulk p-n-junction breakdown may occur if the operating voltage is too high. The high-voltage stress across the thinner gate oxide could also destruct the gate oxide [4]. Thus, the mixed-voltage input–output (I/O) circuit must be designed carefully to overcome these problems, especially the high-voltage gate-oxide stress [5]–[8].

The Schmitt trigger circuit has been widely used in the input buffers to increase noise immunity. The conventional input buffer, which consists of a Schmitt trigger and a level-down converter, is shown in Fig. 1. The Schmitt trigger circuit receives input signals from the I/O pad and rejects input noise. Then, the level-down converter can convert the signal swing from VCC to VDD. The circuit and the transfer curve of the conventional Schmitt trigger circuit [9], [10] are shown in Fig. 2. Transistors P1, P2, P3, N1, N2, and N3 in Fig. 2(a) are the I/O devices with the normal operation voltage of VDD. If the board voltage (VCC) is equal to VDD, the gate–drain and gate–source voltages of transistors P1, P2, P3, N1, N2, and N3 in Fig. 2(a) will not exceed VDD. Thus, the conventional Schmitt trigger circuit can be operated without suffering high-voltage gate-oxide overstress. As shown in Fig. 2(b), the conventional Schmitt trigger circuit with different high-to-low and low-to-high transition threshold voltages (V_H and V_L) has better noise immunity than the inverter. When the input signal IN goes up to VCC from GND, the threshold voltage of the conventional Schmitt trigger circuit is V_H. In other words, the output signal OUT is pulled low when the signal IN exceeds the high-to-low threshold voltage (V_H). Similarly, when the input signal IN goes down to GND from VCC, the threshold voltage of the conventional Schmitt trigger circuit is V_L. In other words, the output signal OUT is pulled up when the input signal IN is lower than the low-to-high threshold voltage (V_L). Hence, the noise immunity of the conventional Schmitt trigger circuit is better than that of inverter. The threshold voltages V_H and V_L can be adjusted by controlling the device dimensions of those transistors [11].

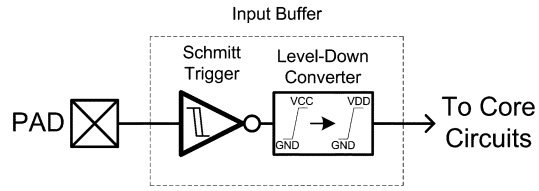

Fig. 1. Conventional input buffer for mixed-voltage I/O interface.

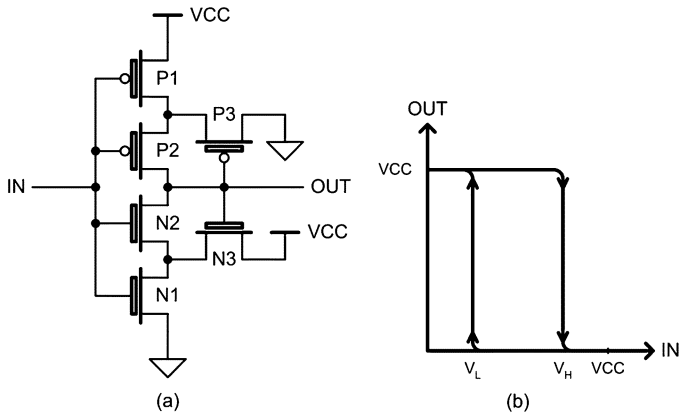

Fig. 2. (a) Circuit. (b) Transfer curve of the conventional Schmitt trigger circuit.

Several modified Schmitt trigger circuits had been reported for different applications [12]–[15]. Fig. 3(a) shows the Schmitt trigger circuit reported in [12]. The extra bias voltage V_B and the extra transistors P4 and N4 are used to adjust the two threshold voltages V_L and V_H. In [13], a multilayer Schmitt trigger circuit was reported to increase the voltage difference between the two threshold voltages V_H and V_L. The two-layer Schmitt trigger circuit is shown in Fig. 3(b). However, as the power-supply

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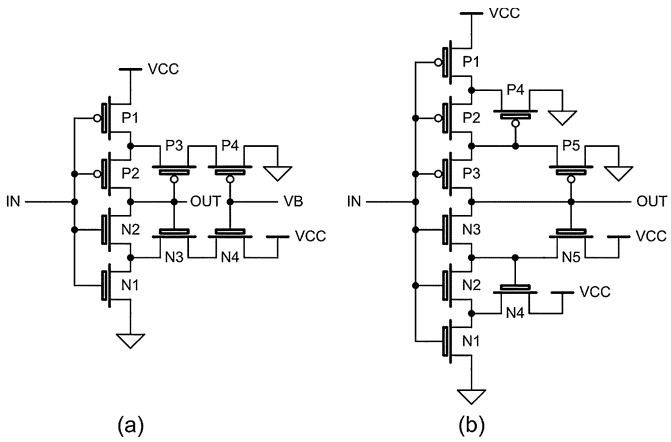

Fig. 3. (a) Schmitt trigger with controllable hysteresis [12]. (b) Two-layer Schmitt trigger [13].

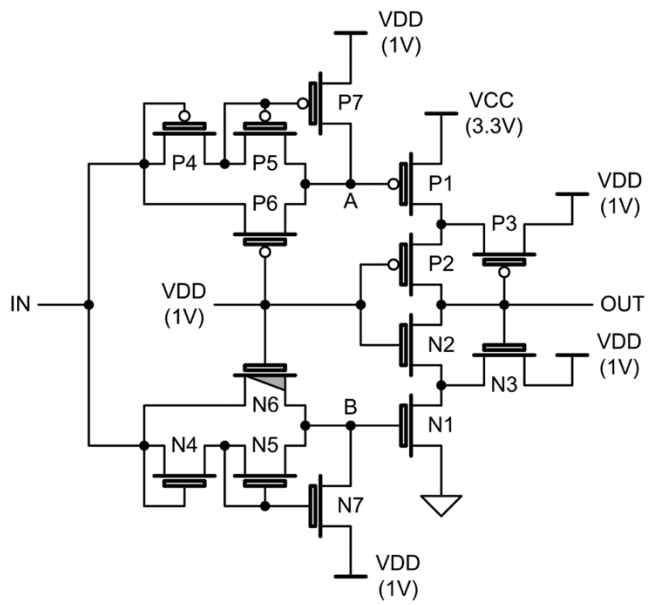

Fig. 4. New proposed Schmitt trigger circuit. (N6 is a native Vt transistor).

voltage is scaled down, the multilayer Schmitt trigger circuit can not be operated correctly. In [14], a low-power Schmitt trigger circuit was reported. An alternative circuit, which has the hysteresis characteristic similar to that of a conventional Schmitt trigger, was reported in [15].

However, the aforementioned Schmitt trigger circuits have high-voltage gate-oxide overstress problem if the board voltage (VCC) is higher than VDD. For example, the digital part of a chip is designed with 1-V devices to decrease its power dissipation, the analog part is designed with 2.5-V devices to improve the circuit performance, and the chip-to-chip interface is 3.3-V PCI-X in a 0.13-μm $1/2.5$-V CMOS process. The gate–source voltages and the gate–drain voltages of transistors P1, P2, P3, N1, N2, and N3 in Fig. 2(a) will be higher than 2.5 V if the board voltage (VCC) is 3.3 V and the I/O devices are 2.5-V devices. Thus, all transistors in Fig. 2(a) will suffer the high-voltage gate-oxide overstress problem. Furthermore, the other Schmitt triggers [12]–[15] also suffer the gate-oxide reliability problem in such a mixed-voltage interface.

In this brief, a new Schmitt trigger circuit constructed with only low-voltage devices is proposed to receive the high-voltage input signals [16]. The new proposed circuit has been successfully verified in a 0.13-μm $1/2.5$-V CMOS process for operating in 3.3-V signal environment without high-voltage gate-oxide overstress problem.

II. New Proposed Schmitt Trigger Circuit

A. Circuit Design

The new proposed Schmitt trigger circuit is shown in Fig. 4. All devices of the proposed Schmitt trigger circuit in Fig. 4 are the I/O devices with the normal operating voltage of 2.5 V. In a 0.13-μm $1/2.5$-V CMOS process, the I/O devices is realized with 2.5-V gate oxide and the core circuits are operated with 1-V power supply. Therefore, the voltage across the gate oxide of the I/O devices in this process can not exceed 2.5 V. As shown in Fig. 4, because the drains of transistors P3 and N3 in Fig. 4 are connected to 1 V (VDD), the gate–drain voltages of transistors P3 and N3 will not exceed 2.5 V. The maximum gate–drain and gate–source voltages of transistors P3 and N3 are around 2.3 V $(3.3 - 1 = 2.3)$. Because the gates of transistors P2 and N2 are connected to 1 V (VDD), the gate–drain voltages and gate–source voltages of transistors P2 and N2 will not exceed 2.5 V. The maximum gate–drain voltages of transistors P2 and N2 are also around 2.3 V $(3.3 - 1 = 2.3)$. If the gate voltage of transistor P1 (node A) is kept higher than 0.8 V $(3.3 - 2.5 = 0.8)$ and the gate voltage of transistor N1 (node B) is kept lower than 2.5 V, transistors P1 and N1 don't have the high-voltage gate-oxide overstress problem. Hence, in order to prevent the gate voltage of transistor P1 under 0.8 V, transistors P4, P5, P6, and P7 are added. Similarly, transistors N4, N5, N6, and N7 are designed to prevent the gate voltage of transistor N1 over 2.5 V.

When the input signal (IN) stays at 3.3 V (VCC), the voltage on node A is also kept at 3.3 V because transistor P6 is turned on. When the input signal (IN) goes to 0 V, the voltage on node A is kept at $2 \cdot |V_{\rm tp}|$ because transistors P4 and P5 are in diode-connected structure. In the 0.13-μm $1/2.5$-V CMOS process, $|{\rm Vtp}|$ of 2.5-V device is about 0.6 V. Therefore, the minimum gate voltage of transistor P1 (node A) is about 1.2 V. However, the diode-connected transistors P5 and P6 may make the voltage on node A to 0 V when the input signal (IN) stays at 0 V for a long time, because of the subthreshold current of transistors P5 and P6. An extra transistor P7 is added to avoid the voltage on node A under 1 V caused by the subthreshold current of transistors P5 and P6. Hence, as the voltage on node A is under 1 V, transistor P7 will be turned on to keep the voltage at 1 V.

When the input signal (IN) stays at 0 V, the voltage on node B is kept at 0 V because transistor N6 is turned on. When the input signal (IN) goes to 3.3 V, the voltage on node B is kept at $3.3 - 2 \cdot |V_{\rm tn}|$, because transistors N4 and N5 are in diode-connected structure. In the 0.13-μm $1/2.5$-V CMOS process, $|V_{\rm tn}|$ of 2.5-V device is about 0.5 V. Therefore, the maximum gate voltage of transistor N1 (node B) is about 2.3 V. However, the diode-connected transistors N5 and N6 may make the voltage on node B to 3.3 V, when the input signal (IN) stays at 3.3 V for a long time, due to the subthreshold current of transistors N5 and N6. Hence, a weak transistor (long-channel transistor)

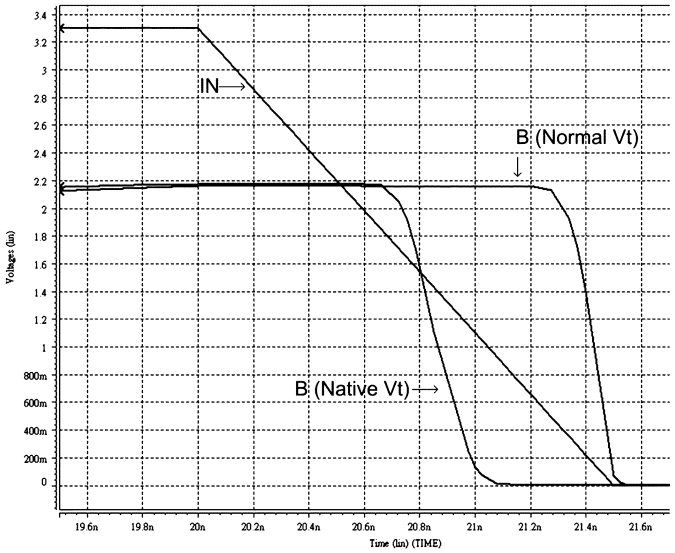

Fig. 5. Simulated waveforms at the nodes IN and B to compare the pull-down speed on the node B, when the transistor N6 is implemented by a native V_t device or a normal V_t device.

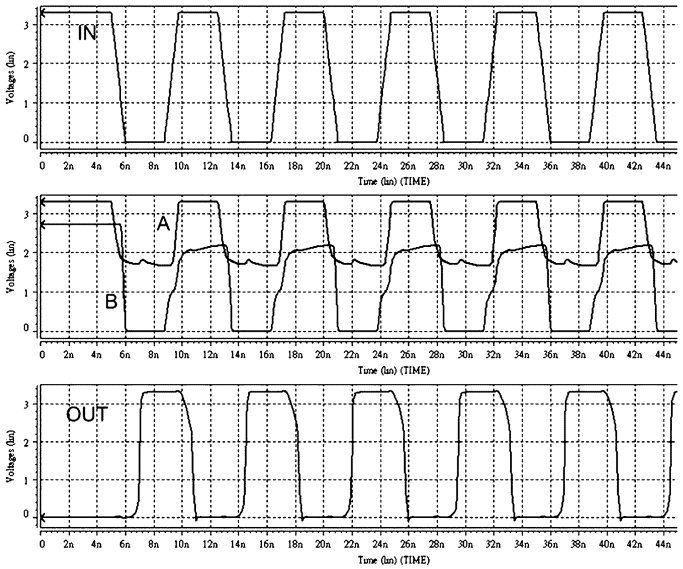

Fig. 6. Simulated waveforms at the nodes IN, OUT, A, and B of the new proposed Schmitt trigger circuit operating at 133 MHz.

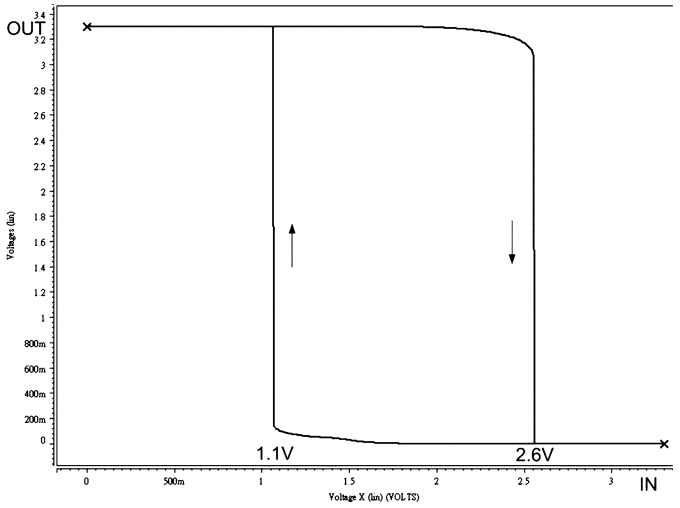

Fig. 7. Simulated transfer curve of the new proposed Schmitt trigger circuit.

N7 is added to avoid the voltage on node B over 2.5 V caused by the subthreshold current of transistors N5 and N6. If node B goes to 3.3 V, transistor N7 provides a small current to keep the gate voltage of transistor N1 under 2.5 V.

In addition, transistor N6 in Fig. 4 can be a 2.5-V native V_t transistor instead of a 2.5-V normal V_t transistor. The threshold voltage of the native V_t transistor is close to 0 V, which is lower than that of the normal V_t transistor [17], [18]. In the 0.13-μm $1/2.5$-V CMOS process, the threshold voltage of the 2.5-V native V_t transistor is about 0.03 V. Because the gate–source voltage of transistor N6 is small, the voltage on node B follows input signal IN to 0 V slowly. Thus, a native V_t transistor is more suitable than a normal V_t transistor to implement the transistor N6 for high-speed applications. Because the native V_t device has been one of the standard devices in a 0.13-μm $1/2.5$-V CMOS process, no extra process or mask is needed [18]. Fig. 5 compares the voltage waveforms at node B when transistor N6 is a native Vt transistor or a normal Vt transistor in the 0.13-μm $1/2.5$-V CMOS process. As shown in Fig. 5, the voltage on node B is pulled down more quickly when transistor N6 is implemented by a native V_t transistor.

B. Simulations

A 0.13-μm $1/2.5$-V CMOS SPICE model is used to simulate the new proposed Schmitt trigger circuit. The simulated waveforms at the nodes IN, OUT, A, and B of the new proposed Schmitt trigger circuit are shown in Fig. 6. The input signal can be correctly translated to the output by the proposed Schmitt trigger circuit. Besides, the voltage level at node A is indeed kept higher than 0.8 V, and that of node B is kept lower than 2.5 V. Therefore, transistors P1 and N1 of the proposed Schmitt trigger circuit don't suffer high-voltage gate-oxide reliability issue in a 3.3-V environment. Besides, the $V_{\rm gs}$ and $V_{\rm gd}$ of all devices are not over 2.5 V. The $V_{\rm ds}$ of all devices are also not over 2.5 V when the input signal is high or low. Hence, the new proposed Schmitt trigger circuit can receive the high-voltage input signals without suffering gate-oxide reliability and hot-carrier issues, whereas it is realized by only using the low-voltage devices with thin gate oxide.

The simulated transfer curve of the new proposed Schmitt trigger circuit is shown in Fig. 7. The new proposed Schmitt trigger circuit has an obvious hysteresis characteristic. In this simulation, the transition threshold voltages V_L and V_H of the new proposed Schmitt trigger circuit are around 1.1 and 2.6 V, respectively.

III. Experimental Results

The new proposed Schmitt trigger circuit has been fabricated in a 0.13-μm $1/2.5$-V 1P8M CMOS process. The layout of the new proposed Schmitt trigger circuit is shown in Fig. 8. Because the proposed Schmitt trigger circuit is connected to an input pad, some guard rings surrounding the whole Schmitt trigger circuit are used to prevent the latch-up problem [19]. The layout area of the new proposed Schmitt trigger circuit including the guard rings is only 8.7 μm $\times$ 19 μm. A whole input buffer shown

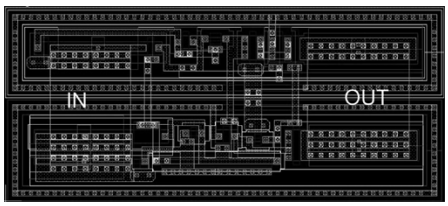

Fig. 8. Layout of new proposed Schmitt trigger circuit.

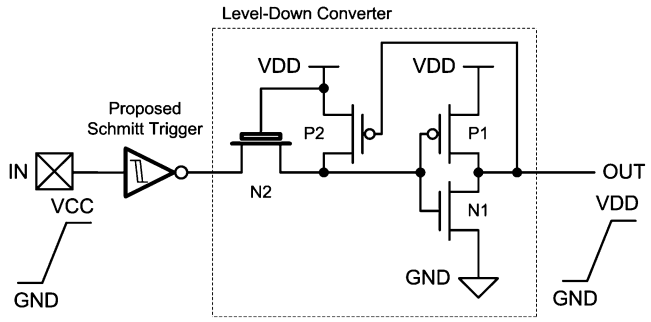

Fig. 9. Whole input buffer with the proposed Schmitt trigger and level-down converter.

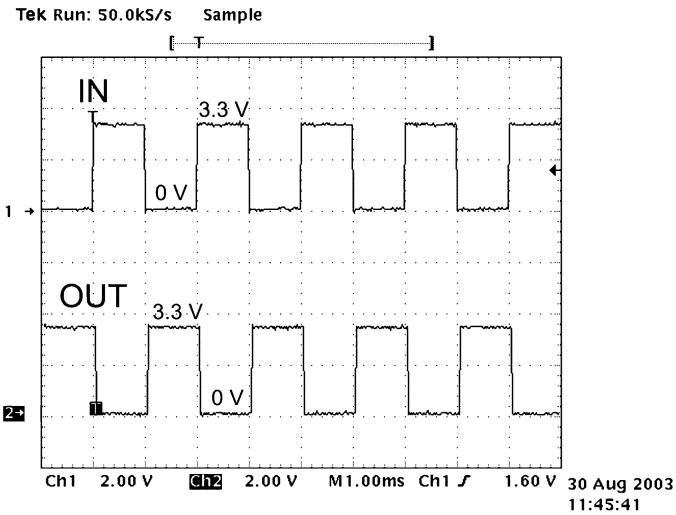

Fig. 10. Measured waveforms of the new proposed Schmitt trigger circuit.

in Fig. 9, which is consisted with the new proposed Schmitt trigger and a level-down converter, has been fabricated in the 0.13-μm CMOS process. In the level-down converter, transistor N2 is a 2.5-V device and transistors P1, P2, and N1 are 1-V devices, which can convert 3.3-V signals to become 1-V signals for internal circuits.

The measured waveforms at the input node and the output node of the new proposed Schmitt trigger circuit are shown in Fig. 10. The new proposed Schmitt trigger can operate correctly with 0-to-3.3-V input signals. In Fig. 11, the input signal is applied with a slow triangular waveform. Therefore, the transition threshold voltages V_L and V_H of the new proposed Schmitt trigger circuit can be measured at the crossing points between the input signal and output signal. The measured dc transfer curve of the new proposed Schmitt trigger circuit is shown in Fig. 12. These two transition threshold voltages V_L and V_H of the fabricated Schmitt trigger circuit are around 1 and 2.5 V, respectively. Due to the process variation, the measured transition

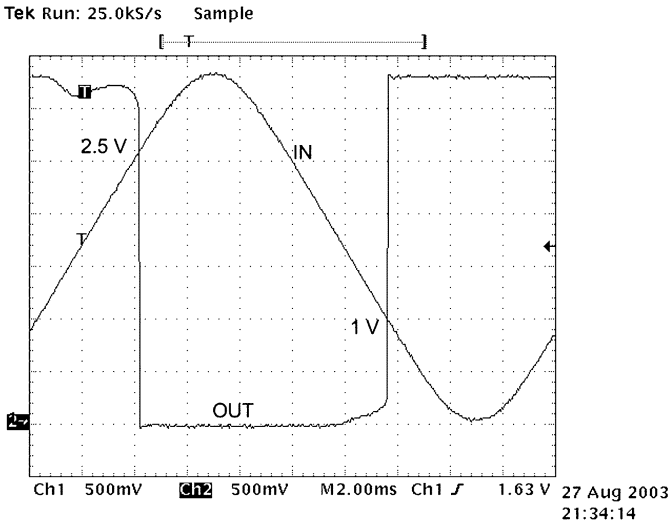

Fig. 11. Measured transition threshold voltages V_L and V_H of the new proposed Schmitt trigger circuit.

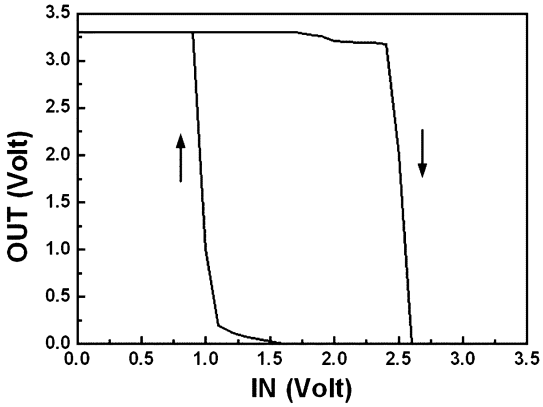

Fig. 12. Measured transfer curve of the new proposed Schmitt trigger circuit.

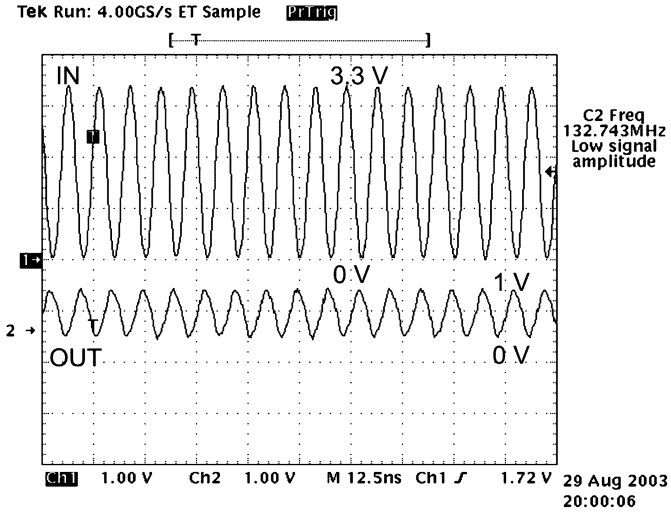

Fig. 13. Measured waveforms at the nodes IN and OUT of the whole input buffer with a 133-MHz 3.3-V PCI-X input signal.

threshold voltages are slightly different from the simulated transition threshold voltages.

The measured waveforms at the nodes IN and OUT of the whole input buffer are shown in Fig. 13 with a 133-MHz 3.3-V PCI-X input signal. The 3.3-V input signal is received by the

proposed Schmitt trigger circuit, and then the signal swing is converted from 3.3 to 1 V by the level-down converter. As shown in Fig. 13, the input buffer can be successfully operated in the 133-MHz 3.3-V PCI-X environment.

IV. Conclusion

A new Schmitt trigger circuit realized with only low-voltage devices to receive the high-voltage signals is proposed. The new Schmitt trigger circuit has been fabricated in a 0.13-μm $1/2.5$-V 1P8M CMOS process. The proposed Schmitt trigger circuit, which consists of low-voltage (2.5 V) devices, can be operated correctly without suffering high-voltage gate-oxide overstress in a 3.3-V interface environment. The measured results have shown that the two transition threshold voltages V_L and V_H of the new proposed Schmitt trigger are 1 and 2.5 V, respectively. The whole input buffer, which is consisted with the proposed Schmitt trigger and a level-down converter, has been verified to be successfully operated in the 133-MHz 3.3-V PCI-X environment. The new proposed Schmitt trigger circuit is suitable to reject noise for mixed-voltage interface applications in the future nanoscale CMOS processes.

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