

Low Noise RF MOSFETs on Flexible Plastic Substrates

H. L. Kao, Albert Chin, *Senior Member, IEEE*, B. F. Hung, C. F. Lee, J. M. Lai, S. P. McAlister, *Senior Member, IEEE*, G. S. Samudra, Won Jong Yoo, *Senior Member, IEEE*, and C. C. Chi

Abstract—We report a low minimum noise figure (NF_{\min}) of 1.1 dB and high associated gain (12 dB at 10 GHz) for 16 gate-finger 0.18- μm RF MOSFETs, after thinning down the Si substrate to 30 μm and mounting it on plastic. The device performance was improved by flexing the substrate to create stress, which produced a 25% enhancement of the saturation drain current and lowered NF_{\min} to 0.92 dB at 10 GHz. These excellent results for mechanically strained RF MOSFETs on plastic compare well with 0.13- μm node ($L_g = 80$ nm) devices.

Index Terms—Associated gain, MOSFET, plastic, RF noise.

I. INTRODUCTION

Si RF MOSFETs [1]–[8] are widely used for wireless communications, due to the continuous improvements in their RF noise and high-frequency gain, associated with the down-scaling of the technology. A major challenge for Si RF ICs is the RF loss from the low resistivity ($10 \Omega \cdot \text{cm}$) Si substrate [9]–[11] which substantially degrades the performance of passive components. One solution is to integrate the Si RF ICs on highly insulating plastic [12], since high-performance RF passive devices can be realized on the low-cost plastic substrate. Furthermore the passive devices often consume a large area of a processed Si wafer, which is not cost effective. Plastic substrates are also flexible. In this letter, we have applied tensile strain to improve the RF performance of Si MOSFETs. This was done by thinning the Si substrate to 30 μm and mounting it on plastic, which could be flexed to create strain. By applying a $\sim 0.7\%$ longitudinal tensile strain the min. noise figure (NF_{\min}) improved from 1.1 to 0.92 dB while the associated gain increased from 11 to 14 dB. These performance improvements result from the 25% higher saturation drive current under tensile strain [13], [14]. The excellent RF performance of the strained plastic-mounted devices compares well with 0.13 μm node devices ($L_g = 80$ nm) [5],

Manuscript received March 3, 2005; revised April 18, 2005. This work was supported in part by the National Research Council (NRC), Ottawa, Canada and the National Science Council of Taiwan, R.O.C., under Grant 93-2215-E-009-001. The review of this letter was arranged by Editor K. De Meyer.

H. L. Kao, A. Chin, B. F. Hung, C. F. Lee, and J. M. Lai are with the Nano-Science Technology Center, Department of Electronics Engineering, National Chiao-Tung University, Hsinchu 300, Taiwan, R.O.C.

A. Chin, G. S. Samudra, and W. J. Yoo are with the Silicon Nano Device Laboratory, Department of Electrical and Computer Engineering, National University of Singapore, Singapore, 119260, on leave from Nano-Science Technology Center, Department of Electronics Engineering, National Chiao-Tung University, Hsinchu 300, Taiwan, R.O.C. (e-mail: albert_achin@hotmail.com).

S. P. McAlister is with the National Research Council of Canada, Ottawa, ON, Canada.

C. C. Chi is with the Department of Physics, National Tsing-Hua University, Hsinchu 300, Taiwan, R.O.C.

Digital Object Identifier 10.1109/LED.2005.851238

[6] giving a full technology generation advantage, and shows the advantage of low-cost thin-Si body flexible electronics on plastic.

II. EXPERIMENTAL DETAILS

Multiple-gate 0.18 μm MOSFETs [5]–[7], [10], [11] with a novel microstrip line layout were used [8], which have gate oxide and poly Si thickness of 4.0 and 200 nm, respectively. The microstrip line layout used Metal-1 as the ground plane of transmission line [8], which can shield the substrate-resistance-generated noise from the RF probing pads and transmission line body in comparing with conventional coplanar waveguide (CPW) transmission line case [5]–[7]. Therefore, the NF_{\min} can be directly measured without complicated de-embedded procedure. To improve the performance we thinned the Si substrate from standard 300 to 30 μm using inductive-coupled plasma (ICP) dry etching followed by a wet etching process. The thinned die was then glued onto a light-transparent polyethylene terephthalate (PET) plastic substrate as in Fig. 1(a) and (b), where high adhesive glue was used without thermal annealing. We have also fabricated a transmission line to measure the RF loss of high insulating PET, which is 0.5 dB/mm at 30 GHz. Fig. 1(c) shows the flexibility of the 30- μm -thick Si substrate under large surface tensile strain. The devices were characterized by dc I - V , S -parameters and NF_{\min} measurements by an HP4155C, HP8510C network analyzer and ATN-NP5B noise parameter system, respectively. Note that we can not measure the device under compressive strain due to the downward curvature and poor contact with probe.

III. RESULTS AND DISCUSSION

Fig. 2 shows the dc I_d - V_d characteristics of 16 gate-finger 0.18 μm RF MOSFETs on a very large-scale integrated (VLSI) standard substrate, on a substrate thinned down to 30 μm and The process of thinning down the Si substrate and mounting it on plastic produces little degradation of the device performance, as indicated by the comparable I_d - V_d characteristics. The saturation drive current was increased by 25%, by applying longitudinal tensile strain of $\sim 0.7\%$. This drive current improvement can be useful in achieving higher operation frequencies in ICs, and provides an alternative method to apply the strain to enhance the device performance, rather than by using SiN-capped strained-Si [4].

Fig. 3 shows the RF current gain ($|H_{21}|^2$) as a function of frequency for the 16 gate-finger 0.18 μm MOSFETs, where the

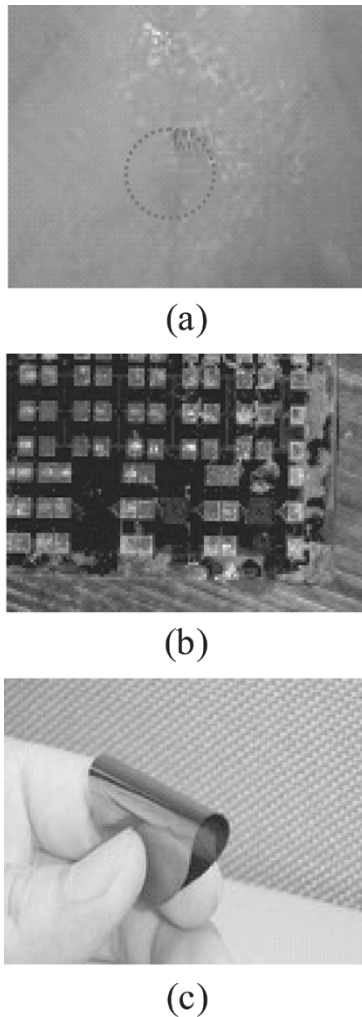


Fig. 1. (a) Image of the fabricated die of RF MOSFETs with $30\text{-}\mu\text{m}$ Si substrate thickness on light-transparent plastic (hold by a hand in the background), (b) enlarged image of the fabricated die on light-transparent plastic shown in (a) and put on a table (Background is the surface of a wooden table.), and (c) a control $\sim 30\text{-}\mu\text{m}$ -thick Si substrate with high flexibility and large surface strain.

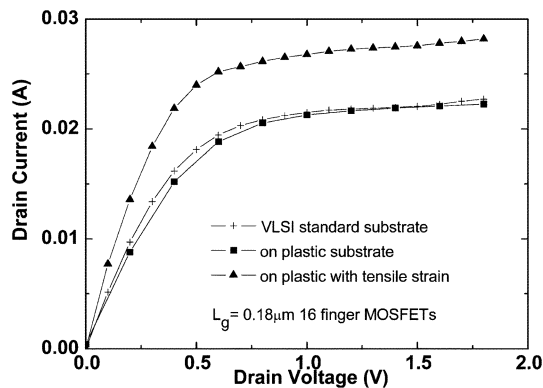


Fig. 2. Measured dc I_d - V_d characteristics of 16-finger $0.18\ \mu\text{m}$ RF MOSFETs on VLSI-standard substrates, on substrates thinned down and mounting on plastic, and for the latter under mechanical tensile strain.

data follow the typical $-20\ \text{dB/dec}$ slope with increasing frequency. The data for the devices on plastic are only marginally different from those on the standard thick substrate, with the unity gain cutoff frequency (f_T) decreasing from 48.5 to 48.0

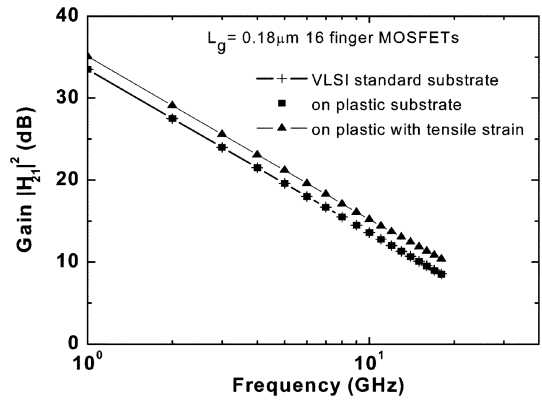


Fig. 3. Gain ($|H_{21}|^2$) versus frequency for the 16-finger $0.18\text{-}\mu\text{m}$ RF MOSFETs on VLSI-standard Si substrates, on plastic and under mechanical strain. The $|H_{21}|^2$ of the device on plastic almost overlaps that for the reference devices.

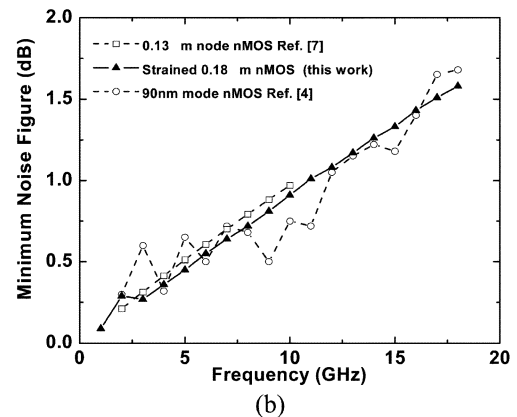
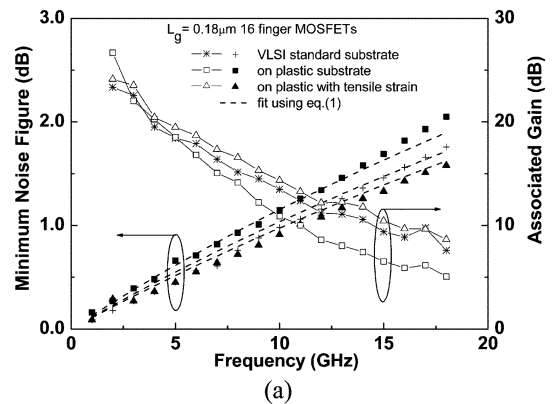


Fig. 4. (a) Minimum noise figure (NF_{\min}) and the associated gain for the reference devices, those mounted on plastic and the latter under mechanical strain. (b) Comparison of published NF_{\min} data of $0.13\text{-}\mu\text{m}$ and SiN-strained 90-nm node MOSFETs with a mechanically strained $0.18\text{-}\mu\text{m}$ MOSFET on plastic of this work.

GHz. The data for the tensile-strained RF MOSFETs on plastic also follows a $-20\ \text{dB/dec}$ slope, and yields a gain enhancement of $1.6\ \text{dB}$ at $10\ \text{GHz}$, and a higher f_T of $59\ \text{GHz}$. These improvements of the RF current gain and f_T are consistent with the higher saturation current arising from the strain-enhanced mobility.

Fig. 4(a) shows the NF_{\min} and associated gain. At $10\ \text{GHz}$ useful for ultrawide band (UWB), NF_{\min} of the reference devices and those on plastic are almost identical (1.0 compared

with 1.1 dB) and the associated gains are 13.5 dB and 11 dB, respectively. The slight degradation of NF_{\min} may be due to damage created by the ICP plasma-thinning process. These data suggest that the RF noise and associated gain are more sensitive to substrate engineering, through the thinning process, than are the dc characteristics. For the mechanically strained 0.18 μm MOSFETs on plastic, a low NF_{\min} of 0.92 dB and high associated gain of 14 dB was obtained at 10 GHz. This RF noise improvement arises from the higher f_T [7], as described by

$$NF_{\min} = 1 + 2\gamma \sqrt{\frac{1 + g_m R_g}{\gamma} \frac{f}{f_T}}. \quad (1)$$

Here, γ is the drain current noise correlation factor and the ideal value of 2/3 was used here to fit the measured NF_{\min} , as shown in Fig. 4(a). The excellent results shown by the tensile-strained RF MOSFETs on plastic compare well with 0.13- μm node ($L_g = 80$ nm) [5]–[7] and 90-nm node SiN-capped strained nMOS [4] devices, as shown in Fig. 4(b). The low-cost and high-performance 0.18- μm RF MOSFETs on plastic are potentially advantageous for flexible electronics and also important for RFID and wireless display applications.

IV. CONCLUSION

We have successfully demonstrated high RF performance 0.18- μm MOSFETs on 30- μm Si substrates mounted on flexible plastic. Excellent RF performance, such as a low 0.92 dB NF_{\min} , high 14 dB associated gain and high 59 GHz f_T were obtained when the devices were subjected to tensile strain.

ACKNOWLEDGMENT

The authors would like to thank G. W. Huang at the National Nano-Device Lab for his help with the RF measurements.

REFERENCES

- [1] C. H. Chen and M. J. Deen, "A general noise and S-parameter de-embedding procedure for on-wafer high-frequency noise measurements of MOSFETs," *IEEE Trans. Microw. Theory Tech.*, vol. 49, no. 5, pp. 1004–1005, May 2001.
- [2] N. Zamdmer, A. Ray, J.-O. Plouchart, L. Wagner, N. Fong, K. A. Jenkins, W. Jin, P. Smeys, I. Yang, G. Shahidi, and F. Assaderaghi, "A 0.13- μm SOI CMOS technology for low-power digital and RF applications," in *Symp. VLSI Tech. Dig.*, 2001, pp. 85–86.
- [3] R. E. Belford, W. Zhao, J. Potashnik, Q. Liu, and A. Seabaugh, "Performance-augmented CMOS using back-end uniaxial strain," in *Proc. Device Research Conf. Dig.*, Jun. 2002, pp. 41–42.
- [4] K. Kuhn, R. Basco, D. Becher, M. Hattendorf, P. Packan, I. Post, P. Vandervoorn, and I. Young, "A comparison of state-of-the-art nMOS and SiGe HBT devices for analog/mixed-signal/RF circuit applications," in *Symp. VLSI Tech. Dig.*, 2004, pp. 224–225.
- [5] C. H. Huang, K. T. Chan, C. Y. Chen, A. Chin, G. W. Huang, C. Tseng, V. Liang, J. K. Chen, and S. C. Chien, "The minimum noise figure and mechanism as scaling RF MOSFETs from 0.18 to 0.13 μm technology nodes," in *Proc. IEEE RFIC Symp.*, 2003, pp. 373–376.
- [6] M. C. King, M. T. Yang, C. W. Kuo, Y. Chang, and A. Chin, "RF noise scaling trend of MOSFETs from 0.5 μm to 0.13 μm technology nodes," in *Proc. IEEE MTT-S Dig.*, 2004, pp. 6–11.
- [7] M. C. King, Z. M. Lai, C. H. Huang, C. F. Lee, M. W. Ma, C. M. Huang, Y. Chang, and A. Chin, "Modeling finger number dependence on RF noise to 10 GHz in 0.13 μm node MOSFETs with 80 nm gate length," in *Proc. IEEE RFIC Symp.*, 2004, pp. 171–174.
- [8] H. L. Kao, A. Chin, J. M. Lai, C. F. Lee, K. C. Chiang, and S. P. McAlister, "Modeling RF MOSFETs after electrical stress using low-noise microstrip line layout," in *Proc. IEEE RFIC Symp.*, Jun. 2005.
- [9] R. Dekker, K. Dessein, J.-H. Fock, A. Gakis, C. Jonville, O. M. Kuijken, T. M. Michielsen, P. Mijlemans, H. Pohlmann, W. Schnitt, C. E. Timmering, and A. M. H. Tombeur, "Substrate transfer: Enabling technology for RF applications," in *IEDM Tech. Dig.*, 2003, pp. 371–374.
- [10] A. Chin, K. T. Chan, H. C. Huang, C. Chen, V. Liang, J. K. Chen, S. C. Chien, S. W. Sun, D. S. Duh, W. J. Lin, C. Zhu, M.-F. Li, S. P. McAlister, and D. L. Kwong, "RF passive devices on Si with excellent performance close to ideal devices designed by electro-magnetic simulation," in *IEDM Tech. Dig.*, 2003, pp. 375–378.
- [11] K. T. Chan, A. Chin, Y. B. Chen, Y.-D. Lin, D. T. S. Duh, and W. J. Lin, "Integrated antennas on Si, proton-implanted Si and Si-on-Quartz," in *IEDM Tech. Dig.*, 2001, pp. 903–906.
- [12] T. Takayama, Y. Ohno, Y. Goto, A. Machida, M. Fujita, J. Maruyama, K. Kato, J. Koyama, and S. Yamazaki, "A CPU on a plastic film substrate," in *Symp. VLSI Tech. Dig.*, 2004, pp. 230–231.
- [13] W. Zhao, J. He, R. E. Belford, L.-E. Wernersson, and A. Seabaugh, "Partially depleted SOI MOSFETs under uniaxial tensile strain," *IEEE Trans. Electron Devices*, vol. 54, no. 3, pp. 317–323, Mar. 2004.
- [14] Y. G. Wang, D. B. Scott, J. Wu, J. L. Waller, J. Hu, K. Liu, and V. Ukraintsev, "Effects of uniaxial mechanical stress on drive current of 0.13 μm MOSFETs," *IEEE Trans. Electron Devices*, vol. 54, no. 2, pp. 529–531, Feb. 2004.