

# High- $\kappa$ Ir/TiTaO/TaN Capacitors Suitable for Analog IC Applications

K. C. Chiang, C. C. Huang, Albert Chin, *Senior Member, IEEE*, W. J. Chen, S. P. McAlister, *Senior Member, IEEE*, H. F. Chiu, Jiann-Ruey Chen, and C. C. Chi

**Abstract**—We have developed novel high- $\kappa$  Ir/TiTaO/TaN capacitors which have high-capacitance density ( $10.3 \text{ fF}/\mu\text{m}^2$ ), small leakage current at 2 V ( $1.2 \times 10^{-8} \text{ A}/\text{cm}^2$ ), and low voltage linearity of the capacitance ( $89 \text{ ppm}/\text{V}^2$ ). These excellent results meet the ITRS roadmap requirements for precision analog capacitors for the year 2018. The good performance is due to the very high  $\kappa$  (45) achieved in the TiTaO dielectric and the high work-function (5.2 eV) provided by the Ir electrode.

**Index Terms**—TiTaO, Ir, MIM, analog, ITRS.

## I. INTRODUCTION

TO ACHIEVE continuing improvements in mixed signal and RF IC performance, the sizes of both the active MOSFETs and the passive MIM capacitors [1]–[16] need to be scaled down. The technology challenge for the MIM capacitor is to achieve high capacitance density, low leakage current and small voltage linearity of the capacitance simultaneously [17]. To meet these device requirements, the use of high- $\kappa$  dielectrics for the MIM capacitors is the only viable choice. This is because decreasing the dielectric thickness ( $t_d$ ) needed for high capacitance density ( $\epsilon_0\kappa/t_d$ ) increases the leakage current and degrades the capacitor's voltage linearity. In this paper, we report novel Ir/TiTaO/TaN capacitors which show high-capacitance density, small leakage current, and low voltage linearity, simultaneously. The TiTaO dielectric capacitors also show good thermal stability, such as low leakage current after a 400 °C thermal cycle associated with its backend process. This contrasts with TiO<sub>2</sub> dielectric capacitors which give high leakage current after 400 °C processing [16]. The excellent device performance arises from using the very high- $\kappa$  TiTaO dielectric ( $\kappa = 45$ ) and high work-function Ir (5.2 eV). These are the first results that meet all the ITRS roadmap requirements

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K. C. Chiang, C. C. Huang, and A. Chin are with the Department of Electronics Engineering, Nano Science Technology Center, National Chiao-Tung University, Hsinchu 300, Taiwan, R.O.C.

A. Chin is with the Department of Electrical and Computer Engineering, National University of Singapore, Singapore, on leave from National Chiao-Tung University, Hsinchu 300, Taiwan, R.O.C. (e-mail: albert\_achin@hotmail.com).

W. J. Chen is with the Graduate Institute of Materials Engineering, National Pingtung University of Science and Technology, Taiwan, R.O.C.

S. P. McAlister is with the National Research Council of Canada, Ottawa, ON, Canada.

H. F. Chiu and J.-R. Chen are with the Department of Materials Engineering, National Tsing-Hua University, Hsinchu 300, Taiwan, R.O.C.

C. C. Chi is with the Department of Physics, National Tsing Hua University, Hsinchu 300, Taiwan, R.O.C.

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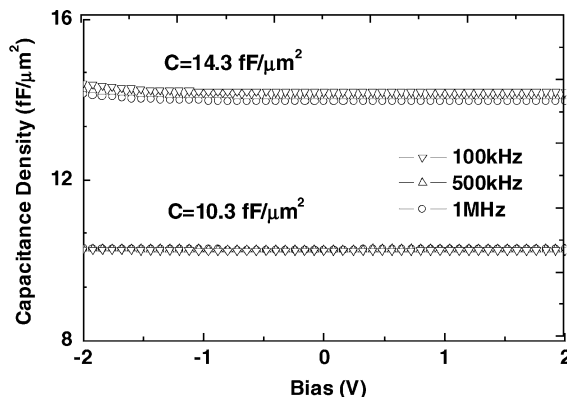


Fig. 1.  $C$ - $V$  characteristics of Ir/TiTaO/TaN TiTaO MIM capacitors.

for analog capacitors in the year 2018— $10 \text{ fF}/\mu\text{m}^2$  capacitance density, leakage current  $<5.8 \text{ fA}/[\text{pF}\cdot\text{V}]$ , and capacitance voltage linearity  $<100 \text{ ppm}/\text{V}^2$  [17].

## II. EXPERIMENTAL PROCEDURE

After depositing  $2\text{-}\mu\text{m}$  SiO<sub>2</sub> on a Si wafer, the lower capacitor electrode was formed using sputter-deposited TaN (50 nm)/Ta (150 nm) bilayers. The Ta was used to reduce the series resistance of TaN ( $3\text{-m}\Omega\text{-cm}$  resistivity). The TaN is needed to serve as a barrier layer between the high- $\kappa$  TiTaO and the Ta electrode. If TaN is too thin, the underneath Ta will be oxidized to form isolating TaO dielectric; if too thick, the series resistance will increase. An isolation SiO<sub>2</sub> was deposited by PECVD and patterned by RIE etching to define the capacitor, with size of  $20 \mu\text{m} \times 20 \mu\text{m}$ . Then Ti<sub>x</sub>Ta<sub>1-x</sub>O ( $x \sim 0.6$ ) dielectric was deposited by PVD, followed by a 400 °C oxidation and 0.5-h annealing step at oxygen ambient to reduce the leakage current. Different TiTaO thicknesses of 41 and 28 nm were used to study the voltage linearity in the devices. Finally, Ir (30 nm) was deposited and patterned by liftoff process to form the top capacitor electrode, although it can be etched by RIE too. The using Ir has additional merit; low resistivity ( $50 \mu\Omega\text{-cm}$ ) is still obtained even annealing under oxygen ambient to form IrO<sub>2</sub> [18]. No mechanical stress caused peering was found for this capacitor. The fabricated devices were characterized by  $C$ - $V$  and  $J$ - $V$  measurements.

## III. RESULTS AND DISCUSSION

Fig. 1 shows the  $C$ - $V$  characteristics of high- $\kappa$  Ir/TiTaO/TaN MIM capacitors. Capacitance densities of  $10.3$  and  $14.3 \text{ fF}/\mu\text{m}^2$  were measured for the 41 and 28 nm TiTaO dielectric devices,

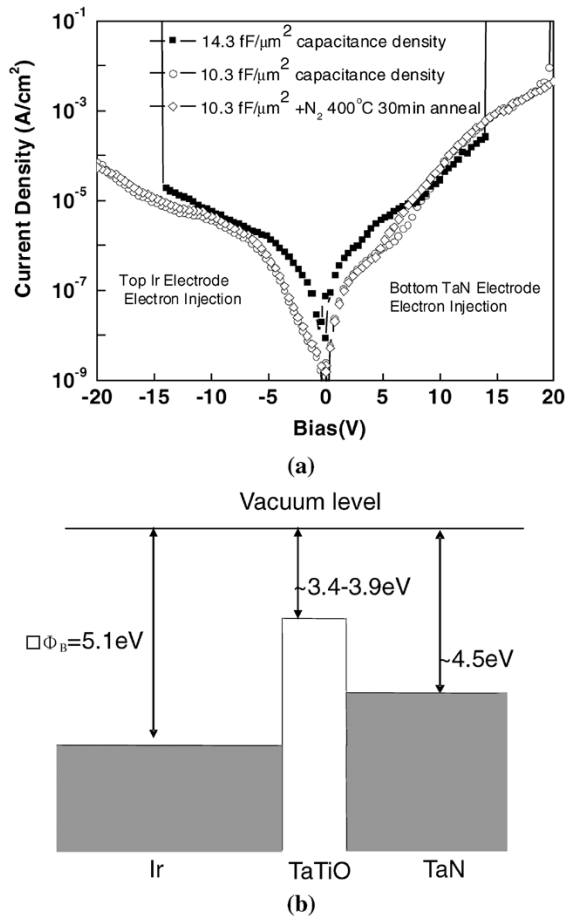


Fig. 2. (a)  $J$ - $V$  characteristics of Ir/TiTaO/TaN MIM capacitors. (b) Band diagram of the Ir/TiTaO/TaN MIM structure. The leakage current is lower when electrons are injected from the top Ir electrode than from the lower TaN electrode.

which give capacitance-equivalent thicknesses (CET) of 3.4 and 2.4 nm, respectively. A high- $\kappa$  value of  $\sim 45$  was obtained from the measured capacitance density in the TiTaO dielectric. The ITRS requirement for analog capacitors, by 2018, is a density of  $10 \text{ fF}/\mu\text{m}^2$ , along with low leakage current and capacitance voltage linearity.

Fig. 2(a) shows the  $J$ - $V$  characteristics of Ir/TiTaO/TaN MIM capacitors with 3.4 and 2.4 nm CET. High breakdown voltages of 14 and 20 V were measured for the 10.3 and 14.3  $\text{fF}/\mu\text{m}^2$  density device, well above values required for most analog function applications. The lower leakage current for electrons injected from the top Ir electrode, compared with the lower TaN electrode, is due to the higher work-function of Ir compared with TaN, as shown in the energy band diagram in Fig. 2(b). The low leakage current of  $1.2 \times 10^{-8} \text{ A}/\text{cm}^2$  at 2 V, or 5.8  $\text{fA}/[\text{pF}\cdot\text{V}]$ , obtained for the 10.3  $\text{fF}/\mu\text{m}^2$  density device, meets the ITRS-required low leakage current of  $< 7 \text{ fA}/[\text{pF}\cdot\text{V}]$  [17]. Such a low leakage current is due to the amorphous structure of the TiTaO being preserved, even after the backend processing involving  $400^\circ\text{C}$  oxidation and  $\text{N}_2$  annealing for 30 min [Fig. 2(a)]. This was confirmed by X-ray diffraction measurements. Further improving the leakage current by optimizing the composition  $x$  in  $\text{Ti}_x\text{Ta}_{1-x}\text{O}$  and trading off the

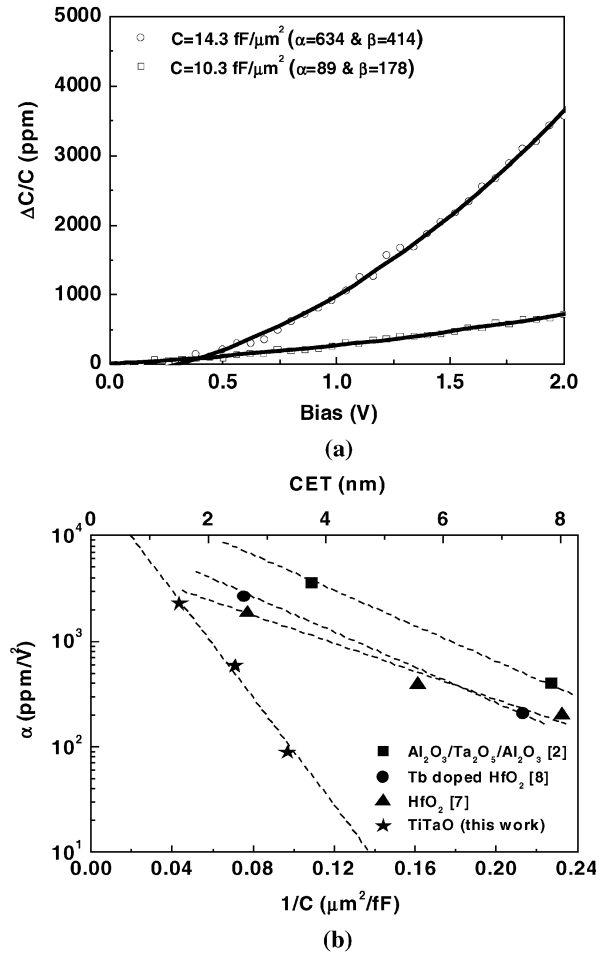


Fig. 3. (a)  $\Delta C/C$ - $V$  and (b)  $\Delta C/C$ - $1/C$  plot for Ir/TiTaO/TaN MIM capacitors.

capacitance density is needed for different system-on-chip application.

For analog capacitors, a low-capacitance voltage linearity is important. Fig. 3(a) shows a  $\Delta C/C$ - $V$  plot for Ir/TiTaO/TaN MIM capacitors with 10.3 and 14.3  $\text{fF}/\mu\text{m}^2$  density. The  $\Delta C/C$  decreases rapidly with decreasing capacitance density from 14.3 to 10.3  $\text{fF}/\mu\text{m}^2$ , which is consistent with the decreasing trend of the leakage current, as shown in Fig. 2(a). We obtained a quadratic voltage linearity ( $\alpha$ ) of 89  $\text{ppm}/\text{V}^2$  for the capacitance, and a first order voltage linearity ( $\beta$ ) of 178  $\text{ppm}/\text{V}$ . These are the lowest reported values [1]–[16] needed to meet the 10  $\text{fF}/\mu\text{m}^2$  density for analog capacitors, as specified in the ITRS roadmap. Fig. 3(b) shows the variation of  $\alpha$  as a function of CET or  $1/C$ . We note that the effect of  $\beta$  can be cancelled by circuit design. An exponential decrease of  $\alpha$  with increasing CET or  $1/C$  was observed for all the  $\text{Ta}_2\text{O}_5$ ,  $\text{HfO}_2$ , Tb-doped  $\text{HfO}_2$ , and Ir/TiTaO/TaN capacitors [2], [7], [8]. This may be due to the trap-related leakage current that has the exponential dependence with CET [6]. For the same CET or capacitance density value, the TiTaO device has the lowest  $\alpha$ —this is due to the high  $\kappa$  value of 45 which exceeds the  $\kappa \sim 22$ –25 values for  $\text{HfO}_2$  and  $\text{Ta}_2\text{O}_5$ . We note that the exponential decrease with increasing  $1/C$  is important when designing capacitors to meet different requirements.

TABLE I  
COMPARISON OF VARIOUS HIGH- $\kappa$  CAPACITORS. ALL THE REQUIREMENTS OF THE ITRS ROADMAP AT 2018 ARE SATISFIED BY THE Ir/TiTaO/TaN CAPACITOR

	ITRS @ 2018	Ta <sub>2</sub> O <sub>5</sub> [2]	Tb-HfO <sub>2</sub> [8]	HfO <sub>2</sub> [7]	This work	
C Density (fF/ $\mu\text{m}^2$ )	10	9.2	13.3	12.8	10.3	14.3
J (A/cm <sup>2</sup> )	-	$2 \times 10^{-8}$ (1.5V)	$1 \times 10^{-7}$ (2V)	$8 \times 10^{-9}$ (2V)	$1.2 \times 10^{-8}$ (2V)	$2 \times 10^{-7}$ (2V)
J/(C•V) (fA/[pF•V])	<7	14.5 @ 1.5V	38 @ 2V	2.9 @ 2V	5.8 @ 2V	—
$\alpha$ (ppm/V <sup>2</sup> )	$\alpha < 100$	3580	2667	1990	89	634
$\beta$ (ppm/V)		2060	332	211	178	414

Table I summarizes the important device parameters for the analog capacitors. The high capacitance density, low leakage current at 2 V and low voltage linearity meet all the requirements described in the in the ITRS roadmap for analog capacitors. Such excellent capacitor device performance is due to the very high  $\kappa$  of 45 in the TiTaO dielectric, and the high work-function Ir electrode. Further improving the RF quality-factor ( $Q = 1/\omega RC$ ) by using a stacked Cu/TaN-barrier/Ir top layer is needed to reduce series resistance. Note that there will be little impact for integrating Ir on back-end process due to low diffusion at low temperature, although high-work function IrO<sub>2</sub> metal-gate p-MOSFET [18] may be more challenging in a high-temperature front-end process.

#### IV. CONCLUSION

By using a novel high- $\kappa$  TiTaO dielectric and a high work-function Ir electrode, we have achieved excellent MIM capacitor performance, which meets the ITRS roadmap requirements for precision analog capacitors needed by 2018.

#### REFERENCES

- [1] C. H. Ng, K. W. Chew, J. X. Li, T. T. Tioa, L. N. Goh, and S. F. Chu, "Characterization and comparison of two metal-insulator-metal capacitor schemes in 0.13  $\mu\text{m}$  copper dual damascene metallization process for mixed-mode and RF application," *IEDM Tech. Dig.*, pp. 241–244, 2002.
- [2] T. Ishikawa, D. Kodama, Y. Matsui, M. Hiratani, T. Furusawa, and D. Hisamoto, "High-capacitance Cu/Ta<sub>2</sub>O<sub>5</sub>/Cu MIM structure for SoC applications featuring a single-mask add-on process," *IEDM Tech. Dig.*, pp. 940–942, 2002.
- [3] J. A. Babcock, S. G. Balster, A. Pinto, C. Dirnecker, P. Steinmann, R. Jumpertz, and B. El-Kareh, "Analog characteristics of metal-insulator-metal capacitors using PECVD nitride dielectrics," *IEEE Electron Device Lett.*, vol. 22, no. 5, pp. 230–232, May 2001.
- [4] M. Armacost, A. Augustin, P. Felsner, Y. Feng, G. Friese, J. Heidenreich, G. Hueckel, O. Prigge, and K. Stein, "A high reliability metal insulator metal capacitor for 0.18  $\mu\text{m}$  copper technology," in *IEDM Tech. Dig.*, 2000, pp. 157–160.
- [5] L. Y. Tu, H. L. Lin, L. L. Chao, D. Wu, C. S. Tsai, C. Wang, C. F. Huang, C. H. Lin, and J. Sun, "Characterization and comparison of high- $\kappa$  metal-insulator-metal (MIM) capacitors in 0.13  $\mu\text{m}$  Cu BEOI for mixed-mode and RF applications," in *Symp. VLSI Tech. Dig.*, 2003, pp. 79–80.
- [6] C. Zhu, H. Hu, X. F. Yu, S. J. Kim, A. Chin, M. F. Li, B. J. Cho, and D.-L. Kwong, "Voltage and temperature dependence of capacitance of high- $\kappa$  HfO<sub>2</sub> MIM capacitors: A unified understanding and prediction," in *IEDM Tech. Dig.*, 2003, pp. 379–382.
- [7] H. Hu, S. J. Ding, H. F. Lim, C. Zhu, M. F. Li, S. J. Kim, X. F. Yu, J. H. Chen, Y. F. Yong, B. J. Cho, D. S. H. Chan, S. C. Rustagi, M. B. Yu, C. H. Tung, A. Du, D. My, P. D. Foo, A. Chin, and D.-L. Kwong, "High performance ALD HfO<sub>2</sub>/AlO<sub>2</sub> laminate MIM capacitors for RF and mixed signal IC applications," in *IEDM Tech. Dig.*, 2003, pp. 879–882.
- [8] S. J. Kim, B. J. Cho, M.-F. Li, C. Zhu, A. Chin, and D. L. Kwong, "HfO<sub>2</sub> and lanthanide-doped HfO<sub>2</sub> MIM capacitors for RF/mixed IC applications," in *Symp. VLSI Tech. Dig.*, 2003, pp. 77–78.
- [9] S. J. Kim, B. J. Cho, S. J. Ding, M.-F. Li, M. B. Yu, C. Zhu, A. Chin, and D.-L. Kwong, "Engineering of voltage nonlinearity in high- $\kappa$  MIM capacitor for analog/mixed-Signal ICs," in *Symp. VLSI Tech. Dig.*, 2004, pp. 218–219.
- [10] M. Y. Yang, C. H. Huang, A. Chin, C. Zhu, M. F. Li, and D. L. Kwong, "High density MIM capacitors using AlTaO<sub>x</sub> dielectrics," *IEEE Electron Device Lett.*, vol. 24, pp. 306–308, May 2003.
- [11] C. H. Huang, M. Y. Yang, A. Chin, C. X. Zhu, M. F. Li, and D. L. Kwong, "High density RF MIM capacitors using high- $\kappa$  AlTaO<sub>x</sub> dielectrics," in *IEEE MTT-S Dig.*, vol. 1, 2003, pp. 507–510.
- [12] M. Y. Yang, C. H. Huang, A. Chin, C. Zhu, B. J. Cho, M. F. Li, and D. L. Kwong, "Very high density RF MIM capacitors (17 fF/ $\mu\text{m}^2$ ) using high- $\kappa$  Al<sub>2</sub>O<sub>3</sub> doped Ta<sub>2</sub>O<sub>5</sub> dielectrics," *IEEE Microw. Wireless Compon. Lett.*, vol. 13, pp. 431–433, Oct. 2003.
- [13] S. B. Chen, J. H. Lai, K. T. Chan, A. Chin, J. C. Hsieh, and J. Liu, "Frequency-dependent capacitance reduction in high- $\kappa$  AlTiO<sub>x</sub> and Al<sub>2</sub>O<sub>3</sub> gate dielectrics from IF to RF frequency range," *IEEE Electron Device Lett.*, vol. 23, no. 4, pp. 203–205, Apr. 2002.
- [14] S. B. Chen, J. H. Lai, A. Chin, J. C. Hsieh, and J. Liu, "High density MIM capacitors using Al<sub>2</sub>O<sub>3</sub> and AlTiO<sub>x</sub> dielectrics," *IEEE Electron Device Lett.*, vol. 23, no. 4, pp. 185–188, Apr. 2002.
- [15] S. B. Chen, C. H. Lai, A. Chin, J. C. Hsieh, and J. Liu, "RF MIM capacitors using high- $\kappa$  Al<sub>2</sub>O<sub>3</sub> and AlTiO<sub>x</sub> dielectrics," in *IEEE MTT-S Dig.*, vol. 1, 2002, pp. 201–204.
- [16] K. C. Chiang, C. H. Lai, A. Chin, H. L. Kao, S. P. McAlister, and C. C. Chi, "Very high density RF MIM capacitor compatible with VLSI," in *IEEE MTT-S Dig.*, Jun. 12–17, 2005.
- [17] *The International Technology Roadmap for Semiconductors*, 2003. Semicond. Ind. Assoc..
- [18] D. S. Yu, A. Chin, C. C. Laio, C. F. Lee, C. F. Cheng, W. J. Chen, C. Zhu, M.-F. Li, S. P. McAlister, and D. L. Kwong, "3 D GOI CMOSFET's with novel IrO<sub>2</sub>(Hf) dual gates and high- $\kappa$  dielectric on 1P6M-0.18  $\mu\text{m}$ -CMOS," in *IEDM Tech. Dig.*, 2004, pp. 181–184.