Briefs

On the Prediction of Geometry-Dependent Floating-Body Effect in SOI MOSFETs

Pin Su and Wei Lee

***Abstract*—This brief demonstrates that, through the perspective of body–source built-in potential lowering $(\Delta V_{\rm bi})$, the geometry-dependent floating-body effect in state-of-the-art silicon-on-insulator (SOI) MOSFETs can be explained and predicted by the geometry dependence of threshold voltage (V_T). The correlation between $\Delta V_{\rm bi}$ and V_T unveiled in this brief is the underlying mechanism responsible for the coexistence of partially depleted and fully depleted devices in a single SOI chip.**

***Index Terms*—Body–source built-in potential lowering, floating-body effect, silicon-on-insulator (SOI) CMOS, threshold voltage, partially depleted (PD), fully depleted (FD).**

As silicon-on-insulator (SOI) technology becomes a mature platform for high-speed and low-power applications [1]–[5], the main barrier to full exploitation of SOI performance and power is that the design of an SOI chip is a relatively risky process due to the lack of efforts on characterizing and modeling the floating-body behavior present in state-of-the-art SOI chips [1], [6]. Sub-100-nm SOI CMOS shows the trend of coexistence of partially depleted (PD) and fully depleted (FD) devices, depending on channel length and width, in a single chip [7]. The floating-body effect, in other words, shows significant geometry dependence. This technological trend poses a challenge to SOI modeling [8], [9], and its underlying mechanism merits investigation. Reference [10] has shown that the *body-source built-in potential lowering* $(\Delta V_{\rm bi})$ may represent the degree of full depletion (and thus floating-body effect) in SOI MOSFETs. In this brief, we show that similar to threshold voltage (V_T), $\Delta V_{\rm bi}$ may exhibit reverse narrow-width effect, reverse short-channel effect (SCE), as well as SCE. Moreover, we demonstrate that $\Delta V_{\rm bi}$ and V_T are correlated. This correlation explains and predicts the geometry-dependent floating-body effect. The implications on the characterization and modeling of scaled SOI CMOS are also addressed.

While V_T is determined by the front surface potential (ϕ), the floating-body effect is determined by the SOI back surface. The coupled back surface potential at the source junction $\Delta V_{\rm bi}$ can be probed by finding the onset of the external body bias (through a body contact) after which the V_T and hence the channel current of the SOI device is modulated (Fig. 1 inset) [10]. Fig. 1 shows that the frontgate coupling induces $\Delta V_{\rm bi}$ and in the strong inversion regime this frontgate-to-body coupling is shielded by the surface inversion layer, a manifestation of the correlation between $\Delta V_{\rm bi}$ and ϕ.

This correlation, under the assumption of thick buried oxide, can be formulated by applying the Poisson equation in the vertical direction [11], [12]

$$\Delta V_{\rm bi} = \phi - \frac{Q_B}{2C_{\rm Si}} \qquad (1)$$

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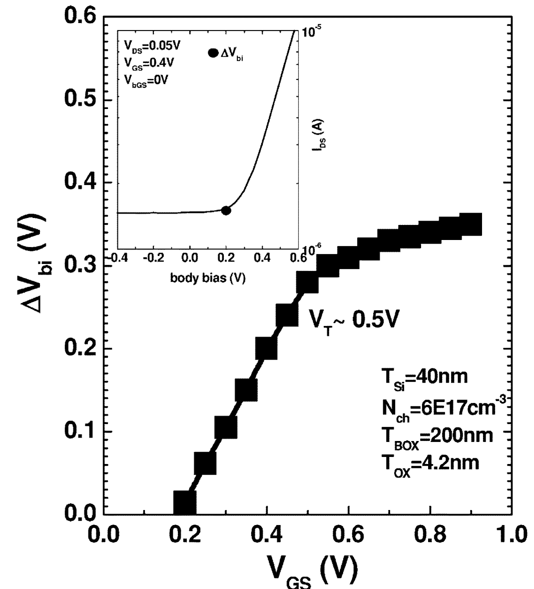

Fig. 1. Resemblance of $\Delta V_{\rm bi}$ and ϕ as a function of $V_{\rm GS}$. Notice that $\Delta V_{\rm bi}$ can be experimentally determined by the drain current versus body bias characteristics (at $V_{\rm DS} = 0.05$ V) of body-contacted devices.

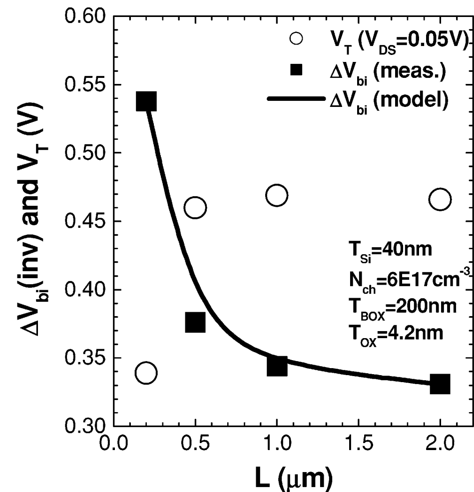

Fig. 2. Short-channel effect on $\Delta V_{\rm bi}$, which can be modeled by the same exponential functional form derived from the quasi-two-dimensional SCE for V_T [15].

where $Q_B = qN_{\rm ch}T_{\rm Si}$ and $C_{\rm Si} = \varepsilon_{\rm Si}/T_{\rm Si}$. Equation (1) indicates that $\Delta V_{\rm bi}$ increases when bulk charge Q_B (i.e., channel doping $N_{\rm ch}$ or SOI thickness $T_{\rm Si}$) decreases. Notice that at the onset of strong inversion

$$\Delta V_{\rm bi}({\rm inv}) = 2\phi_B - \frac{Q_B}{2C_{\rm Si}} \qquad (2)$$

where ϕ_B is a doping parameter that relates the potential of an electron at the Fermi level to the doping concentration [13]. $\Delta V_{\rm bi}({\rm inv})$ can be used as an index to represent the degree of full depletion (i.e., the immunity of floating-body effect) of SOI devices.

Fig. 2 shows that $\Delta V_{\rm bi}({\rm inv})$ rolls up while V_T rolls off as the channel length (L) is scaled down due to charge sharing from the source and

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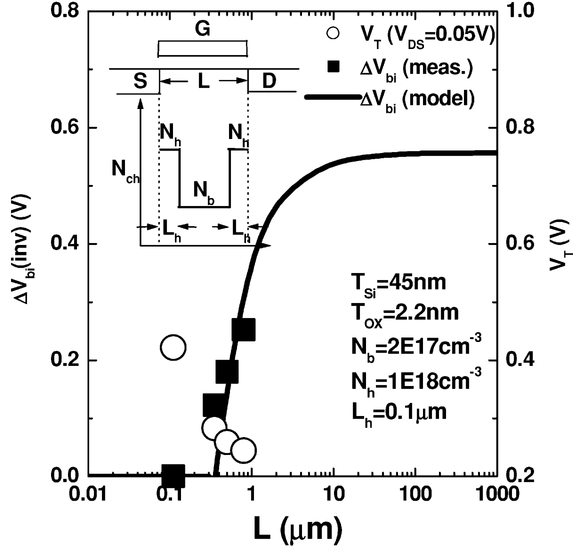

Fig. 3. Reverse SCE on $\Delta V_{\rm bi}$, which can be captured by the same functional form of the average channel doping for the reverse SCE on V_T [16].

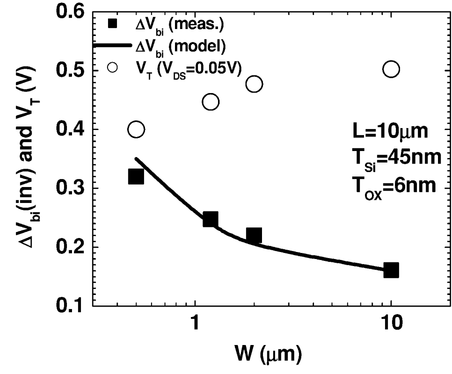

Fig. 4. Reverse narrow-width effect on $\Delta V_{\rm bi}$, which can be modeled by the same basic $1/W$ functional form for the reverse narrow-width effect on V_T [18].

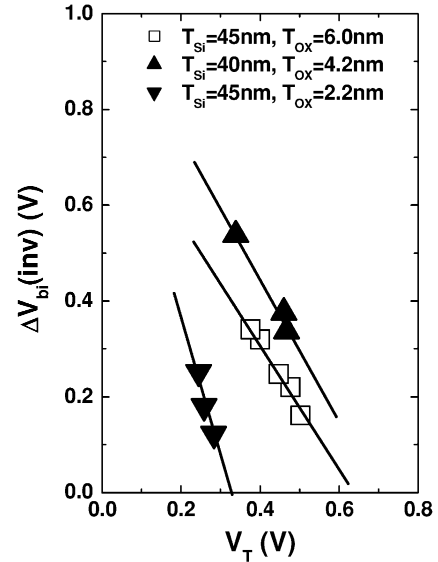

Fig. 5. Correlation between $\Delta V_{\rm bi}$ and V_T.

drain electrodes [14]. Also shown in Fig. 2 is that the same basic double exponential functional form, derived from the quasi-two-dimensional SCE for V_T [15], can be used to model the SCE on $\Delta V_{\rm bi}$

$$\Delta V_{\rm bi}({\rm inv}) = 2\phi_B - \frac{Q_B - \Delta Q_{\rm B,SCE}}{2C_{\rm Si}} \tag{3}$$

$$\Delta Q_{\rm B,SCE} = 2C_{\rm Si}\beta_0 \left[\exp\left(\frac{-\beta_1 L}{2l}\right) + 2\exp\left(\frac{-\beta_1 L}{l}\right)\right](V_{\rm bi} - 2\phi_B) \tag{4}$$

where β_0 and β_1 are model parameters, $V_{\rm bi}$ is the body-source built-in potential, and l is the characteristic length. Notice that the ratio of L to l may determine the enhancement of $\Delta V_{\rm bi}$ and the further suppression of floating-body effect of short-channel SOI devices.

As the SCE and $\Delta Q_{\rm B,SCE}$ are put down by raising L/l using the halo/pocket implant, V_T rolls up while $\Delta V_{\rm bi}({\rm inv})$ rolls off as L is scaled down, as shown in Fig. 3. The impact of laterally nonuniform channel doping on the length-dependent floating-body effect may be assessed by the approximated average channel doping

$$\Delta V_{\rm bi}({\rm inv}) \sim 2\phi_B - \frac{Q_B(L)}{2C_{\rm Si}} \tag{5}$$

$$Q_B(L) = qT_{\rm Si}\frac{N_{\rm b}(L - 2L_h) + N_h(2L_h)}{L} \tag{6}$$

where $N_b, N_h,$ and L_h represent background doping, average halo doping, and halo characteristic length, respectively (Fig. 3 inset). Note that although various functional forms for the average channel doping have been proposed to model the reverse SCE on V_T, the functional form in (6) has been shown satisfactory [16].

Equation (5) predicts the coexistence of both PD nominal devices ($\Delta V_{\rm bi}({\rm inv}) = 0$ V) and FD long-channel devices ($\Delta V_{\rm bi}({\rm inv}) > 0$ V) with continuous variations in between for state-of-the-art SOI CMOS, which is verified by the measured $\Delta V_{\rm bi}({\rm inv})$ in Fig. 3. Since these medium-to-long channel devices exhibit negligible floating-body effect, they are potential replacements of body-contacted devices.

In Fig. 4, the enhancement of $\Delta V_{\rm bi}({\rm inv})$ for devices with narrow width (W) can be attributed to the gate-field encroachment from the STI edges [7]. Since the bulk charge Q_B is effectively reduced by the fringing field [17], V_T rolls off while $\Delta V_{\rm bi}({\rm inv})$ rolls up as W is scaled down. Also shown in Fig. 4 is that, similar to the modeling of reverse narrow-width effect on V_T, the same basic $1/W$ functional form [18] can be used to model the reverse narrow-width effect on $\Delta V_{\rm bi}$. It is worth noting that this geometrical effect may enable FD narrow-width devices on a PD-SOI platform [7].

The geometry dependence of $\Delta V_{\rm bi}$ resembles that of V_T due to the geometry dependence of bulk charge Q_B. Moreover, $\Delta V_{\rm bi}$ and V_T are correlated by the following relationship:

$$\Delta V_{\rm bi} = \phi - \frac{T_{\rm Si}}{6T_{\rm OX}}(V_T - \Delta) \tag{7}$$

where $V_T = \Delta + Q_B/C_{\rm OX}, C_{\rm OX} = \varepsilon_{\rm OX}/T_{\rm OX}$, and $\Delta = V_{\rm fb} + 2\phi_B$. Note that although Δ depends on the flat-band voltage $V_{\rm fb}$, for n^+ polysilicon-gate NMOSFET and p^+ polysilicon-gate PMOSFET (dual-gate CMOS), the value of Δ is close to 0. Equation (7) predicts that $\Delta V_{\rm bi}({\rm inv})$ is linearly dependent on V_T with a slope equal to $-T_{\rm Si}/6T_{\rm OX}$, as verified by Fig. 5.

For a given SOI technology, in other words, the geometry dependence of $\Delta V_{\rm bi}$ and floating-body effect can be predicted by (7), provided that the geometry dependence of V_T is known. Therefore, for floating-body SOI devices where the body contact is not available, the degree of full depletion $\Delta V_{\rm bi}({\rm inv})$ may still be experimentally probed through the V_T measurement because of the correlation between $\Delta V_{\rm bi}$ and V_T. Notice that the need for multiple $V_T/T_{\rm OX}$ transistors for low

active/standby power requirement in a single chip can result in the coexistence of both PD and FD devices in the same circuit by design, as indicated by (7).

Using (7) to estimate the immunity of floating-body effect for devices with various feature size is also crucial to SOI compact modeling. To circumvent the modeling challenge imposed by the trend of coexistence of PD and FD devices in a single chip, a unified SOI compact model based on the concept of body-source built-in potential lowering has been proposed [8], [10]. Under this generic model framework where the PD/FD module may be selected through a module selector, the value of $\Delta V_{\mathrm{bi}}(\mathrm{inv})$ estimated by (7) can be used to determine the PD/FD module adequately in a per-instance manner to gain both simulation accuracy and efficiency.

In conclusion, the geometry-dependent floating-body effect can be explained and predicted by the correlation between ΔV_{bi} and V_T. This brief points out the underlying mechanism responsible for the coexistence of PD and FD devices in a state-of-the-art SOI chip.

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On-Chip Antennas for 60-GHz Radios in Silicon Technology

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***Abstract*—The recent advances in 60-GHz radios have called for the parallel development of compact and efficient millimeter-wave antennas. This brief addresses for the first time the design, fabrication, and characterization of on-chip inverted-F and quasi-Yagi antennas for 60-GHz radios. The design was made using the Zeland IE3D software package. The fabrication was realized with the back-end-of-line process of silicon substrates of low resistivity 10 Ω·cm. The characterization was conducted on wafer with Cascade Microtech coplanar probes and an HP8510XF network analyzer. The results show that the inverted-F antenna achieved a minimum return loss of 32 dB and a gain of −19 dBi at 61 GHz; while the quasi-Yagi antenna achieved a minimum return loss of 6.75 dB and a gain of −12.5 dBi at 65 GHz. Good agreement has been observed between the measured and simulated results.**

***Index Terms*—60-GHz radios, inverted-F antennas, on-chip antennas, quasi-Yagi antennas, wireless personal area network (WPAN).**

I. Introduction

There is much interest today in exploiting the 60-GHz band for wireless personal area network (WPAN) applications because a large bandwidth of 7 GHz is available [1]. The large bandwidth and millimeter-wave frequency have indeed created many challenges in the design of radio front-ends. The 60-GHz radio front-end implemented as an assembly of microwave monolithic integrated circuits (MMICs) in gallium arsenide (GaAs) semiconductor technology has proven feasible but rather expensive [2]. The 60-GHz radio front-end based on MMICs in silicon germanium (SiGe) semiconductor technology has been attempted. For instance, Renolds *et al.* demonstrated 60-GHz radio front-end circuits including a low-noise amplifier (LNA), a direct down converter, a power amplifier, and a voltage-controlled oscillator (VCO) in SiGe technology [3]. Design toward realizing a low-cost fully integrated SiGe 60-GHz radio front-end has been carried out. As the high-frequency capabilities of complimentary metal oxide semiconductor (CMOS) technology improve through scaling, CMOS has become a viable technology for millimeter-wave operation. Doan *et al.* has explored CMOS for 60-GHz applications and designed an LNA using a standard 0.13 μm CMOS process [4]. Luiz *et al.* demonstrated 64- and 100-GHz VCOs in 90-nm CMOS [5]. Liu *et al.* demonstrated a 63-GHz VCO in a standard 0.25-μm CMOS [6]. In addition, CMOS technology that promises to integrate a complete 60-GHz system (radio front-end plus digital processor) on a single chip (SoC) further enhances its competitiveness.

An antenna plays a key role in a radio. It has independent properties that affect the radio as a whole. Current antennas for 60-GHz radios are mainly discrete designs on conventional dielectric substrates [7], [8]. A relatively new development for 60-GHz antenna designs is the application of multichip module (MCM) technologies, which embeds antennas into integrated circuit packages [9]. At 60 GHz, the antenna form factor is on the order of millimeters or less and opens up new

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