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High voltage applications and NBTI effects of DT-pMOSFETS with reverse Schottky substrate contacts

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Abstract

In this study, the characteristics of DT-pMOSFETs are discussed using the reverse Schottky substrate contacts. With this diode, the DTMOS can be operated at high voltage and temperature. In addition, it exhibited an improved driving current, DIBL, transconductance, and subthreshold slope. The driving current for DTMOS was 20% larger, and was 12 mV improved for DIBL under DTMOS operation. Furthermore, the NBTI effects of DTMOS were also reported for the first time. This is because DTMOS could operate just below 0.7 V of V_G due to the junction turn-on behavior. It is interesting to note that the shift of the ΔV_{TH} of pMOSFETs under NBTI measurement was significantly alleviated in the DT operating mode, about 30 mV improved after 10,000 s stressing, due to the alleviated electrical field across the gate oxide which was due to the substrate bias and the threshold voltage adjustment under DTMOS operation.
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1. Introduction

The Dynamic Threshold voltage MOSFET (DTMOS) proposed by Assaderaghi et al. [1] is attractive for high-speed technical applications. By shorting the gate to the substrate, the threshold voltage operating under the DT mode is reduced due to the forward biasing of the substrate so that the current drive can be drastically improved when in the "on" state. Since the device exhibits the same normal-mode V_{TH} under the off state (because $V_G = V_{BS} = 0$), low standby power consumption is maintained. The subthreshold slope and short channel effects are also improved due to the dynamics substrate bias [1–3]. However, the pn diode between the substrate and the source turns on as the forward bias between the substrate and the source terminals becomes larger than 0.7 V. A considerably large leakage current due to the turn-on diode current between substrate and source terminals was a serious issue under DT mode operation, as shown in Fig. 1. The large leakage current dominates the output characteristics when the gate voltage of DT-pMOSFETs is larger than −0.7 V. Therefore, the power supply voltage for DTMOS applications is restricted to less than 0.7 V due to the turn-on behavior between the substrate and the source junction. Some reports [4–6] proposed that the Schottky contact formation in the substrate contact and the body potential would be limited to a value (~0.4 V) lower than forward diode voltage drop. The subthreshold slope,

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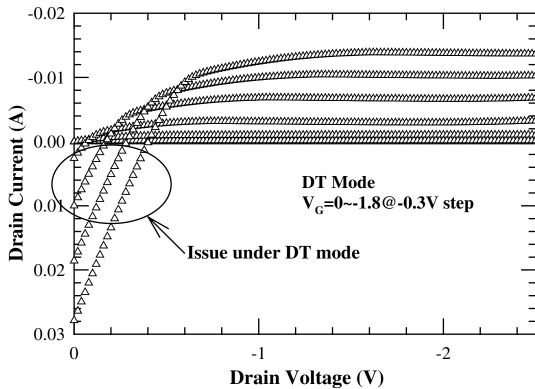

Fig. 1. I_D–V_D curves for conventional DTMOS, with a gate length equal to 0.8 μm and a width equal to 100 μm.

transconductance, and threshold voltage can be improved by the dynamic substrate bias and any turn-on behavior between the substrate and source terminals will not occur due to the limitations of the substrate bias from the reverse Schottky substrate contacts. Furthermore, a drift in threshold voltage due to the reliability degradation is a major concern in the analog and mixed-signal applications. Negative Bias Temperature Instability (NBTI) of p^+-gate MOSFETs has been reported as one of the serious issues for the reliability of ultra-thin gate dielectrics due to a higher threshold voltage degradation [7–9]. The NBTI degradation was used as a limit of the device's lifetime when the gate oxide thickness was less than 3.5 nm. Normally in NBTI stressing, the stressing temperature ranges from 100 to 200 °C, and E_{OX} by gate electrode was from −6 to −15 MV/cm. Higher temperature stress enhances NBTI and its degradation was thermally activated, i.e., very sensitive to temperature effects, as shown in Eqs. (1) and (2) [10].

$$\Delta N_{it} = 9 \times 10^{-4} E_{OX}^{1.5} t^{0.25} \exp(-0.2/kT)/t_{OX}, \quad (1)$$

$$\Delta N_f = 490 E_{OX}^{1.5} t^{0.14} \exp(-0.15/kT), \quad (2)$$

where E_{OX} was electrical field and t_{OX} was gate dielectric thickness. ΔN_{it} and ΔN_f are the increase of the interfacial states and the fixed charges in the oxide under NBTI stressing, respectively. From Eq. (2), it implied that ΔN_f was no t_{OX} independent in the 4–30 nm range, which was different from ΔN_{it} [10]. However, the detailed degradation process is still not well understood. There are no reports about the effects of NBTI under DTMOS operation, which means that the gate oxide characteristics could not be understood as DTMOS operation. This is because the gate voltage of DT-pMOSFETs must be less than −0.7 V. In this study, the novel structure and electrical characteristics of DT-pMOSFETs were reported with a reverse Schottky substrate contact for its high voltage and temperature applications. In addition, the NBTI effect of this device will be discussed in this study for the first time.

2. Device fabrication

P-channel MOS transistors with channel length as small as 0.8 μm were fabricated on 6-in. silicon wafers with resistivities of 15–20 Ω cm using a conventional pMOSFET baseline. Local oxidation of silicon (LOCOS) was used to isolate the device. An As^+ channel implant (at 100 keV, 1×13 cm^{-2}) was used for the adjustment of the threshold voltage. A gate dielectric with a thickness of 2.8 nm was grown in an ambient N_2O atmosphere, followed by a 200 nm poly-Si deposition. The channel width was 100 μm. Shallow S/D extensions were formed by BF_2 implant at 10 keV to a dose of 1×10^{15} cm^{-2}. After the formation of a TEOS sidewall spacer (200 nm), deep source/drain junctions were formed by BF_2 implantation at 20 keV to a dose of 6×10^{15} cm^{-2}. Wafers were then annealed by a rapid thermal process (RTP) at 1020 °C for 20 s for dopant activation. Finally, a 550 nm-thick TEOS by PECVD was deposited, and a Ti/TiN/Al–Si–Cu/TiN 4-layer metal was deposited and patterned to complete the contact metallization. Without any substrate ion implantation, the substrate contact formed was a Ti-silicide on an n^- type substrate. Finally, gas sintering was performed on metal alloy at 400 °C. Electrical characterizations were performed using a HP4156 system and a temperature-regulated hot chuck at temperature ranging from 25 to 100 °C.

3. Results and discussion

3.1. Electrical characteristics of DT-pMOSFETs with reverse Schottky substrate contacts

Fig. 2 shows the cross section and equivalent circuits of the device after silicidation. Instead of n^+ substrate ion implantation forming ohmic contact, the n^--substrate was reacted directly with Ti in order to form a Schottky barrier. In operation, the source was the ground, and the gate shorted to the substrate was biased in negatively biased. It is well known that the serious issue under DT mode occurs as substrate/source is forward biased, which is shown in Fig. 1, exhibiting the diode's turn-on behavior. Therefore, DTMOS cannot be widely used when operational voltage is larger than 0.7 V. In order to avoid the condition to extend the application range of DTMOS, the substrate bias should be limited to below −0.7 V to avoid the junction turn-on behavior under DTMOS operation. Adding this reverse Schottky barrier, the voltage is only a cut-in voltage for source/substrate, and drops other voltage on the

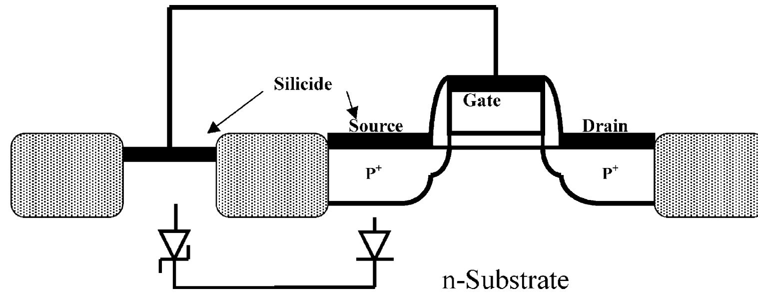

Fig. 2. A cross section of the device and its equivalent circuit between source and substrate.

reverse Schottky barrier. Hence, it can be operated in high voltage without any concerns of turn-on behavior. In addition, this structure still maintained the advantages of conventional DTMOS. The transfer characteristics were shown in Fig. 3(a). The subthreshold slope was steep under the DTMOS operation. Fig. 3(b) shows the drain current versus drain voltage, under different modes at room temperature, with the gate voltage ranging from 0 to 3 V at −0.5 V steps. As expected, no turn-on diode characteristic in Fig. 1 was found by adding the

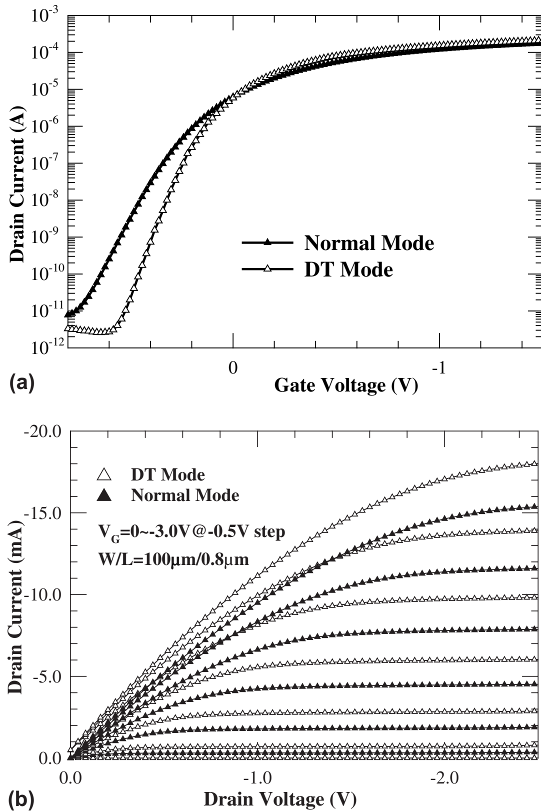

Fig. 3. (a) Transfer characteristics, (b) drain current versus drain voltage, in which the gate length was equal to 0.8 m and width was equal to 100 μm, for both DT and normal modes.

reverse Schottky substrate contact because the gate voltage was larger than 0.7 V. In addition, the saturation current under DT mode at $V_D = -2.5$ V and $V_G = -3.0$ V was large than that that under normal mode (about 20%). This was due to the good V_{TH} reduction and increasing transconductance under DTMOS operation [11–13]. The threshold voltages of DT mode and normal mode for the device were −241.8 and −350.4 mV, respectively. The gate voltage versus transconductance for DT and normal modes is depicted in Fig. 4(a), where $V_D = -0.1$ V. The hump behavior of transconductance under DT mode was due to the body potential limitation by the reverse Schottky Substrate barrier. The threshold voltage versus substrate bias for normal devices with Schottky substrate contacts, which was simulated the DT mode behavior, was also shown in Fig. 4(b) for a range of temperatures. The absolute value of threshold voltage decreases as the value of the substrate bias decreases to a negative value. However, the threshold voltage was almost constant as the substrate bias <−0.6 V as a result from the reverse biased Schottky barrier at the substrate contacts. In addition, the reverse Schottky barrier contacts could prevent from the turn-on behavior between source/substrate junction, as shown in Fig. 1. Saturation transconductance ($V_G = V_D = -1.8$ V) versus drain induced barrier lowering (DIBL) under different modes for two different temperature (25 and 100 °C) was shown in Fig. 5. The magnitude of DIBL was decreased for DT-mode operation both for 25 and 100 °C conditions. This is may be due to the substrate bias, which could decrease the depletion region as DTMOS operation [1]. Furthermore, the saturation transconductance was also increased for DTMOS due to the reduction of the threshold voltage, same as the linear transconductance.

3.2. NBTI effects of DTMOS

First of all, there is still no reference to the NBTI behaviors between DTMOS and normal MOSFETs comparisons due to the operation limitation of conventional DTMOS, as is shown in Fig. 1. The degradation of the threshold voltage due to NBTI effects of the

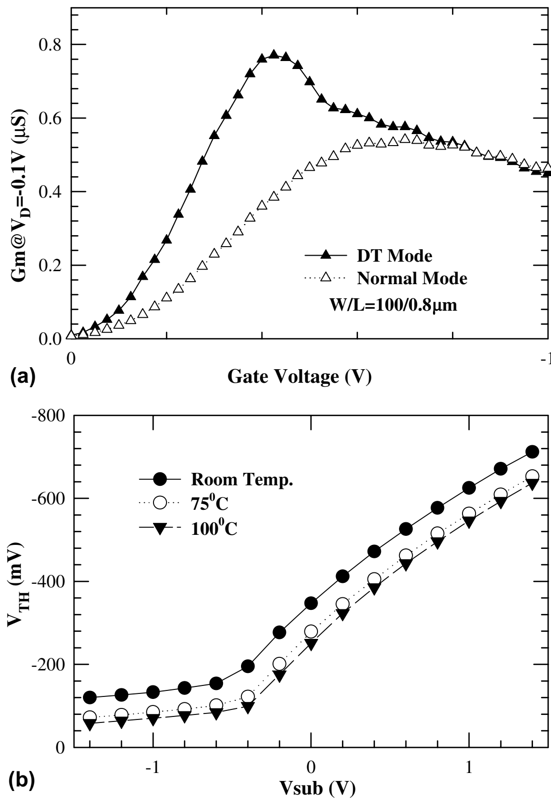

Fig. 4. (a) Gate voltage versus transconductance, where the gate length was equal to 0.8 μm and the width was equal to 100 μm, for both DT and normal modes. (b) The threshold voltage versus substrate bias for different temperature (25, 75, and 100 °C).

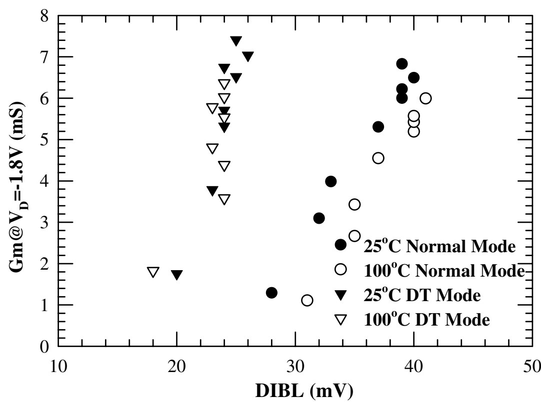

Fig. 5. Saturation transconductance ($V_D = -1.8$ V) versus drain induced barrier lowering (DIBL) under different modes for different temperature (25 and 100 °C).

DT-pMOSFETs was shown in Fig. 6. The stressing conditions were $V_G = -3.5$ V, while other terminals were grounded at 100 °C. As the interface density, D_{it}, and

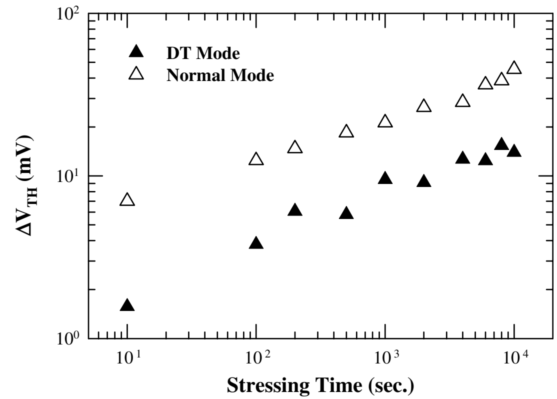

Fig. 6. Stress time dependence of threshold voltage degradation ($\Delta V_{TH} = V_{TH}(t) - V_{TH}(0)$) for pMOSFETs under different operation modes. The NBTI stressing was at $V_G = -3.5$ V and the other terminals were grounded.

oxide trap charge increased, the absolute value of the threshold voltage increased as well [7–9]. To operate in normal mode, the shift of the V_{TH} monotonically increases as the stressing time increases, and the value of ΔV_{TH} is about 46 mV after 10,000 s of stressing. However, it is interesting to note that the degradation of V_{TH} was significantly reduced and saturated by approximately 13 mV after 1000 s, while operating under DT mode. This is due to the fact that the electrical field across gate oxide is reduced by the substrate bias, $E_{OX} = \frac{V_G - V_{FB} - \varphi_s - V_{SUB}}{t_{OX}}$ under DTMOS operation. In addition, due to negative substrate bias while in DT mode, the magnitude of the threshold voltage would be reduced, [11] and DTMOS operation could decrease the variation of the threshold voltage [12]. Therefore, the threshold voltage degradation of NBTI effects under DTMOS operation could be effectively suppressed. It is also interesting to note that the slopes as shown in figure, for DT and normal modes do not depict any apparent differences. Finally, for the perspective of the NBTI effect, the threshold voltage degradation under DT mode operation was drastically improved due to the alleviated electrical field across the gate oxide and the threshold voltage adjustment.

4. Conclusion

The electrical characteristics of DT-pMOSFETs with the reverse Schottky substrate contacts and its NBTI effects were reported in this study for the first time. This structure showed the possibility that DTMOS operates at high voltage and temperature. It was found that the saturation current, DIBL, transconductance, and subthreshold slope could all be simultaneously improved. In addition, the serious V_{TH} degradation of NBTI stressing

of conventional pMOSFETs was significantly reduced using the novel structure due to the reduced electrical field across the gate oxide and the threshold voltage adjustment ability under DTMOS operation. Therefore, DT-pMOSFETs with the reverse Schottky substrate contacts are a good candidate for the next generation industrial applications.

Acknowledgments

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