Performance and Reliability of Poly-Si TFTs on FSG Buffer Layer

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***Abstract*—A novel and process-compatible scheme for fabricating poly-Si thin-film transistors (TFTs) on an FSG buffer layer was proposed and demonstrated. Experimental results reveal that remarkably improved device performance and uniformity can be achieved with appropriate fluorine concentration. The poly-Si TFTs fabricated on FSG layers have a higher on-current, a lower leakage current, and a higher field-effect mobility compared with the conventional poly-Si TFTs. Furthermore, the incorporation of fluorine also increased the reliability of poly-Si TFTs against hot carrier stressing, which is attributed to the formation of Si–F bonds.**

***Index Terms*—Buffer layer, fluorine, fluorinated silicate oxide (FSG), polycrystalline silicon thin-film transistors (poly-Si TFTs), reliability.**

I. Introduction

POLYCRYSTALLINE silicon thin-film transistors (poly-Si TFTs) have attracted much attention owing to the possibility of realizing the integration of driving circuits and pixel elements on a single glass substrate, and the potential to accomplish the system-on-panel (SOP) [1]. High-performance and high-reliability poly-Si TFTs are required to reach this goal. Excimer laser annealing (ELA) has been utilized in enlarging the grains of the poly-Si to reduce trap states, leading to an excellent device performance [2]. However, the random distribution of grain boundaries in poly-Si films still causes a large leakage current and poor device uniformity. Hydrogenation process has been utilized to terminate the grain boundary trap states [3]. However, hydrogenated poly-Si TFTs suffer from an instability issue due to weak Si–H bonds [4]. On the other hand, a low-temperature plasma-enhanced chemical vapor deposition (PECVD)-oxide buffer layer is conventionally adopted to block the contaminations from the inexpensive glass or flexible plastic substrate. Nevertheless, the mismatch between the thermal expansion coefficient of the poly-Si and that of the oxide causes considerable mechanical tensile stress at the interface during ELA, leading to the degradation in device performance [5]–[8]. All these drawbacks limit the applications of poly-Si TFTs. Recently, fluorine atoms have been proposed to terminate trap states in the poly-Si [9]–[12]. The formation of Si–F bonds improves the device reliability. However, ion implantation is not appropriate for extremely large-sized glass substrate in current productions.

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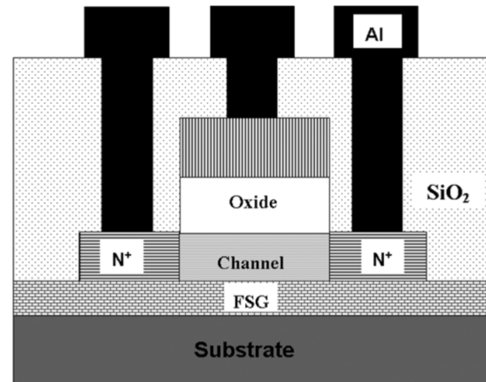

Fig. 1. Cross section of the proposed poly-Si TFT fabricated on a FSG buffer layer.

Therefore, a new method must be found to introduce fluorine atoms into poly-Si films. Fluorinated silicate oxide (FSG) has been known easy to integrate using PECVD systems. The out-diffused fluorine atoms form FSG can terminate trap states and also release the strain bonds at the interface [13]. This letter proposes a novel process-compatible fluorination technique using a FSG film as the buffer layer. The Poly-Si TFTs fabricated on FSG buffer layers exhibit high device performance, uniformity, and reliability.

II. Experimental

Fig. 1 schematically depicts the cross section of the proposed poly-Si TFT. All the experimental devices in this letter were fabricated on thermally oxidized Si wafers. First, a 50-nm-thick FSG buffer layer was deposited using a PECVD system at 350 °C with SiH_4, CF_4, and N_2O as process gases. To determine the effect of fluorine content in FSG layers, varying CF_4 flow rates of 10, 20, and 40 sccm, with a SiH_4 flow rate of 90 sccm and a N_2O rate of 5 sccm, were used to grow various FSG buffer layers, denoted by FSG1, FSG2, and FSG3, respectively. The fluorine contents in FSG1, FSG2, and FSG3 were about 2%, 4%, and 7%, respectively. Then, 100-nm-thick amorphous silicon layers were deposited on the FSG layers in a low-pressure chemical vapor deposition (LPCVD) system. Next, a semi-Gaussian-shaped KrF excimer laser ($\lambda = 248$ nm) with an energy density of 420 $\mathrm{mJ/cm^2}$ was performed for the phase transformation from amorphous to polycrystalline silicon. The

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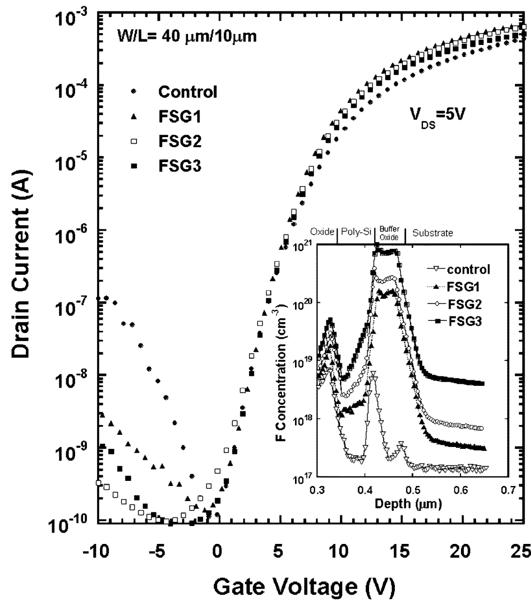

Fig. 2. Transfer characteristics of the poly-Si TFTs fabricated on various buffer layers. The inset shows the SIMS profiles of fluorine in the poly-Si on various buffer layers.

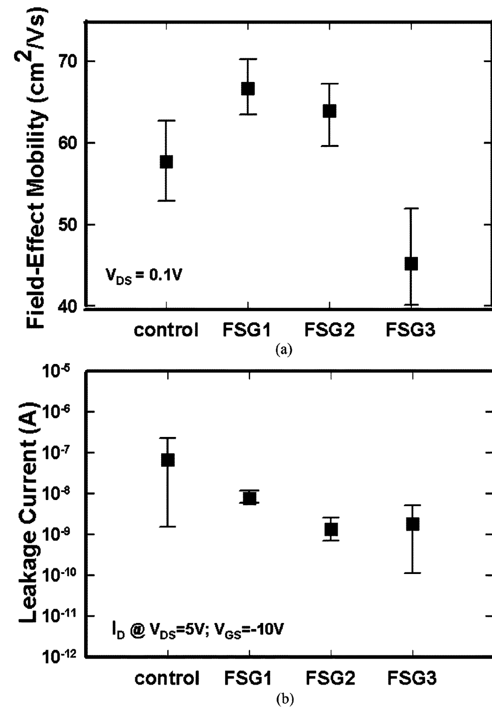

Fig. 3. (a) Distributions of field-effect mobility and (b) leakage current of the poly-Si TFTs on different buffer layers. The vertical bars indicate the minimum and maximum values of the devices characteristics and the squares are the average values.

average grain size of the poly-Si is approximately 300 nm. Individual active regions were then patterned and defined. After a clean process, a 100-nm-thick TEOS oxide and a 200-nm-thick poly-Si were deposited to serve as the gate insulator and the gate electrode. A self-aligned phosphorous ion implantation was preformed at the dosage and energy of 5×10^{15}cm^{-2} and 40 keV, respectively. The dopant activation was performed by ELA, followed by a deposition of passivation layer and the definition of contact holes. Finally, a 500-nm-thick Al electrode was deposited and patterned. For comparison, the control samples were fabricated on a 50-nm-thick conventional PECVD-oxide buffer layer.

III. Results and Discussion

Fig. 2 shows the transfer characteristics of the conventional and the proposed poly-Si TFTs at $V_{\rm DS} = 5$ V. The poly-Si TFTs fabricated on the FSG buffer layers exhibit better on-state and off-state characteristics than those of the control sample. Notably, under a large negative gate bias, the leakage currents of the TFTs on FSG layers are over one order of magnitude lower than that on the conventional oxide buffer layer. This is ascribed to the facts that the reduced the traps by the incorporation of fluorine in the poly-Si films during ELA [12] and the released tensile stress at the poly-Si/buffer-oxide-layer interface [13]. The evidence of the fluorine incorporation can be firmly demonstrated with the SIMS profiles of fluorine shown in the inset of Fig. 2. It was clearly observed that considerable fluorine atoms were detected in the poly-Si for the FSG samples and, in particular, two fluorine peaks were located at the top and bottom interfaces. Therefore, we believe that the weak bonds and dangling bonds in the poly-Si grain boundaries and both top and bottom interfaces, resulting in lots of trap states and interface states, were terminated by fluorine [10]. In order to verify the effect of fluorine passivation, the effective trap state density (N_T) was calculated from the square root of the slope of the $\ln(I_D V_{\rm DS}/V_{\rm GS})$ versus $1/V_{\rm GS}^2$ plots, which was proposed by Proano *et al.* [14]. The N_T for the control, FSG1, FSG2, and FSG3 were 5.64×10^{12}, 3.91×10^{12}, 3.97×10^{12}, and 4.01×10^{12}cm^{-2}, respectively. These figures strongly hint that the fluorine can effectively terminate the present trap states. However, the FSG3 shows a detrimental effect on the performance of the resulting TFT. This is attributed to the moisture absorption. According to previous report, the moisture absorption increased with increasing fluorine content in the FSG layers [15]. The absorbed moisture would easily form OH or react with fluorine to form HF, which in turn corrode the devices and result in the degraded performance and reliability [16].

Fig. 3 displays the statistical distributions of the field-effect mobility $(\mu_{\rm eff})$ and the leakage current $(I_{\rm off})$ of the poly-Si TFTs fabricated on different buffer layers. The vertical bars in the figure indicate the minimum and maximum values of the devices characteristics and the squares present the average values. The average values of the $\mu_{\rm eff}$ for the control, FSG1, FSG2, and FSG3 samples were 57.7, 66.7, 63.9, and 45.2 with standard deviations of 4.05, 2.98, 3.09, and 4.15, respectively. This tendency indicates that with moderate fluorine content in FSG layers the average values and the deviations of $\mu_{\rm eff}$ can be greatly improved. Also, the average values of the $I_{\rm off}$ for the control, FSG1, FSG2, and FSG3 samples were 6.8×10^{-8}, 7.8×10^{-9}, 1.3×10^{-9}, and 1.8×10^{-9} with standard deviations of 8.14×10^{-8}, 2.46×10^{-9}, 6.55×10^{-10}, and 1.93×10^{-9}, respectively. The uniformity of the poly-Si TFTs is strongly affected by the random distribution of grain boundaries. Therefore, using fluorine to terminate those trap states can effectively alleviate the influence of grain boundaries.

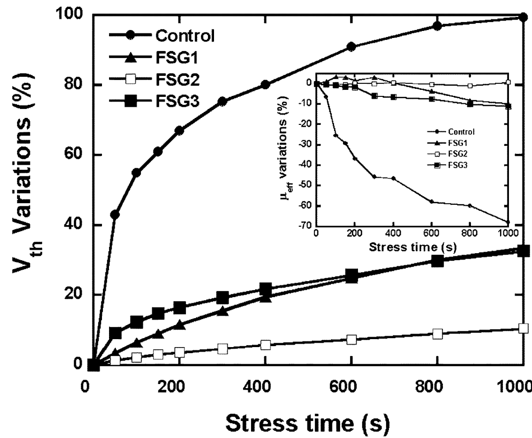

Fig. 4. Variations of threshold voltage as a function of stress time under hot carrier stress. The inset shows the variations of field-effect mobility as a function of stress time under hot carrier stress.

Hot-carrier-stress was performed at $V_{\rm DS} = 20$ V and $V_{\rm GS} = 10$ V for 1000 s to investigate the device reliability. Fig. 4 plots the variations of threshold voltage $(V_{\rm th})$ and $\mu_{\rm eff}$ over hot carrier stress time. The variations of $V_{\rm th}$ and $\mu_{\rm eff}$ were defined as $(V_{\rm th,stressed}–V_{\rm th,0})/V_{\rm th,0} \times 100\%$ and $(\mu_{\rm eff,stressed}–\mu_{\rm eff,0})/\mu_{\rm eff,0} \times 100\%$, respectively, where $V_{\rm th,stressed}$, $\mu_{\rm eff,stressed}$, $V_{\rm th,0}$, and $\mu_{\rm eff,0}$ represent the measured values before and after stress. Notably, the control shows relatively large variations in both $V_{\rm th}$ and $\mu_{\rm eff}$ after 1000s stress, whereas the FSG2 stays almost unchanged. These results imply that poly-Si TFTs fabricated on the FSG layer greatly reduced the device degradation under hot carrier stress, which is due to the formation of the Si–F bonds. Since the calculated percentages of F content in the FSG layers are 2%, 4%, and 7% for FSG1, FSG2, and FSG3, respectively, we deduce based on the above experimental results that the trap states can be effectively terminated when the fluorine content in the FSG is above 2%; while the absorbed moisture in the FSG as the content is above 4% starts to induce visible corrosion of the poly-Si structures after competing with the trap states termination. Definitely, the corrosion becomes more severe as the content reached 7%. As a result, the optimized condition of fluorine content of FSG is probably within 2% to 4%.

IV. Conclusion

A novel process-compatible scheme for fabricating poly-Si TFTs on an FSG buffer layer is proposed. Significant improvements in the device performance and uniformity were successfully demonstrated with fluorine incorporation in the poly-Si layer. The incorporation of fluorine also promotes the hot-carrier immunity. Fabricating poly-Si TFTs on FSG buffer layers with appropriate fluorine content improves not only the electrical performance and uniformity but also the reliability.

References

[1] T. Serikawa, S. Shirai, A. Okamoto, and S. Suyama, "Low-temperature fabrication of high-mobility poly-Si TFTs for large-area LCDs," *IEEE Trans. Electron Devices*, vol. 36, no. 9, pp. 1929–1933, Sep. 1989.

[2] G. K. Guist and T. W. Sigmon, "High-performance thin-film transistors fabricated using excimer laser processing and grain engineering," *IEEE Trans. Electron Devices*, vol. 45, no. 4, pp. 925–932, Apr. 1998.

[3] I. W. Wu, W. B. Jackson, T. Y. Huang, A. G. Lewis, and A. Chiang, "Passivation kinetics of two types of defects in polysilicon TFT by plasma hydrogenation," *IEEE Electron Device Lett.*, vol. 12, no. 5, pp. 181–183, May 1991.

[4] ——, "Mechanism of device degradation in n- and p-channel polysilicon TFTs by electrical stressing," *IEEE Electron Device Lett.*, vol. 11, no. 4, pp. 167–170, Apr. 1990.

[5] E. Fujii, K. Senda, F. Emoto, A. Yamamoto, A. Nakamura, Y. Uemoto, and G. Kano, "A leaser-recrystallization technique for silicon-TFT integrated circuits on quartz substrates and its application to small-size monolithic active-matrix LCDs," *IEEE Trans. Electron Devices*, vol. 37, no. 1, pp. 121–127, Jan. 1990.

[6] M. Cao, S. Talwar, K. J. Kramer, T. W. Sigmon, and K. C. Saraswat, "A high-performance polysilicon thin-film transistor using XeCl excimer laser crystallization of pre-patterned amorphous Si films," *IEEE Trans. Electron Devices*, vol. 43, no. 4, pp. 561–567, Apr. 1996.

[7] K. Kitahara, A. Moritani, A. Hara, and M. Okabe, "Micro-scale characterization of crystalline phase and stress in laser-crystallized poly-Si thin films by Raman spectroscopy," *Jpn. J. Appl. Phys.*, vol. 38, pp. L1312–1314, 1999.

[8] S. Higashi, N. Ando, K. Kamisako, and T. Sameshima, "Stress in pulsed-laser-crystallized silicon films," *Jpn. J. Appl. Phys.*, vol. 40, pp. 731–735, 2001.

[9] H. N. Chern, C. L. Lee, and T. F. Lei, "The effects of fluorine passivation on polysilicon thin film transistors," *IEEE Trans. Electron Devices*, vol. 41, no. 5, pp. 698–702, May 1994.

[10] S. Maegawa, T. Ipposhi, S. Maeda, H. Nishimura, T. Ichiki, M. Ashida, O. Tanina, Y. Inoue, T. Nishimura, and N. Tsubouchi, "Performance and reliability improvement in poly-Si TFTs by fluorine implantation into gate poly-Si," *IEEE Trans. Electron Devices*, vol. 42, no. 6, pp. 1106–1112, Jun. 1995.

[11] J. W. Park, B. T. Ahn, and K. Lee, "Effects of F^+ implantation on the characteristics of poly-Si films and low-temperature n-ch poly-Si thin-film transistors," *Jpn. J. Appl. Phys.*, vol. 34, pp. 1436–1441, Mar. 1995.

[12] C. H. Kim, S. H. Jung, J. S. Yoo, and M. K. Han, "Poly-Si TFT fabricated by laser-induced *in situ* fluorine passivation and laser doping," *IEEE Electron Device Lett.*, vol. 22, no. 8, pp. 396–398, Aug. 2001.

[13] Y. Mitani, H. Satake, Y. Nakasaki, and A. Toriumi, "Improvement of charge-to-breakdown distribution by fluorine incorporation into thin gate oxides," *IEEE Trans. Electron Devices*, vol. 50, no. 11, pp. 2221–2226, Nov. 2003.

[14] R. E. Proano, R. S. Misage, and D. G. Ast, "Development and electrical properties of undoped polycrystalline silicon thin-film transistors," *IEEE Trans. Electron Devices*, vol. 36, no. 9, pp. 1915–1922, Sep. 1989.

[15] H. Miyajima, R. Katsumata, Y. Nakasaki, Y. Nishiyama, and N. Hayasaka, "Water absorption properties of fluorine-doped $\mathrm{SiO_2}$ films using plasma-enhanced chemical vapor deposition," *Jpn. J. Appl. Phys.*, vol. 35, pp. 6217–6225, 1996.

[16] G. Passemard, P. Fugier, P. Nobl, F. Pries, and O. Demolliens, "Study of fluorine stability in fluoro-silicate glass and effects on dielectric properties," *Microelectron. Eng.*, vol. 33, pp. 335–342, 1997.