Large-Scale Atomistic Circuit-Device Coupled Simulation of Discrete-Dopant-Induced Characteristic Fluctuation in Nano-CMOS Digital Circuits

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Abstract The increasing characteristics variability in nano-CMOS devices becomes a major challenge to scaling and integration. In this work, a large-scale statistically sound "atomistic" circuit-device coupled simulation methodology is presented to explore the discrete-dopant-induced characteristic fluctuations in nano-CMOS digital circuits. According to the simulation scenario, the discrete-dopant-induced characteristic fluctuations are examined for a 16-nm-gate MOSFET and inverter circuit. The fluctuations of the intrinsic current-voltage and capacitance-voltage characteristics, and timing behaviors for the explored device and circuit are estimated. The timing fluctuation may result in a significant signal delay in the digital circuit. Consequently, links should be established between circuit design and fundamental device technology to allow circuits and systems to accommodate the individual behavior of every transistor on a silicon chip. The proposed simulation approach could be extended to outlook the fluctuations in various digital and analog circuits.

1 Introduction

Yield analysis and optimization, which take the manufacturing tolerances, model uncertainties, variations in the process parameters, etc, into account, have been known as indispensable components of the circuit design methodology[1]. Various randomness effects resulting from the random nature of manufacturing process, such as ion implantation, diffusion, and thermal annealing, have induced significant fluctuations of electrical characteristics in nano-MOSFETs. The number of dopants is of the order of tens in the depletion region of a MOSFET, whose influence on device characteristic is large enough to be distinct[2]. Diverse approaches have recently been reported to study fluctuation-related issues in semiconductor devices and circuits [2–7]. However, the attention is less drawn on the existence of timing characteristic fluctuations of an active device due to random dopant placement.

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Moreover, due to the randomness of the dopant position in the device, the fluctuation of the device's gate capacitance is hard to be modeled in the current compact models [7]. Therefore, in this study, we propose a large-scale statistically sound circuit-device coupled simulation approach to analyze the random dopant effect in nano-CMOS circuit, concurrently capturing the discrete-dopant-number- and discrete-dopant-position-induced fluctuations. Based on the statistically generated large-scale doping profiles, the device simulation is performed by solving a set of three-dimensional (3D) drift-diffusion equations with quantum corrections by the density gradient method [8, 9] on a parallel computing system [10, 11]. In the estimation of the circuit-level characteristics fluctuations, to capture the nonlinearity of gate capacitance fluctuation, the aforementioned device equations are coupled with the circuit nodal equations of the studied circuit and solve simultaneously. The proposed simulation approach can outlook the fluctuations in circuit characteristics and benefit the development of next generation nanoelectronic circuits and systems.

The paper is organized as follows. In Sec. 2, we introduce the large-scale statistically sound "atomistic" simulation approach and simulation techniques for studying the random dopant effect in nanoscale device and circuit. In Sec. 3, we investigate the discrete-dopant-induced device and circuit characteristic fluctuations in the 16-nm-gate CMOS circuit. Finally, we draw conclusions and suggest future work.

2 Simulation Technique

Figure 1 shows the simulation flow for the proposed approach. To consider the effect of random fluctuation of the number and location of discrete dopants in the channel region, 758 dopants are randomly generated in a $(80\ \text{nm})^3$ cube, in which the equivalent doping concentration is $1.48\times10^{18}\ \text{cm}^{-3}$ (the nominal channel doping concentration), as shown in Fig. 1(a). The cube of $(80\ \text{nm})^3$ is then partitioned into sub-cubes of $(16\ \text{nm})^3$. The number of dopants in the sub-cubes may vary from zero to 14, and the average number is six, as shown in Figs. 1(b), 1(c), and 1(f). Then the coordinates of discrete dopants in these sub-cubes are equivalently mapped into the corresponding coordinates in device channel region for the 3D device simulation, as shown in Fig. 1(d). The device simulation is performed by solving a set of 3D drift-diffusion equations with density gradient quantum correction [8, 9]. The step function is used to include the discrete dopant effect into the source of the Poisson equation. The step function $H(x,y,z) = 1$, for $x \geq 0$, $y \geq 0$, and $z \geq 0$; $H(x,y,z) = 0$, otherwise. The effect of the discrete dopant is considered by including the following term into the source doping concentration of the Poisson equation

$$N_A = \sum_{i=0}^{k} N_A^{dopant} \left(H(x-x_l, y-y_l, z-z_l) - H(x-x_u, y-y_u, z-z_u)\right), \qquad (1)$$

k is numbers of dopant in the device channel. N_A^{dopant} is the associated doping concentration for a dopant within a box. The volume of the box is defined by two coordinates, the lower point (x_l, y_l, z_l) and the upper point (x_u, y_u, and z_u). To calculate the numerical solution of the 3D device transport equations, we first decouple

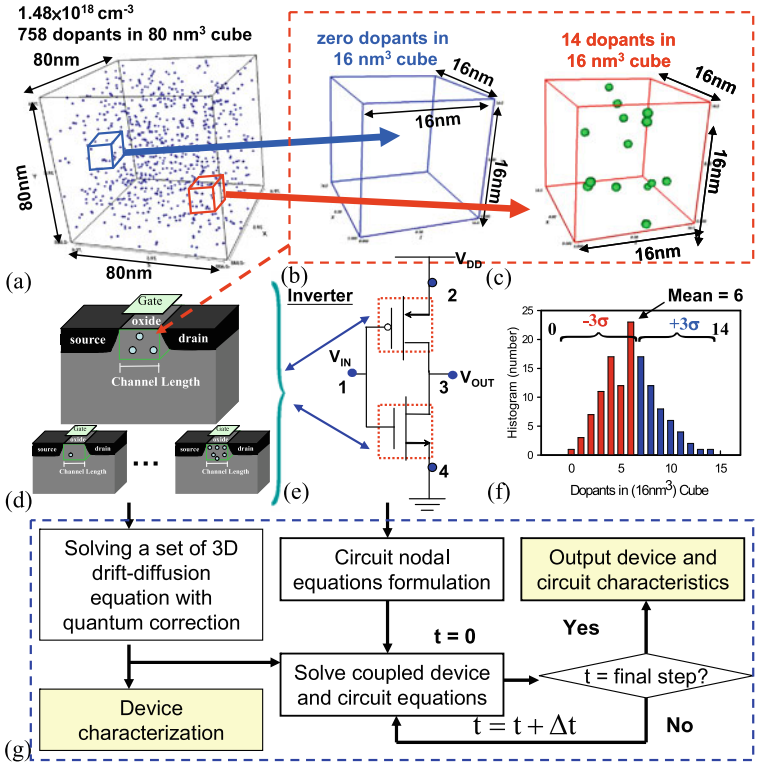


Fig. 1: a Discrete dopants randomly distributed in the $(80\ \text{nm})^3$ cube with the average concentration $1.48\times10^{18}\ \text{cm}^{-3}$. The dopants in sub-cubes of $(16\ \text{nm})^3$ may vary from zero to 14 (the average number is six), [(**b**), (**c**), and (**f**)]. **d** The sub-cubes are then mapped into 3D device channel region for device characterization. **e** A CMOS inverter for the analysis of circuit characteristic fluctuations, where the upper device is the P-MOSFET and the lower one is the N-MOSFET. **g** The simulation flow for device and circuit-device coupled simulations

the coupled partial differential equations by the Gummels decoupling method. The device transport equations are approximated by the finite volume method over a non-uniform mesh. Then the nonlinear algebraic equations are solved with the monotone iteration method [12] on our parallel computing system [10, 11]. An inverter circuit is then adopted as an example for estimating the circuit characteristics fluctuations, as shown in Fig. 1(e). The circuit nodal equations are then formulated (node1: $V_1 = V_G$, node2: $V_2 = V_{DD}$, node3: $I_{d,P-MOSFET} = I_{d,N-MOSFET}$, node4: $V_4 = 0$, for example). Currently, there is no well-established compact model available for describing the discrete-dopant-induced nonlinear device characteristic fluctuations, instead of using a compact modeling approach, the circuit nodal equations are coupled with device transport equations and solved simultaneously to examine the circuit characteristic fluctuations [13, 14]. The simulation flow for the proposed device and circuit-device coupled simulations is shown in Fig. 1(g). The large-scale

simulation technique is statistically sound for random dopant fluctuation characterization.

3 Results and Discussion

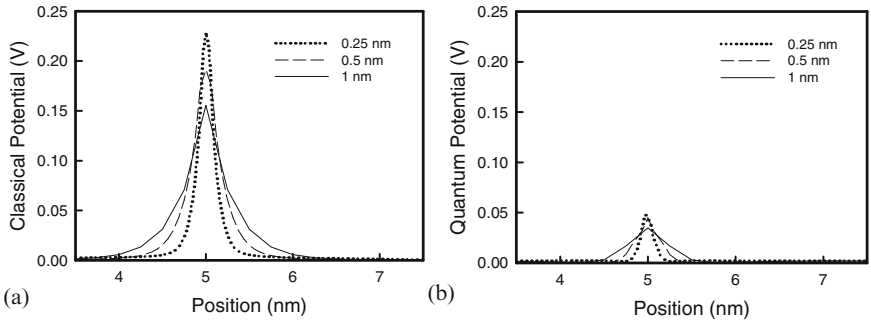


Fig. 2: Potential profiles for **a** classical and **b** quantum potential with different mesh size

Figure 2(a) and 2(b) illustrate the mesh size dependence of the classical and quantum mechanical potentials for a single discrete dopant within the silicon channel. In the "atomistic" simulation, the key point to study random impurities induced fluctuation relies on how to introduce the microscopic non-uniformity of localized impurity distributions inside the device. In conventional drift-diffusion approach for a large device size, the number of impurities included in each mesh exceeds one and the equivalent doping concentration does not change abruptly at every mesh node. Also, the dopant density at each mesh node changes gradually and the non-uniformity of impurity arrangement is averaged.

However, for the nanoscale transistor, the corresponding number of impurities is significantly reduced. Most meshes contain no dopant or, at most, one dopant. The dopant density at each mesh node changes its order of magnitude and behaves like a δ-function. The resolution of individual impurities for the conventional drift-diffusion simulation using a fine mesh creates problems of singularities in the Coulomb potential, as shown in Fig. 2(a). The sharp Coulomb potential wells may un-physically trap majority carriers, reduce the mobile electron concentration, modify the depletion region, and alter the threshold voltage (V_{th}). Therefore, the density gradient quantum correction [8, 9] is used to handle the discrete dopant effect by properly introducing the related quantum mechanical effects, as plotted in Fig. 2(b). The quantum mechanical potential shows less sensitivity to the mesh size and is quite similar for mesh spacing below 0.5 nm. We notice that the potential barrier of the Coulomb well is about 45 mV, which roughly corresponds to the ground state of a hydrogenic model of an impurity in silicon.

Figure 3(a) shows the I_D-V_G characteristics of the discrete-dopant-fluctuated 16-nm-gate planar MOSFETs, where the solid line shows the result of the nominal case (1.48×10^{18} cm^{-3} continuously doping concentration), and the dashed lines are

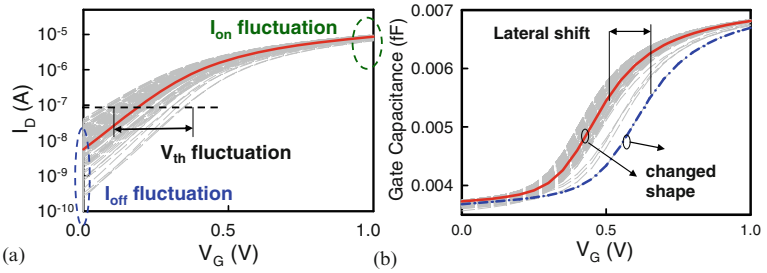


Fig. 3: Fluctuations of **a** I_D-V_G **b** and C-V curves for the studied 16-nm-gate planar MOSFETs

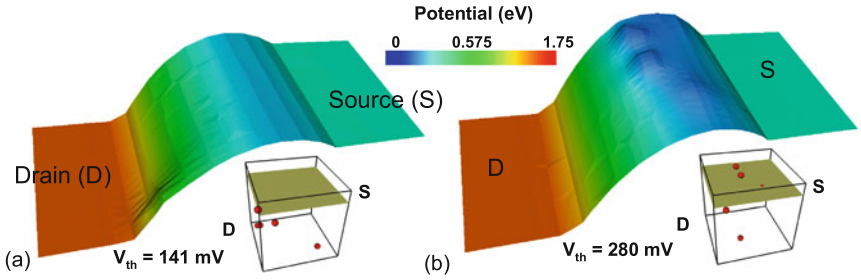


Fig. 4: Cutting-plane plots of the off-state potential profiles ($V_G = 0$ V; $V_D = 1$ V) for the simulated device with the same dopant number (six dopants) in channel region but with different V_{th}

discrete-dopant-fluctuated devices. The fluctuations of the on- and off-state currents (I_{on} and I_{off}) and V_{th} characteristics are observed. The detailed physical mechanism was described somewhere else [3–5]. Figure 3(b) shows the capacitance-voltage (C-V) characteristics of the discrete-dopant-fluctuated 16-nm-gate planar MOSFETs. The lateral shift and the changed shape for the C-V curves are observed. The lateral shift of gate capacitance results from the variation of V_{th} and may be described by the correspond parameters in a compact model. However, the changed shape of the C-V curves result from the position of discrete dopants in the channel, and it is hard to be described by any compact modeling approach [8, 9]. Figure 4 compares the off-state potential profiles for two devices with the same dopant number (six dopants) in the channel region but with different V_{th}. The potential barriers in Fig. 4 are induced by the corresponding dopants within the device channel. The different distribution of discrete dopants may induce different potential profiles and thus alter the device's transport characteristics. The V_{th} difference between Figs. 4(a) and 4(b) is about 139 mV, which is 99% of the nominal V_{th}, 140 mV. Therefore, instead of using a compact modeling approach, we have to use device simulation, and a circuit and device coupled simulation approach to capture the nonlinear variations induced by the discrete-dopant-position effect.

Figure 5(a) shows the voltage transfer curves for the discrete-dopant-fluctuated 16-nm-gate CMOS inverters. Two points on the voltage transfer curve determine the noise margins of the inverter. These are the maximum permitted logic "0" at the input, V_{IL}, and the minimum permitted logic "1" at the input, V_{IH}. The two

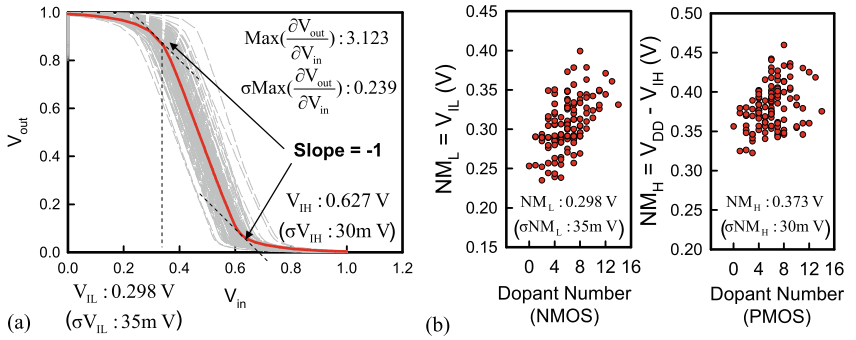
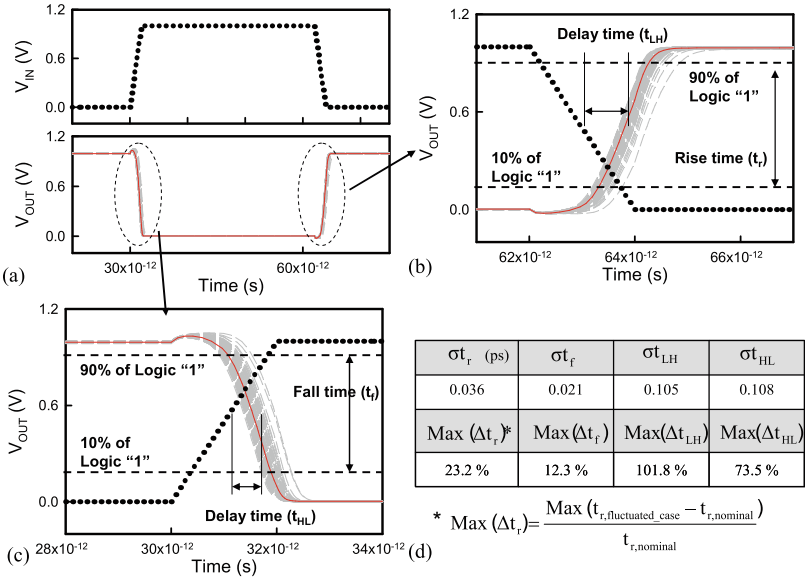


Fig. 5: a Voltage transfer curves for the studied 16-nm-gate planar MOSFET circuit. **b** Noise margins, NM_L and NM_H, as a function of the dopant number in the N-MOSFET and P-MOSFET

points on the voltage transfer curve are defined as those values of V_{in} where the incremental gain is unity; the slope -1 V/V. The nominal value and fluctuations of the V_{IL} and V_{IH} are shown in the insets of Fig. 5(a). The V_{IL} fluctuation is larger than the V_{IH} due to the larger V_{th} fluctuation of the N-MOSFET than the P-MOSFET. In the inverter circuit, the maximum slope of the voltage transfer curve implies the maximum voltage gain of the inverter. Therefore, the voltage gain fluctuation of the inverter is estimated, which is about 7% of the nominal value, as shown in the inset of Fig. 5(a). Noise margins for the logic "0" and "1", NM_H and NM_L, as a function of the dopant number are plotted in Fig. 5(b), where the NM_H and NM_L are defined. The NM_L is increased with the increasing dopant number in the N-MOSFET due to the increased V_{th} of device. For the NM_H, as numbers of dopant in the P-MOSFET increases, the increased V_{th} of device may decrease the V_{IH} of voltage transfer curve and thus increase the NM_H. We notice that even for cases with the same number of dopants within device channel, their noise margins are still quite different due to the different distribution of random dopants. The noise margins of the inverter circuit may be increased as dopant number increases; however, the fluctuations of the noise margins are also increased due to the more sources of fluctuation in the device channel region.

Figure 6 shows the timing characteristics of the CMOS inverter. The input and output signals are shown in Fig. 6(a). Figures. 6(b) and 6(c) are the zoom-in plots for the fall and rise transition characteristics of the output signal, where the rise time (t_r), the fall time (t_f), low-to-high delay time(t_{LH}) and high-to-low delay time (t_{HL}) are defined in the insets. The timing fluctuations are consequently summarized in Fig. 6(d). For the studied inverter circuits, the t_r fluctuation is larger than the t_f fluctuation because of the smaller driving capability of the P-MOSFET than that of the N-MOSFET. The device with the larger driving capability may require less time to charge and discharge the load capacitance and thus exhibits less timing fluctuations. The t_r and t_f fluctuations may not play an important role in timing characteristics; however, their maximum difference are about 23% and 12%, which bring a significant impact on timing. The delay time is dependent on the starting point of the signal transition, for example the time of 90% of the logic "1" for t_{HL} and the time of 10%



σt_r (ps)	σt_f	σt_{LH}	σt_{HL}
0.036	0.021	0.105	0.108
Max $(\Delta t_r)^*$	Max (Δt_f)	Max(Δt_{LH})	Max(Δt_{HL})
23.2 %	12.3 %	101.8 %	73.5 %

* $\text{Max}(\Delta t_r) = \dfrac{\text{Max}(t_{r,\text{fluctuated\_case}} - t_{r,\text{nominal}})}{t_{r,\text{nominal}}}$

Fig. 6: a Input and output signals for the discrete-dopant-fluctuated 16-nm-gate inverter circuits. **b**, **c** Zoom-in plots for the fall and rise transitions, where the insets define the rise, fall, high-to-low, and low-to-high delay times. **d** Summarized timing characteristic fluctuations

of the logic "1" for t_{LH}. Since the time of 90% and 10% of the logic "1" are related to the V_{th} of the N-MOSFET and P-MOSFET, respectively, the t_{HL} fluctuation is larger than the t_{LH} fluctuation due to the larger V_{th} fluctuation of the N-MOSFET. For the fall transition characteristics, the signal falls as the N-MOSFET is turned on. Therefore, as the V_{th} of the N-MOSFET is increased, the starting point of the fall transition is delayed. The t_{HL} is increased as the dopant number of N-MOSFET increases. Moreover, the t_{HL} fluctuation is increased as numbers of dopant increases due to the more sources of fluctuation inside device channel. Similarly, we can infer that the t_{HL} and t_{HL} fluctuation are increased as the dopant number of P-MOSFET increases.

4 Conclusions

Statistical variability introduced by discreteness of charge and granularity of matter could not be completely eliminated by advanced process control and already critically affects timing issues in digital logic circuits. In this paper, a large-scale 3D "atomistic" circuit-device coupled simulation approach has been implemented to investigate the discrete-dopant-induced characteristic fluctuations in nano-CMOS digital circuits. The quantum mechanical potential is less sensitive to the mesh size and quite similar for mesh spacing below 0.5 nm. The quantum mechanical potential barrier is about 45 mV, which roughly corresponds to the ground state of a hydrogenic model of an impurity in silicon. According to the proposed simulation

scenario, the nonlinearity of device characteristic fluctuations including discrete-dopant-number and discrete-dopant-position effects have been estimated in terms of surface potential, I-V, and C-V curves. For the discrete-dopant fluctuated 16-nm-gate inverter circuit, The maximum difference of t_f, t_r, t_{HL} and t_{LH} are about 23%, 12%, 101.8% and 73.5%, respectively. The significant timing variation may result in significant timing violation and delay in state-of-art nano-CMOS circuits and systems. The study may benefit the development of next generation nanoscale circuits and systems, where the design paradigms have to change to acclimatize the even increasing variability. Besides the inverter circuits, the simulation approach could be further applied for various digital and analog circuits characteristic fluctuations. Also, the fluctuation suppression techniques could be verified and developed.

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