Complementary-LVTSCR ESD Protection Circuit for Submicron CMOS VLSI/ULSI

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***Abstract*—There are one LVTSCR device merged with short-channel NMOS and another LVTSCR device merged with short-channel PMOS in complementary style to offer effective and direct ESD discharging paths from the input or output pads to VSS and VDD power lines. The trigger voltages of LVTSCR devices are lowered to the snapback-breakdown voltages of short-channel NMOS and PMOS devices. This complementary-LVTSCR ESD protection circuit offers four different discharging paths to one-by-one bypass the four modes of ESD stresses at the pad, so it can effectively avoid the unexpected ESD damages on internal circuits. Experimental results show that it can perform excellent ESD protection capability in a smaller layout area as compared to the conventional CMOS ESD protection circuit. The device characteristics under high-temperature environment of up to 150°C is also experimentally investigated to guarantee the safety of this proposed ESD protection circuit.**

I. Introduction

ELECTROSTATIC discharge (ESD) protection for submicron CMOS IC's is much degraded due to both the smaller feature size of scaled-down devices and the advanced CMOS technologies of Light-Doped Drain (LDD) structure and silicided-diffusion process [1]. To improve ESD protection capability of CMOS on-chip ESD protection circuit, the lateral SCR device had been used as a main protection element to bypass ESD stress. The trigger voltage of lateral SCR device in the submicron CMOS process is around 30 $\sim$ 50 V. But, the gate-oxide thickness in 0.6 $\sim$ 0.8 μm CMOS process is only around 150 $\sim$ 200 Å. This gate oxide will be damaged by a voltage about 15 $\sim$ 20 V across it because the dielectric breakdown strength of SiO_2 is about 10 MV/cm. Thus, the lateral SCR device with trigger voltage of 30 $\sim$ 50 V cannot protect the gate oxide of CMOS input stage alone without other secondary-protection elements.

If the trigger voltage of lateral SCR device can be reduced below the gate-oxide breakdown voltage of CMOS devices, the lateral SCR device can perform the highest ESD protection capability in a smallest layout area (compared with other ESD protection elements such as diode, thick-oxide device, gate-oxide device, and parasitic bipolar device in CMOS IC's) [2]. To lower the trigger voltage of lateral SCR device in submicron CMOS technologies, some efforts had been contributed to modify the structure of lateral SCR device [3], [4]. In [3], a modified structure of lateral SCR device called as LVTSCR (Low-Voltage Trigger SCR) had been reported with its trigger voltage lower than the gate-oxide breakdown voltage.

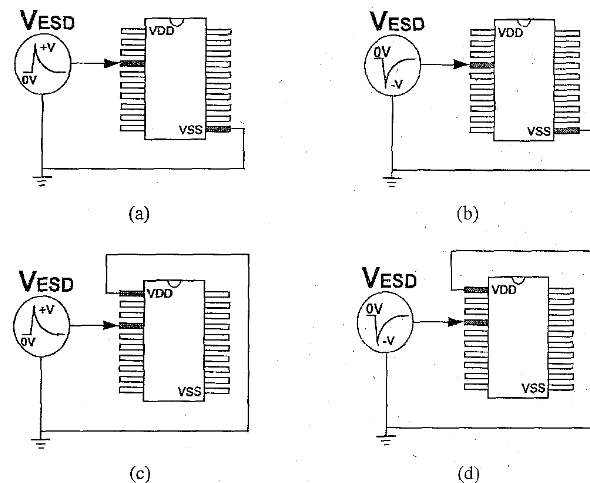

Fig. 1. A schematic diagram to show the four modes of ESD stresses: (a) PS-mode, (b) NS-mode, (c) PD-mode, and (d) ND-mode.

Since the ESD voltages may have positive or negative polarities to both VDD and VSS(ground) nodes, there are four different ESD-stress worst cases at each input or output pins as shown in Fig. 1.

1) PS mode: ESD stress at a pin with positive voltage polarity to VSS(GND) pin when VDD pin and other input/output pins are floating.
2) NS mode: ESD stress at a pin with negative voltage polarity to VSS(GND) pin when VDD pin and other input/output pins are floating.
3) PD mode: ESD stress at a pin with positive voltage polarity to VDD pin when VSS(GND) pin and other input/output pins are floating.
4) ND mode: ESD stress at a pin with negative voltage polarity to VDD pin when VSS(GND) pin and other input/output pins are floating.

These ESD voltages could damage both NMOS and PMOS devices in the input stage or output driver of CMOS IC's. In [3], the LVTSCR device is only arranged between the output or input pad to VSS(GND) node. There is no ESD protection element arranged between the pad and VDD node. For the ND-mode or PD-mode ESD stresses, the ESD current/voltage is first diverted from the input pin to VSS power line of CMOS IC through the LVTSCR device, and then this ESD

Manuscript received June 8, 1995; revised October 9, 1995. The review of this paper was arranged by Editor T. Nakamura.

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Publisher Item Identifier S 0018-9383(96)02695-0.

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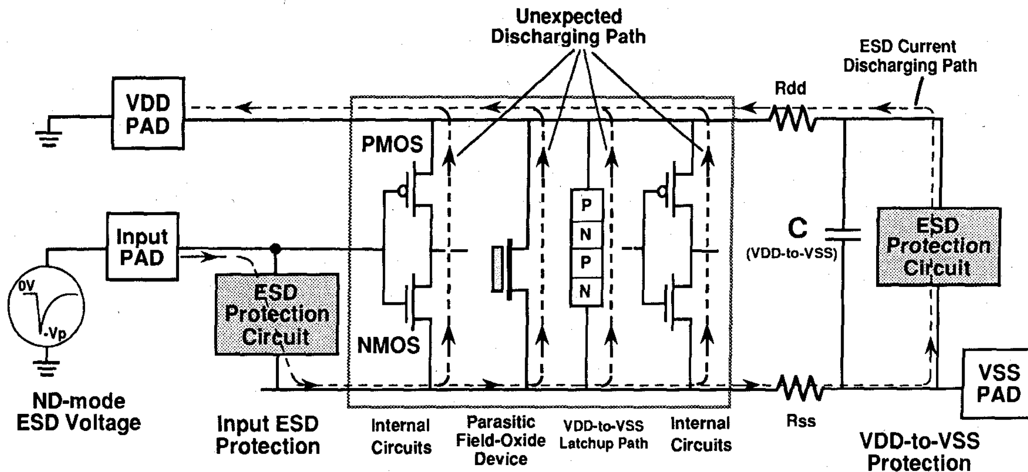


Fig. 2. A schematic diagram to show the unexpected discharging paths in the internal circuits but beyond the ESD protection circuits of CMOS IC's due to ND-mode ESD stress on the input pad.

current/voltage flows through the VDD-to-VSS ESD protection element to VDD power line. Finally, the ESD current/voltage goes out of CMOS IC from the VDD pin. Due to the parasitic resistance and capacitance of VSS/VDD power lines in CMOS IC's as well as voltage drops on the input-to-VSS and VDD-to-VSS ESD protection elements, such nondirect ESD discharging path had been reported to cause some unexpected ESD damages on internal circuits beyond ESD protection circuits [5]–[9]. Fig. 2 shows a schematic diagram to explain the unexpected discharging paths in the internal part of a CMOS IC under ND-mode ESD-stress condition, in which there is only an input-to-VSS ESD protection circuit at the input pad. The ND-mode ESD-stress voltage between input pad and VDD pad is transferred to cause voltage stress between the VSS and VDD power lines. If this voltage stress between VSS and VDD power lines can not be effectively and quickly bypassed through the VDD-to-VSS ESD protection circuit, this ND-mode ESD voltage will cause unexpected ESD damages on internal circuits. In [5]–[6], the unexpected ESD damages had been found to occur in the VDD-to-VSS latchup paths of CMOS IC's. This ND-mode ESD voltage between VSS and VDD power lines had also caused damages on the parasitic n-type field-oxide devices [5]–[7], which is parasiticly formed by two $N+$ diffusions separated by the field oxide. Of course, this ESD voltage between VDD and VSS power lines caused ESD damages on the devices of internal circuits [8]–[9]. Thus, an input ESD protection circuit for advanced submicron CMOS IC's should perform effective and direct ESD discharging paths from the input pad to both VSS and VDD power lines. This is especially necessary for a submicron CMOS VLSI/ULSI with larger die size and longer VDD/VSS power lines which often surround the whole chip.

In this paper, to overcome above problem of nondirect ESD discharging path and to employ the advantages of high ESD protection capability and low trigger voltage of LVTSCR device with small layout area, a new complementary-LVTSCR ESD protection circuit is proposed [10]. In this complementary-LVTSCR ESD protection circuit, there is one NMOS-triggered LVTSCR device arranged from the pad to VSS power line and another PMOS-triggered LVTSCR device is arranged from VDD power line to the pad to perform direct discharging paths for the four modes of ESD stresses. Thus, this proposed ESD protection circuit can offer effective ESD protection without causing unexpected ESD damages on the internal circuits.

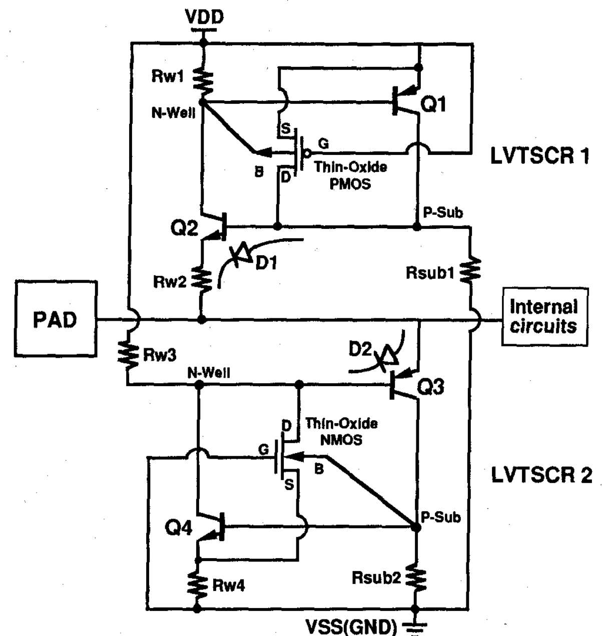


Fig. 3. The complementary-LVTSCR ESD protection circuit.

II. COMPLEMENTARY-LVTSCR ESD PROTECTION CIRCUIT

A. Circuit and Device Configurations

The proposed complementary-LVTSCR ESD protection circuit for submicron CMOS IC's is shown in Fig.

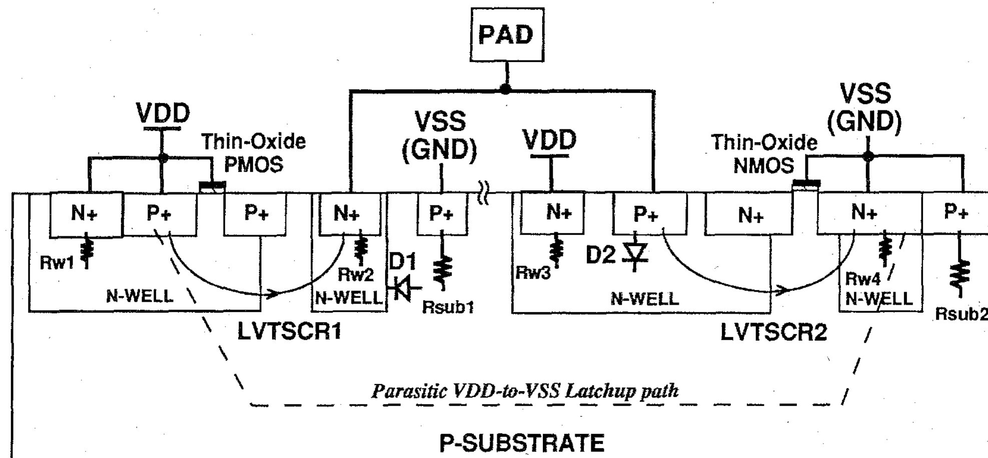


Fig. 4. The schematic cross-sectional view of the complementary-LVTSCR devices (realized in P-substrate/N-well CMOS process).

3. The corresponding schematic cross-sectional view of complementary-LVTSCR device is shown in Fig. 4, where the P-substrate N-well CMOS process is used to demonstrate the complementary-LVTSCR structures. They can be also implemented in N-substrate P-well CMOS process as well if appropriate modifications are made. There are two LVTSCR structures in this complementary-LVTSCR ESD protection circuit. The LVTSCR1 device is arranged between VDD power line and input (or output) pad with its cathode connected to the pad. The LVTSCR2 device is arranged between input (or output) pad and VSS(GND) power line with its anode connected to the pad.

The LVTSCR1 device is formed by a lateral SCR device (composed by BJT's Q1 and Q2) with a short-channel thin-oxide PMOS which are merged together to lower the trigger voltage of lateral SCR device, as shown in the left-hand part of Fig. 4. The Q1 is a parasitic vertical p-n-p bipolar junction transistor (BJT) which is formed by a $P+$ diffusion connected to VDD as its emitter in an N-well, the N-well connected to VDD through a parasitic well resistance Rw1 as its base, and the P-substrate connected to VSS (or ground) through a parasitic substrate resistance Rsub1 as its collector. The Q2 is a parasitic lateral n-p-n BJT which is formed by an $N+$ diffusion in an N-well connected to the pad through a parasitic well resistance Rw2 as its emitter, P-substrate (also as the collector of BJT Q1) as its base, and an adjacent N-well (also as the base of BJT Q1) as its collector. BJT's Q1 and Q2 are cross-coupled to form a lateral SCR structure. The thin-oxide PMOS is composed by a nonconnection $P+$ diffusion across the N-well/P-substrate junction as its drain, N-well connected to VDD as its bulk, and a $P+$ diffusion in the N-well of bulk as its source. The gate of thin-oxide PMOS is connected to VDD to ensure itself off in the normal-operation conditions of CMOS IC's. The purpose of inserting a short-channel thin-oxide PMOS into the lateral SCR structure is to use the drain of thin-oxide PMOS in the snapback-breakdown condition to trigger on the lateral SCR structure during ESD stress. Therefore, the trigger voltage of LVTSCR1 device is equivalent to the snapback-breakdown voltage of the short-channel thin-oxide PMOS rather than the original trigger voltage (about 30 $\sim$ 50 V) of the lateral SCR device. The holding voltage of LVTSCR1 is still the same as the original holding voltage (about $\sim$1 V) of a lateral SCR device.

Similarly, the LVTSCR2 device is formed by a lateral SCR device (composed by BJT's Q3 and Q4) with a short-channel thin-oxide NMOS merged together to lower the trigger voltage of lateral SCR device, as shown in the right-hand part of Fig. 4. Q3 is a parasitic vertical p-n-p BJT which is formed by a $P+$ diffusion connected to pad as its emitter in an N-well, the N-well connected to VDD through a parasitic well resistance Rw3 as its base, and the P-substrate connected to VSS (ground) through a parasitic substrate resistance Rsub2 as its collector. Q4 is a parasitic lateral n-p-n BJT which is formed by an $N+$ diffusion in an N-well connected to VSS through a parasitic well resistance Rw4 as its emitter, P-substrate (collector of BJT Q3) as its base, and an adjacent N-well (base of BJT Q3) as its collector. Q3 and Q4 are cross-coupled to form a lateral SCR structure. The thin-oxide NMOS is composed by a nonconnection $N+$ diffusion crossing the N-well/P-substrate junction as its drain, P-substrate connected to VSS as its bulk, and an $N+$ diffusion extended out of an N-well (emitter of BJT Q4, connected to VSS) as its source. The gate of thin-oxide NMOS is connected to VSS to ensure itself off in the normal-operation conditions of CMOS IC's. The purpose of inserting a short-channel thin-oxide NMOS into the lateral SCR structure is to use the drain of thin-oxide NMOS in its snapback-breakdown condition to trigger on the lateral SCR structure during ESD stress. Therefore, the trigger voltage of LVTSCR2 device is equivalent to the snapback-breakdown voltage of the short-channel thin-oxide NMOS rather than the original trigger voltage (about 30 $\sim$ 50 V) of the lateral SCR device [3]. The holding voltage of LVTSCR2 is also the same as the original holding voltage (about $\sim$1 V) of a lateral SCR device.

There also exist two junction diodes D1 and D2 in the complementary-LVTSCR structure. D1 (D2) is merged into the LVTSCR1 (LVTSCR2) device to save layout area. The cathode of diode D1, formed by an N-well in P-substrate,

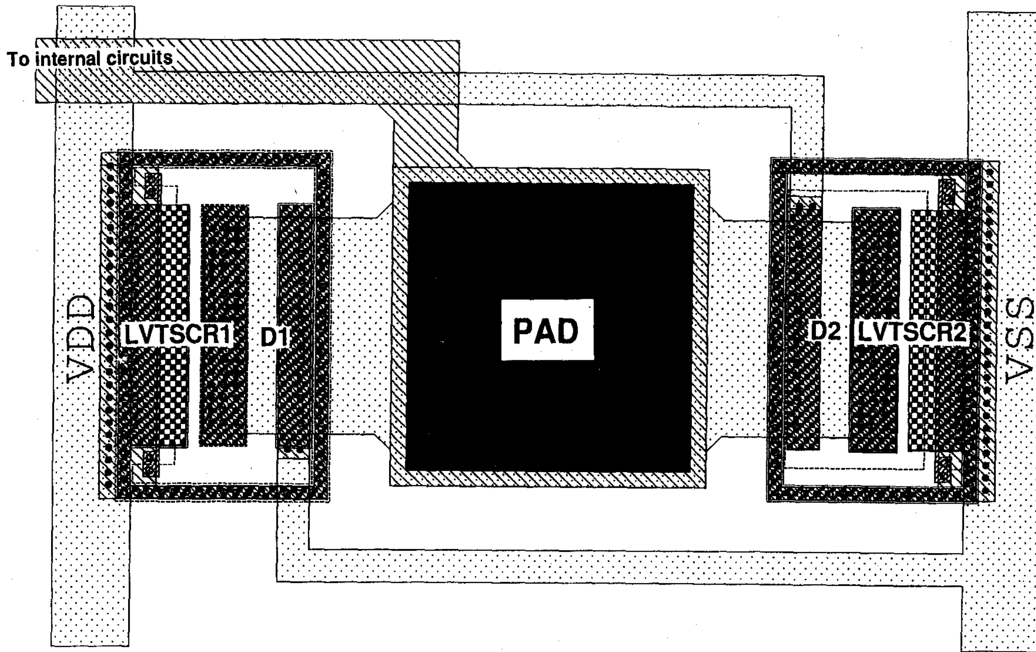


Fig. 5. Layout example of complementary-LVTSCR ESD protection circuit.

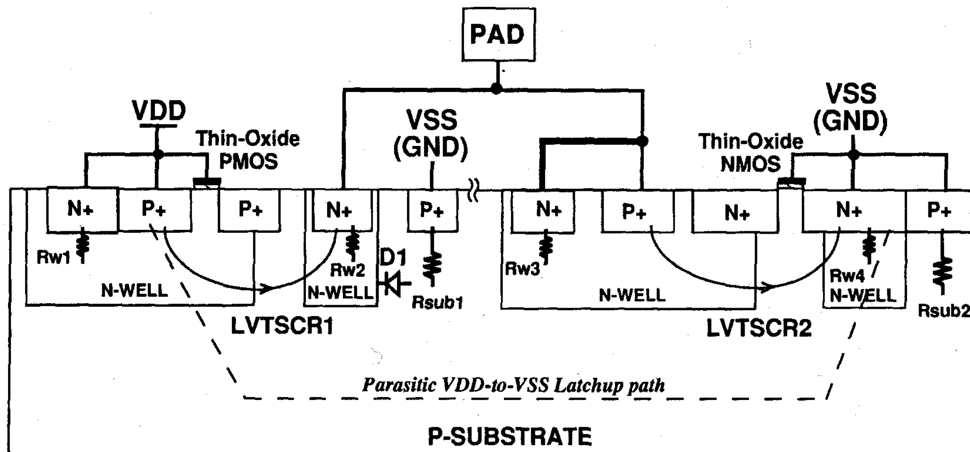


Fig. 6. Modified structure of complementary-LVTSCR ESD protection circuit for application in the mixed-voltage interface.

is connected to the pad through a parasitic N-well resistor Rw2 and its anode is connected to VSS(GND) through the P-substrate resistor Rsub1. The anode of diode D2, formed by a $P+$ diffusion in an N-well, is connected to the pad and its cathode is connected to VDD through a parasitic N-well resistor Rw3. D1 clamps the low voltage level of input (or output) signals on the pad to about VSS $-$ 0.6 V. D1 also performs an ESD discharging path from VSS to the pad. D2 clamps the high voltage level of input (or output) signals on the pad to about VDD $+$ 0.6 V. D2 also performs an ESD discharging path from the pad to VDD.

A typical layout example of this complementary-LVTSCR ESD protection circuit is shown in Fig. 5, which is realized by a 0.8-μm single-ploy double-metal twin-well CMOS technology. In Fig. 5, the LVTSCR1 and LVTSCR2 are separated by the pad and also surrounded by latchup guard rings to prevent VDD-to-VSS latchup. The parasitic VDD-to-VSS latchup path in this complementary-LVTSCR structure is also shown in Fig. 4 by the dashed line from VDD to GND(ground). This VDD-to-VSS latchup path can be broken by the guard rings and the emitter-shorting method [11]. With suitable prevention, this complementary-LVTSCR ESD protection circuit can be free of VDD-to-VSS latchup issue under 5-V CMOS operations.

B. Circuit Operating Principles

In normal CMOS operations with 5-V VDD and 0-V VSS power supplies, diodes D1 and D2 clamp voltage level on the pad between about 5.6 V and $-$0.6 V. The gates of thin-oxide

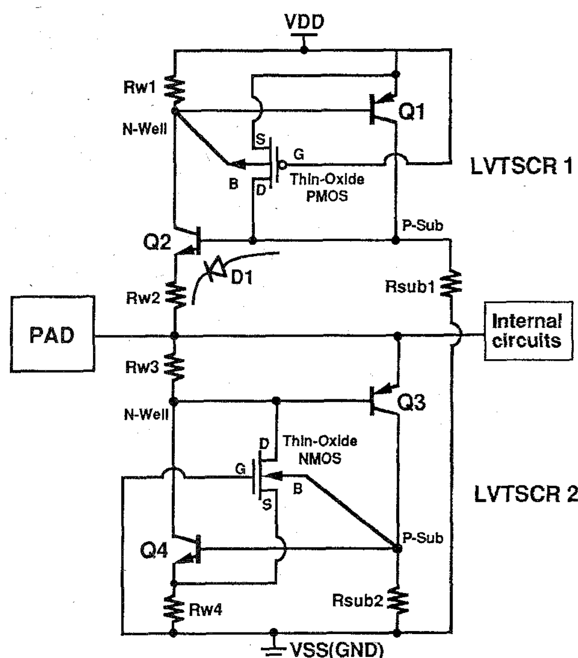


Fig. 7. Equivalent circuit diagram of the modified structure in Fig. 6.

TABLE I

	Conventional CMOS ESD protection circuit				Complementary-LVTSCR ESD protection circuit			
	PMOS		NMOS		LVTSCR1		LVTSCR2	
Layout Area (μmXμm)	94.0X145.2		94.0X145.2		66.7X108.6		65.2X107.0	
ESD-Stress condition	PD-mode	ND-mode	PS-mode	NS-mode	PD-mode	ND-mode	PS-mode	NS-mode
HBM ESD failure voltage (V)	above 8000 *	−3250	5500	above −8000 *	above 8000 *	−8000	above 8000 *	above −8000 *
MM ESD failure voltage (V)	400	−200	300	−500	700	above −800 *	650	above −800 *

* limited by the ESD testing machine (ESD Simulator : HANWA HED-S5000)

PMOS (in LVTSCR1) and NMOS (in LVTSCR2) are shorted to their sources, so LVTSCR1 and LVTSCR2 remain inactive in variable normal operating conditions of CMOS IC's.

When PS-mode ESD event occurs, the positive ESD voltage is diverted to the drain ($N+$ diffusion crossing the N-well/P-substrate junction) of thin-oxide NMOS through the $P+$ diffusion/N-well/$N+$ diffusion forward-conducting path. The thin-oxide NMOS in LVTSCR2 is turned on by means of drain snapback breakdown to first clamp positive ESD voltage on the pad to the voltage level of snapback-breakdown voltage (about 13 $\sim$ 16 V) of thin-oxide NMOS. The discharging current from the $N+$ diffusion in N-well to P-substrate due to the snapback-breakdown drain of thin-oxide NMOS helps and leads to latchup happen in the lateral LVTSCR2 device. Once the latchup happens in the lateral LVTSCR2 device, ESD current is mainly discharged through the lateral SCR structure. After then, the ESD voltage on the pad is clamped by the holding voltage of turned-on lateral SCR structure to about 1 $\sim$ 2 V so as to protect the internal circuits which are connected to this pad. Thus, this LVTSCR2 device can effectively protect CMOS IC's against PS-mode ESD stress alone without other secondary protection elements as those shown in [4].

In NS-mode ESD-stress condition, diode D1 is forward conducting. So, the NS-mode ESD current can be directly discharged through diode D1. Diode in its forward-conducting condition can perform very well ESD protection.

In PD-mode ESD events, ESD stress occurs at the pad with positive polarity to VDD. The PD-mode ESD current can be directly discharged through diode D2 in its forward-conducting condition.

When ND-mode ESD event occurs, negative ESD voltage is diverted to the cathode of LVTSCR1 device ($N+$ diffusion in an N-well), through the P-substrate, and then to the drain ($P+$ diffusion crossing the P-substrate/N-well junction) of thin-oxide PMOS. The drain of thin-oxide PMOS breaks down and leads to latchup to occur in the lateral LVTSCR1 device. Once the latchup happens in LVTSCR1 device, the ESD current is mainly discharged through the lateral SCR structure. The negative ESD voltage on the pad is clamped by the holding voltage of turned-on lateral SCR structure to about $-1 \sim -2$ V so as to protect the internal circuits.

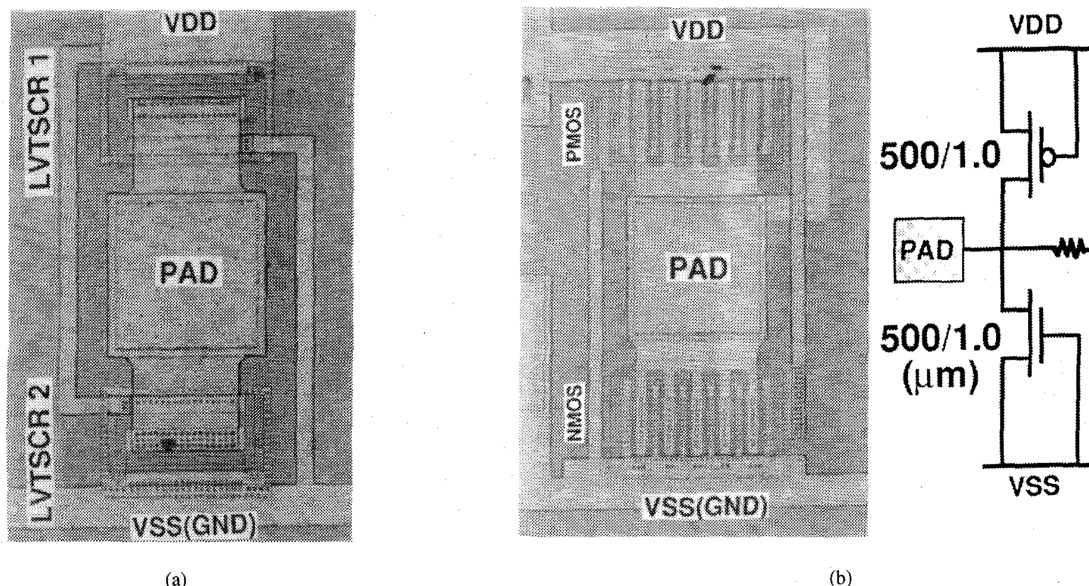
Due to high capability of power delivery in the SCR device, this complementary-LVTSCR ESD protection circuit can sustain high ESD stresses in a small layout area with a lower trigger voltage.

C. Modification for Application in Mixed-Voltage System

In mixed-voltage system, there are multiple VDD power supplies. For example, an IC in the mixed-voltage system has a VDD power supply of 5 V, but the other has its VDD power supply of 3 V. If this proposed complementary-LVTSCR ESD protection circuit is used in the input pad of 3-V IC but with the input signal coming from the output buffer of a 5-V IC, the 5-V input signal will cause a current flow from the 5-V VDD power supply toward the 3-V VDD power supply due to the forward conducting diode D2 in the LVTSCR2 structure. This limits the use of ESD-protection diode placed from the input pad to VDD.

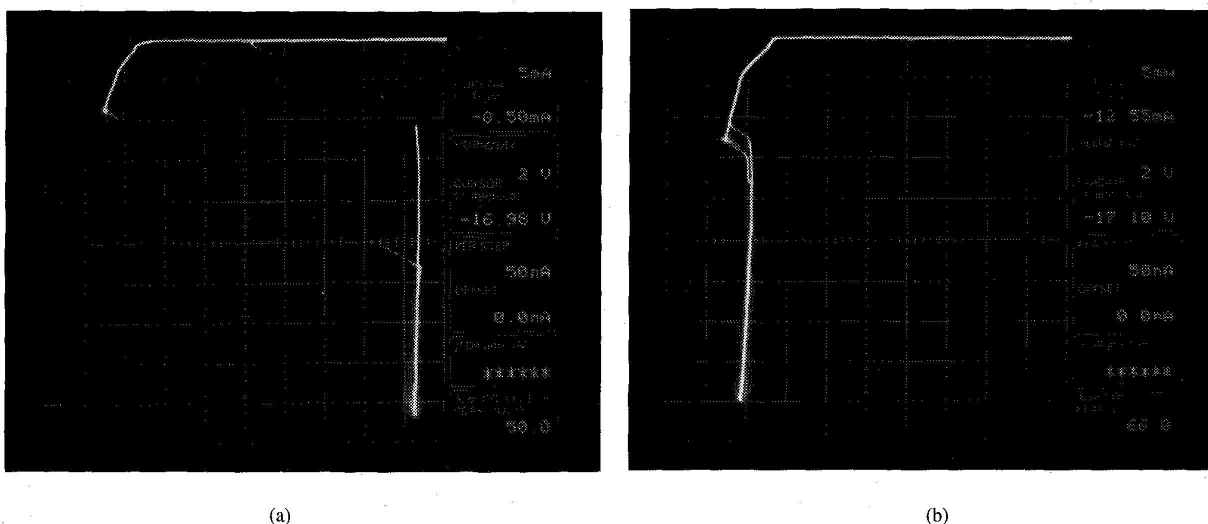
Besides, the DRAM products often with an on-chip substrate bias generator have a parasitic bipolar transistor if the input pin of DRAM has an ESD-protection diode or PMOS device from the input pad to VDD. This parasitic bipolar transistor will cause a current flow to the bias generator if the input signal voltage exceeds the VDD value. This also limits the use of diode D2 in the LVTSCR2 structure to protect the DRAM IC's with substrate bias generator.

From above discussion, the mixed-voltage interface and the on-chip substrate bias generator cause some limitations to place an ESD protection circuit between the input pad and VDD node. But, if an input pin has no input-to-VDD ESD protection circuit, the internal circuits are more sensitive to ND-mode ESD stress as shown in Fig. 2. Thus, mixed-voltage chip-to-chip interface I/O circuitry with ESD protection circuit must be designed to avoid ESD stress and prevent undesirable current leakage paths that cause system-level power loss. In [12]–[13], a five-stage diode string (comprising of $P+$ diffusion/N-well diodes) had been reported as an input-to-VDD ESD protection element for the mixed-voltage interface



(a) (b)

Fig. 8. Microphotography of test chip in (a) is the complementary-LVTSCR ESD protection circuit, in (b) is the conventional CMOS ESD protection circuit.



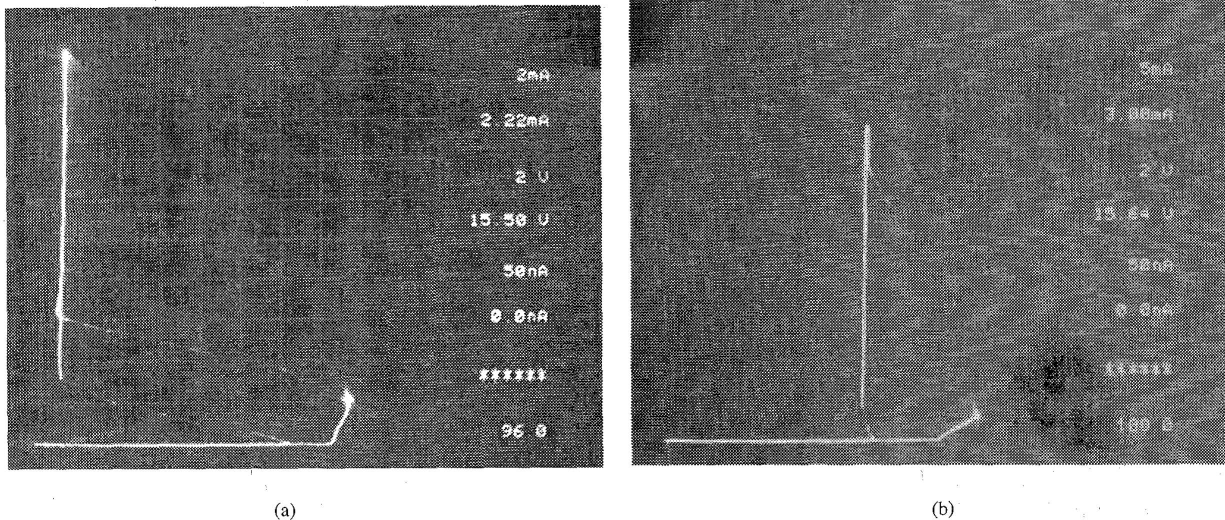
(a) (b)

Fig. 9. Measured I-V characteristics of (a) LVTSCR1 device in the complementary-LVTSCR ESD protection circuit, (b) gate-connected-to-source thin-oxide PMOS device in the conventional CMOS ESD protection circuit.

environments. In [13], it also reported another self-biased-well ESD circuit for the mixed-voltage interface environment.

If the parasitic diode D2 in LVTSCR2 structure of the proposed complementary-LVTSCR ESD protection circuit in Figs. 3 and 4 can be removed. This complementary-LVTSCR ESD protection circuit is still suitable as an effective ESD protection circuit for the input pin of mixed-voltage interface. The modified structure of this complementary-LVTSCR ESD protection circuit for mixed-voltage interface is shown in Fig. 6. The equivalent circuit of this modified structure is shown in Fig. 7. In Fig. 4, the diode D2 in the LVTSCR2 structure is formed by the $P+$ diffusion in the N-well which is connected to VDD through an $N+$ diffusion. If the connection of this $N+$ diffusion in the N-well is changed from VDD to the input pad as shown in Fig. 6, the N-well becomes self biased by the input signal and the function of diode D2 can be disabled. With modification in the connection of $N+$ diffusion in the N-well, this modified complementary-LVTSCR ESD protection circuit is still suitable to protect the input pins of CMOS IC's in mixed-voltage interface environments.

This modified complementary-LVTSCR ESD protection circuit can be also used to protect the DRAM IC's with substrate bias generator. Under this application, the $P+$ diffusion in P-substrate connected to VSS(GND) in Fig. 6 should be removed because of the negative substrate bias of DRAM IC's. Thus, the function of diode D1 is also removed, but this low-level voltage clamping function can be replaced by the thin-oxide NMOS in the LVTSCR2. The low-level voltage of



(a) (b)

Fig. 10. Measured I-V characteristics of (a) LVTSCR2 device in the complementary-LVTSCR ESD protection circuit, (b) gate-connected-to-source thin-oxide NMOS device in the conventional CMOS ESD protection circuit.

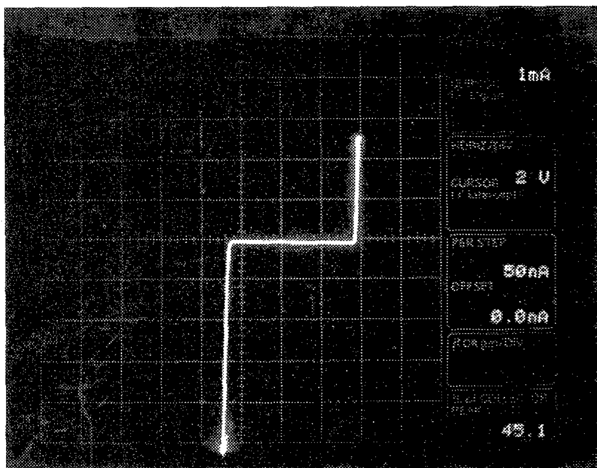


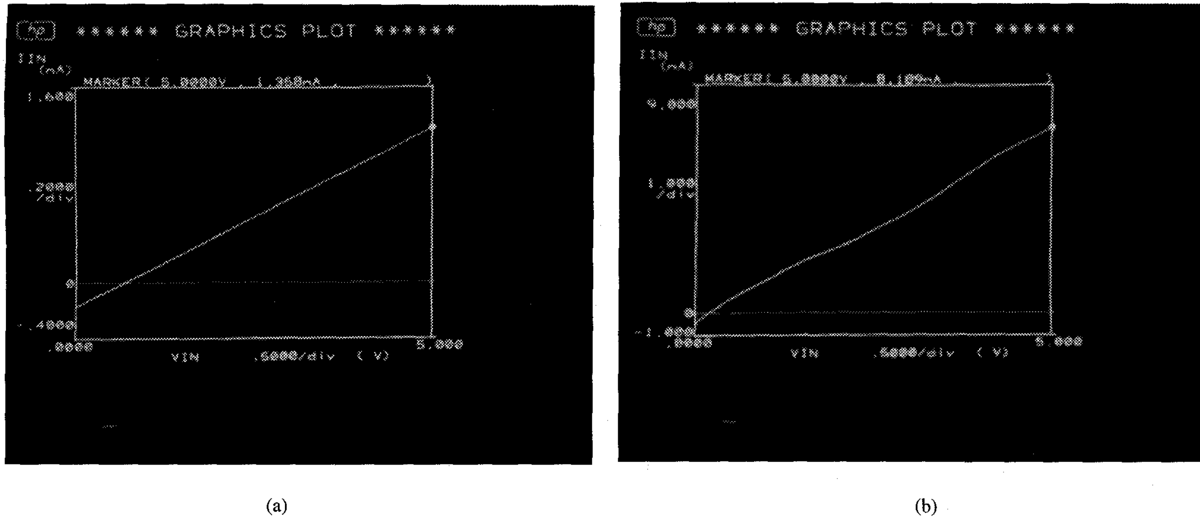
Fig. 11 Measured I-V characteristics of voltage clamping effect on the input signals at a pad with the fabricated complementary-LVTSCR ESD protection circuit. X axis (2 V/div.) is the input voltage applied at the pad with 5-V VDD and 0-V VSS, whereas the Y axis (1mA/div.) is the measured input current at the pad.

input signal becomes clamped at about VSS-Vthn, where Vthn is the threshold voltage of thin-oxide NMOS in the LVTSCR2 device.

With above modification to protect the mixed-voltage interface or the DRAM IC's with substrate bias generator, the ESD-protection operating principles are also a little different to the original design due to the absence of D2 or D1 diodes. The ND-mode ESD stress is still protected by LVTSCR1, and the PS-mode ESD stress is still protected by LVTSCR2. The NS-mode ESD stress can be protected by the thin-oxide NMOS under forward conducting condition in series with N-well resistance in the LVTSCR2 structure, if diode D1 is disabled in the case of DRAM IC's with substrate bias generator. But the PD-mode ESD stress has no direct discharging path in this modified complementary-LVTSCR ESD protection circuit due to the absence of diode D2. The PD-mode ESD voltage will be diverted to the floating VSS power line through LVTSCR2 and causes very small voltage drop (holding voltage of LVTSCR2) on the LVTSCR2 device. Then, the PD-mode ESD voltage goes through the VDD-to-VSS ESD protection element to VDD power line. In most cases, the VDD-to-VSS ESD protection element is a thin-oxide NMOS with its gate and source connected to VSS and its drain connected to VDD [14]. Thus, the PD-mode ESD voltage on the VSS power line goes through the forward conducting NMOS to VDD power line. So, the voltage drop from the input pad to VDD pad through above described path is equal to the holding voltage plus the NMOS threshold voltage. This voltage drop is less than 3 V, so the internal circuits can be still free to ESD damages. Although this PD-mode ESD discharging path involves with the floating VSS power line and the VDD-to-VSS ESD protection element, this condition is quite different to the ND-mode condition described in Fig. 2. In Fig. 2, the ND-mode ESD voltage causes VDD-to-VSS ESD-protection NMOS to break down. So, in that ND-mode condition, the minimum voltage drop between input pad and VDD pad is as high as the breakdown voltage of gate-ground NMOS, and it is about 15 $\sim$ 16 V in a 0.8-μm CMOS technology. This high voltage drop with the effect of parasitic resistance and capacitance in the ND-mode ESD-stress condition of Fig. 2 is the main reason to cause unexpected ESD damages on internal circuits but beyond the ESD protection circuit. Thus, with suitable modification, this proposed complementary-LVTSCR ESD protection circuit can still provide the mixed-voltage interface or DRAM IC's with excellent ESD-protection capability.

III. Experimental Results

A test chip to realize this complementary-LVTSCR ESD protection circuit has been designed and fabricated by a 0.8-μm CMOS technology with LDD structure. One of the test pads is shown in Fig. 8(a), which corresponds to the



(a) (b)

Fig. 12. Comparison of input leakage currents between (a) the complementary-LVTSCR ESD protection circuit and (b) the conventional CMOS ESD protection circuit with 5-V VDD and 0-V VSS. X axis (0.5 V/div.) is input voltage applied at the pad, whereas Y axis [0.2 nA/div. in (a); 1.0 nA/div. in (b)] is the measured input leakage current at the pad.

layout example in Fig. 5. In Fig. 8(b), a conventional CMOS ESD protection circuit, composed by a PMOS (from the pad to VDD) and an NMOS (from the pad to VSS) with gate shorted to source, is also fabricated in the same test chip as a comparing reference. In Fig. 8(a), the channel width/length of PMOS and NMOS inserted in LVTSCR1 and LVTSCR2 is 75/1.0 μm, and total layout area of LVTSCR1 (LVTSCR2) is only 66.7 × 108.6 (65.2 × 107.0) μm^2 which also includes a 4-μm latchup guard ring of $N+$ ($P+$) diffusion surrounding the whole LVTSCR1 (LVTSCR2) device. The channel width/length of PMOS and NMOS in the conventional CMOS ESD protection circuit of Fig. 8(b) is 500/1.0 μm, and the total layout area of each PMOS and each NMOS is 145.2 × 94.0 μm^2, respectively. The Human-Body Mode (HBM) and Machine Mode (MM) ESD testing results in four modes of ESD stresses are shown in Table I by the ESD failure criterion of 1-μA increase in leakage current below 7.1-V bias. The ESD tester machine is the HED-S5000 produced by *HANWA* company in Japan. The lowest ESD failure voltage of the four-mode ESD testing results at a pin is defined as the ESD failure threshold of the pin. The results show that the ESD failure threshold of conventional PMOS/NMOS ESD protection circuit is only 3250 V (200 V) but that of complementary-LVTSCR ESD protection circuit within a smaller layout area is up to 8000 V (650 V) in HBM (MM) ESD testing. This proposed complementary-LVTSCR ESD protection circuit performs 2.46 (3.25) times HBM (MM) ESD failure threshold in only 0.52 times layout area to that of conventional PMOS/NMOS ESD protection circuit. This verifies the excellent performance of this proposed ESD protection circuit in submicron CMOS technologies.

The turn-on characteristics of fabricated LVTSCR1 device is shown in Fig. 9(a), which is measured from the pad with grounded VDD but VSS floating (as the ND-mode ESD-stress condition). The trigger voltage of LVTSCR1 device is lowered to only -16.98 V and its holding voltage is -1.34 V with turn-on resistance of 6.72 Ω. The snapback-breakdown characteristics of thin-oxide PMOS in the conventional CMOS ESD protection circuit is also shown in Fig. 9(b), where the snapback-breakdown voltage is -17.10 V. The turn-on characteristics of fabricated LVTSCR2 device is shown in Fig. 10(a), which is measured from the pad with grounded VSS but VDD floating (as the PS-mode ESD-stress condition). The trigger voltage of LVTSCR2 device is lowered to only 15.50 V and its holding voltage is 1.02 V with turn-on resistance of 6.28 Ω. The snapback-breakdown characteristics of thin-oxide NMOS in the conventional CMOS ESD protection circuit is also shown in Fig. 10(b), where the snapback-breakdown voltage is 15.64 V. From Figs. 9 and 10, it has been verified that the LVTSCR1 (LVTSCR2) device is really triggered on by means of drain of thin-oxide PMOS (NMOS), which inserted in the LVTSCR1 (LVTSCR2) device, in its snapback-breakdown condition. This also proves the correct concept and design of this complementary-LVTSCR ESD protection circuit.

Fig. 11, which is measured from the pad with 5-V VDD and 0-V VSS, shows the voltage clamping effect of diodes D1 and D2 in this complementary-LVTSCR ESD protection circuit. The voltage level of input signals at the pad is clamped between $+5.6$ V and -0.6 V. This clamping effect of diodes also further guarantees that the LVTSCR1 and LVTSCR2 devices are not triggered on for CMOS IC's in normal operating conditions, because the trigger voltage of LVTSCR1 (LVTSCR2) is as high as -16.98 V. (15.50 V). But, in the modified complementary-LVTSCR ESD protection circuit for application in mixed-voltage interface or the DRAM IC's with negative substrate bias, the diode D2 is absent, so the high-level voltage clamping effect is also removed. Under this application, the voltage level of input signal should be avoided to exceed the trigger voltage of LVTSCR2 (15.5 V).

Fig. 12 shows the comparison of leakage currents in the fabricated complementary-LVTSCR ESD protection circuit

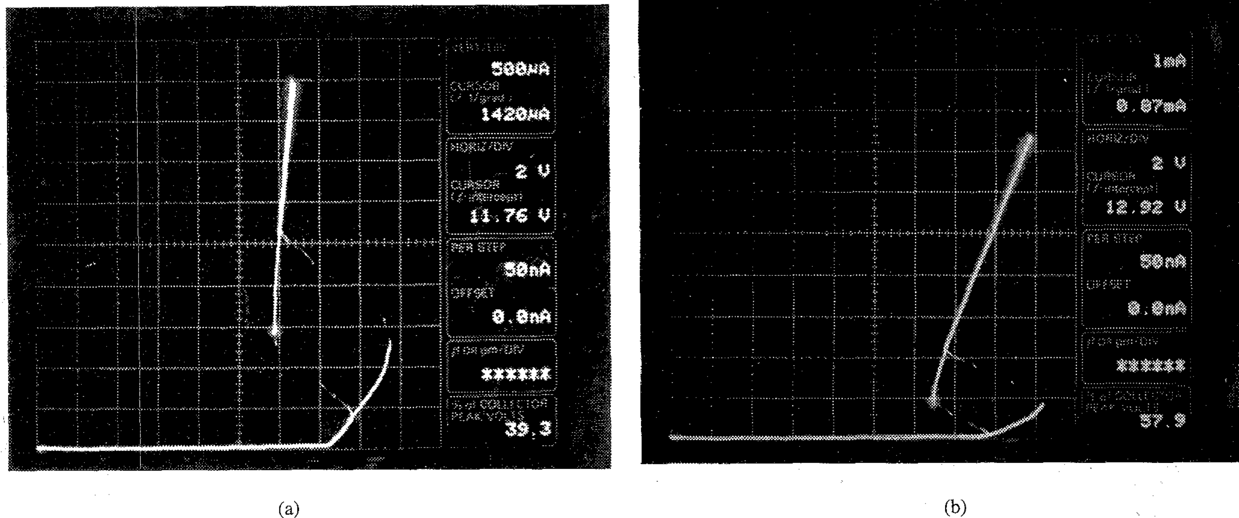


Fig. 13. Measured I-V characteristics of VDD-to-VSS latchup in the fabricated complementary-LVTSCR ESD protection circuit under operating temperature of (a) 25°C, and (b) 150°C.

and the conventional CMOS ESD protection circuit, which is measured (by HP4145) by applying a voltage ramp from 0 V to 5 V to the input pad with 5-V VDD and 0-V VSS bias condition. In Fig. 12(a), the input leakage current at 5-V input voltage bias in the complementary-LVTSCR ESD protection circuit is only 1.358 nA. But in Fig. 12(b), the input leakage current in the conventional CMOS ESD protection circuit is up to 8.189 nA. The input leakage current is proportional to the total diffusion area which connected to the pad. Due to the layout area of complementary-LVTSCR ESD protection circuit is only 0.52 times to that of the conventional CMOS ESD protection circuit, the leakage current in the complementary-LVTSCR ESD protection circuit is much smaller. Moreover, the input junction capacitance is also proportional to the diffusion area connected to the pad, the input capacitance of this complementary-LVTSCR ESD protection circuit is believed to be smaller than that of the conventional CMOS ESD protection circuit. With low leakage current and low input capacitance, this complementary-LVTSCR ESD protection circuit is more suitable to protect the input pins of analog CMOS IC's in high-precision applications.

The above experimental data and curves are all measured in the room temperature with air condition about 26°C. To verify the thermal stability of LVTSCR1, LVTSCR2, and parasitic VDD-to-VSS latchup path in the complementary-LVTSCR ESD protection circuit, some test chips are assembled in the ceramic package for high-temperature measurement environments. A *ThermoChuck* system with high temperature range up to 200°C and temperature accuracy of ±0.5°C, produced by *TEMPTRONIC* in USA, is used to investigate the thermal effect on the fabricated complementary-LVTSCR ESD protection circuit. Fig. 13(a) shows the I-V curve measured from VDD to VSS nodes in the complementary-LVTSCR ESD protection circuit to monitor the VDD-to-VSS latchup issue under temperature condition of 25°C. It is shown that the holding voltage (current) of VDD-to-VSS latchup is as high as 11.76 V (1.42 mA). With increase of operating temperature of the ceramic package up to 150°C, the measured VDD-to-VSS latchup characteristics is shown in Fig. 13(b), in which the holding voltage (current) is as high as 12.92 V (0.87 mA). The dependence of the holding voltage (current) of VDD-to-VSS latchup path in the fabricated complementary-LVTSCR ESD protection circuit on the temperature parameter are shown in Fig. 14. It is shown that the higher temperature leads to higher holding voltage but smaller holding current. The increase of holding voltage at high temperature is due to the increase of decoupling effect of latchup guard rings and the long-distance P-substrate resistance along the VDD-to-VSS latchup path. The higher temperature (above room temperature) leads to higher resistivity of silicon substrate [15]. The long-distance P-substrate resistance along the VDD-to-VSS latchup path increases as temperature increases, so it enhances decoupling effect and causes the increase of holding voltage. Thus, this complementary-LVTSCR ESD protection circuit has been experimentally guaranteed to be free of VDD-to-VSS latchup problem in 5-V CMOS IC's under high-temperature operating conditions.

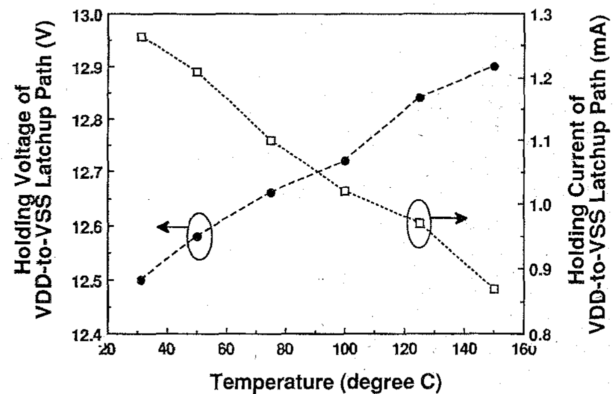


Fig. 14. The dependence of holding voltage (current) of VDD-to-VSS latchup path in the complementary-LVTSCR ESD protection circuit on temperature variation.

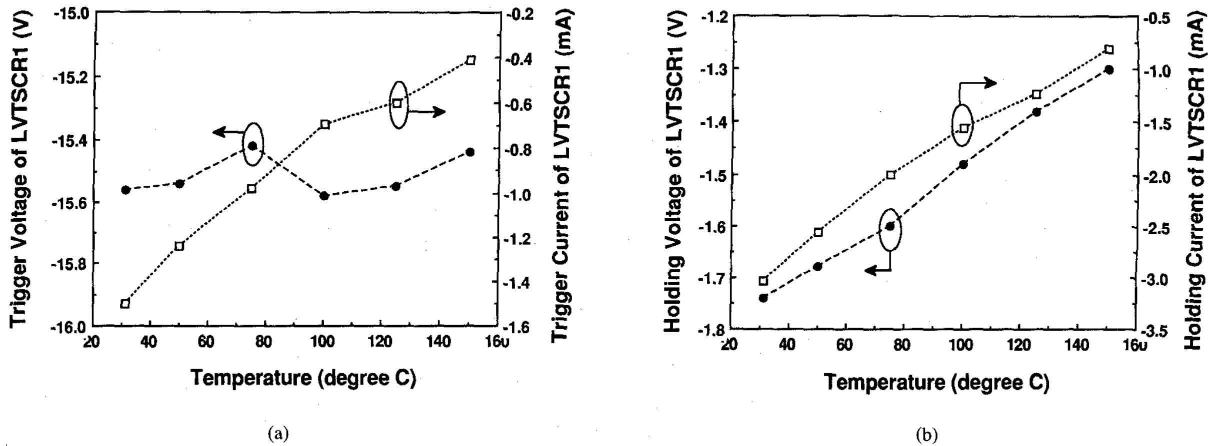


Fig. 15. The temperature effects on (a) the trigger voltage (current), and (b) the holding voltage (current), of the LVTSCR1 device.

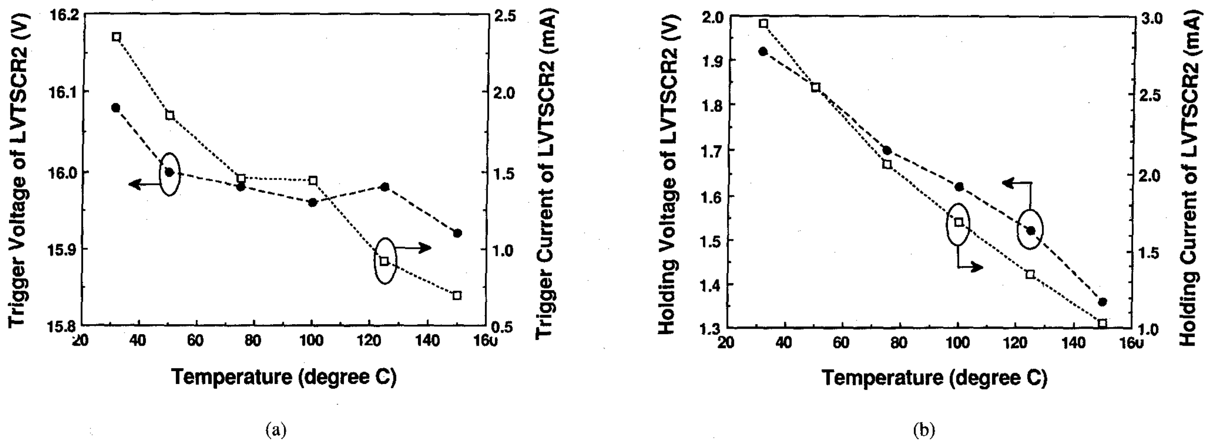


Fig. 16. The temperature effects on (a) the trigger voltage (current), and (b) the holding voltage (current), of the LVTSCR2 device.

To investigate the temperature effect on the complementary-LVTSCR ESD protection circuit, the I-V characteristics of LVTSCR1 and LVTSCR2 devices in the ceramic package are also measured under different temperatures from 30°C to 150°C. The measured results are shown in Figs.15 and 16. Fig. 15(a) shows the relation between the trigger voltage (current) of LVTSCR1 and the temperature. The dependence of holding voltage (current) of LVTSCR1 on the temperature is shown in Fig. 15(b). Fig. 16(a) shows the relation between the trigger voltage (current) of LVTSCR2 and the temperature. The dependence of holding voltage (current) of LVTSCR2 on the temperature is shown in Fig. 16(b). It is found that the trigger voltages of LVTSCR1 and LVTSCR2 are not sensitive to temperature variation because they are triggered on by the snapback breakdown of short-channel thin-oxide PMOS or NMOS which inserted in the lateral SCR structures. But, the holding voltages and currents of LVTSCR1 and LVTSCR2 decrease (in absolute value) as temperature increases. This means that the latchup capability of LVTSCR1 and LVTSCR2 is increased as temperature increases. This behavior is quite different to the VDD-to-VSS latchup characteristics because there are no decoupling guard rings or long-distance substrate resistance in the latchup paths of LVTSCR1 and LVTSCR2 structures. Through above experimental investigation, it is safely proved that this proposed complementary-LVTSCR ESD protection can still remain inactive and still be free of VDD-to-VSS latchup under high-temperature operating environment.

IV. Conclusion

A robust ESD protection circuit with complementary-LVTSCR structures and junction diodes has been designed, fabricated, and tested in submicron CMOS technology. The trigger voltage of lateral SCR device is lowered by inserting a short-channel thin-oxide PMOS (NMOS) into the lateral SCR structure to form the LVTSCR1 (LVTSCR2) device. Thus, the trigger voltage of LVTSCR1 (LVTSCR2) device is equivalent to the snapback-breakdown voltage of short-channel thin-oxide PMOS (NMOS) device. But, the holding voltages of LVTSCR1 and LVTSCR2 devices are still the same as the original holding voltage of lateral SCR device. By the complementary-style arrangement of LVTSCR1, LVTSCR2, D1, and D2 devices from the pad to both VDD and VSS power lines, this complementary-LVTSCR ESD protection

circuit can perform four different ESD discharging paths to effectively protect CMOS IC's against the four-mode ESD stresses without causing unexpected ESD damages on internal circuits. For applications in the mixed-voltage interface or DRAM IC's with negative substrate bias, a modified complementary-LVTSCR ESD protection circuit has been also discussed.

From experimental results, the LVTSCR1 and LVTSCR2 devices with enough lower trigger voltage can sustain much higher ESD stress within a smaller layout area than other conventional ESD protection circuits in submicron CMOS IC's with LDD process. This complementary-LVTSCR ESD protection circuit has been also guaranteed to be free of VDD-to-VSS latchup problem in 5-V CMOS IC's even under high-temperature operating condition of up to 150°C. The leakage current and input capacitance of this complementary-LVTSCR ESD protection circuit are also much smaller than those of conventional CMOS ESD protection circuit. With these excellent advantages, this complementary-LVTSCR ESD protection circuit is very suitable for advanced submicron CMOS IC's in high-density, high-reliability, and high-speed applications.

The fabrication of this proposed complementary-LVTSCR ESD protection circuit is also fully process compatible to both CMOS and BiCMOS technologies with N-well/P-substrate, P-well/N-substrate, or twin-well processes.

ACKNOWLEDGMENT

The authors wish to thank Editor T. Nakamura, and his reviewers for their valuable suggestions on revising this paper.

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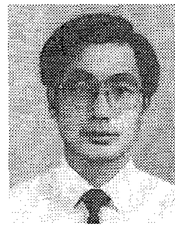

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