Available online at www.sciencedirect.com
SCIENCE DIRECT®
Microelectronic Engineering 80 (2005) 30–33
MICROELECTRONIC ENGINEERING
www.elsevier.com/locate/mee

Impact of post-deposition-annealing on the electrical characteristics of HfO_xN_y gate dielectric on Ge substrate

Chao-Ching Cheng[1], Chao-Hsin Chien[1,2], Ching-Wei Chen[1], Shih-Lu Hsu[2], Ming-Yi Yang[3], Chien-Chao Huang[3], Fu-Liang Yang[3], and Chun-Yen Chang[1]

[1]*Institute of Electronics, National Chiao-Tung University, Hsinchu, Taiwan 300, R.O.C.*
[2]*National Nano Device Laboratory, Hsinchu, Taiwan 300, R.O.C.*
[3]*Taiwan Semiconductor Manufacturing Company, Ltd., Hsinchu, Taiwan 300, R.O.C.*
Tel: 886-03-5712121 Ext:52981 email: ccheng.ee92g@nctu.edu.tw

Abstract

We systematically investigated the effect of post-deposition-annealing (PDA) on the electrical characteristics of Ge MOS capacitors with hafnium-oxynitride gate dielectric. The higher PDA temperature and longer PDA time was found to obtain the lower equivalent oxide thickness (EOT) of HfO_xN_y/Ge gate stack, however, with a larger hysteresis width. A lower EOT of 19.5 Å with a low leakage current of 1.8 x 10^{-5} A/cm^2 at V_G = -1V was achieved after 600°C annealing for 5 min. The improved capacitor properties after the PDA may be closely related to the different compositions and thicknesses of the resultant interfacial layers.

Keywords: Germanium; high-k gate dielectric; HfO_xN_y; post-deposition-annealing

1. Introduction

In recent years, high-k gate dielectrics on Si substrate have been proved being able to significantly reduce the leakage currents as compared to the traditional SiO_2/Si system, while still maintain excellent reliability and high-level of transistor performance. In order to further enhance device driving capability, Germanium is a great potential semiconductor material due to its higher intrinsic electron and hole mobilities for carrier transport. Interestingly, the lack of sufficiently stable native Ge oxide makes the integration of high-k gate dielectric on top of Ge substrate receive more and more attentions. Up to now, several metal oxides, e.g., ZrO_2 [1], HfO_2 [2,3], Al_2O_3 [4] showing promising electrical properties have been demonstrated to be suitable for Ge. Those previous works suggested that the surface passivation prior to the deposition of the metal oxides using NH_3 [5] or SiH_4 [6] annealing was needed for pursuing high-quality gate dielectrics. However, this procedure increases the process complexity as well as the electron-trapping rate due to hydrogen incorporation [7]. Since the hafnium oxynitride (HfO_xN_y) has a higher crystallization temperature (800°C) than pure HfO_2 (400°C) and the

0167-9317/$ - see front matter
doi:10.1016/j.mee.2005.04.033

nitrogen incorporation can strengthen the immunity against oxygen diffusion for suppressing the interfacial layer (IL) formation during processing. In this work, we systematically investigated the impact of post-deposition-annealing (PDA) on the electrical properties of HfO_xN_y dielectric on the Ge substrates.

2. Experimental

The Ge substrate used was (100) Ga-doped p-type wafers with a resistivity of 25-29 Ω·cm. The wafers were subject to a cleaning processing of deionized (DI) water rinse followed by diluted HF (1:50) dipping for several cycles. After drying, the HfN thin-films were deposited with reactive sputtering with a pure Hf target, followed by a PDA with rapid thermal system for oxidation and densification. The HfN sputtering was performed in an $Ar+N_2$ ambient [$N_2/Ar+N_2$=0.33] with a power of 150 W and a chamber pressure of 7.6 mTorr. To avoid excess oxidation and minimize the IL, the PDA was carried out in an N_2 ambient instead of O_2 ambient for converting HfN into HfO_xN_y. The effects of PDA temperature and time on electrical performance of the HfO_xN_y gate dielectric on Ge substrate were investigated. The temperatures chosen were 400°C, 500°C, and 600°C with the duration times of 1 min, 3 min, and 5 min, respectively. After that, a 1000Å Pt was deposited by e-beam evaporation through a shadow mask to define the capacitor gate electrode, subsequently, the post metallization anneal (PMA) was performed at the temperature of 400°C for 30 sec. Finally, Al was deposited on the backside of Ge wafer to reduce the contact and series resistances, followed by the forming gas annealing (10% H_2/N_2, 300°C, 30 min). The thickness of sputtered dielectric films before and after PDA was taken by focused ion beam (FIB) technique. The capacitance–voltage (C–V) and current–voltage (I–V) characteristics of each capacitor were measured by using an HP4284 LCR meter, and a Keithley 4200 semiconductor characterization system, respectively.

3. Results and Discussion

Figure 1 shows the typical high frequency (100MHz) C-V characteristics of HfO_xN_y/p-Ge capacitors before and after PDA with different temperatures. The HfO_xN_y/p-Si MOS capacitor without PDA is also included for comparison. It was observed that the accumulation capacitance of the as-deposited HfO_xN_y dielectric on Ge was apparently higher than that on Si regardless of the completely identical fabrication processing. The resultant difference in EOT value, evaluated at V_g = -2V, between these two samples is about 0.5 nm. Meanwhile, the lower inversion capacitance upon increasing annealing temperature indicates that the high temperature PDA step is helpful to diminish the process-induced and/or in-situ defects in the Ge substrate.

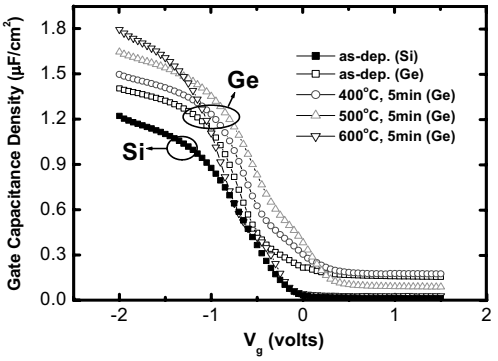

Fig. 1 The 100 kHz C-V characteristics of Pt/HfO_xN_y/Ge (open symbols) MOS capacitors before and after the PDA. For comparison, as-deposited HfO_xN_y on Si (solid symbols) was also shown.

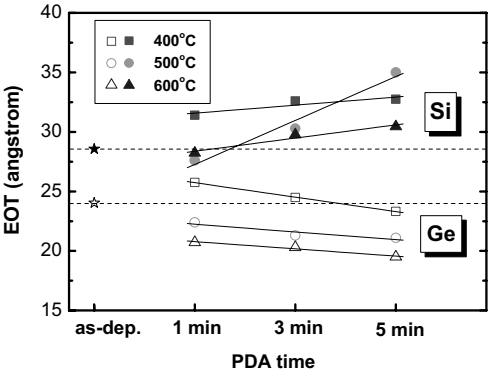

Fig. 2 The EOT dependence of the HfO_xN_y film on Si (solid symbols) and Ge (open symbols) substrates on the PDA temperature and time.

Moreover, the inversion capacitance was found to reveal a significant dependence on the measuring frequency, differing from that observed in the Si case and the higher PDA is the weaker frequency dependence is (not shown). This feature might be due

to the fast minority carrier generation rate in Ge substrate because of its smaller bandgap and the reduced density of bulky defects originating from the sputtering process by PDA. Meanwhile, a small bump was appeared after the PDA in the depletion region, indicating that some slow states were generated near the interface by this high temperature step.

Fig. 2 displays the variation of EOT as functions of the PDA temperature and time. In general, both the EOTs of HfO_xN_y films on Si and Ge substrates decreased with raising the PDA temperatures, however, the opposite trends of the EOT dependence on PDA time were found for these two different capacitors. To further investigate the thickness variation of Hf-oxynitride and their ILs after the PDA, the cross-sectional HRTEM pictures are shown in Fig. 3. We found that the thickness of HfO_xN_y dielectric deposited on both substrates was identical, while the IL was thicker in HfO_xN_y/Si than HfO_xN_y/Ge for the as-deposited samples. The IL thickness difference can explain the result in Fig. 1. After annealing, these two stacks exhibit the distinct thickness variation behaviors over PDA time, which seems consistent with the result shown in Fig. 2.

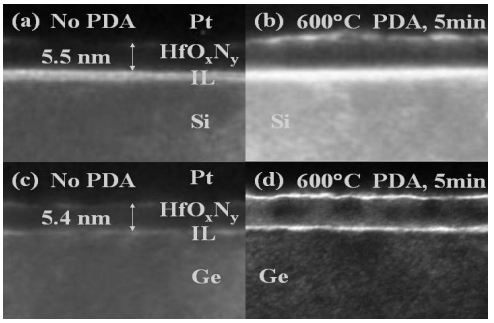

Fig.3 Cross-sectional HRTEM images of HfO_xN_y films on Si (a)-(b) and Ge (c)-(d) substrates before and after the PDA.

Fig. 4 shows the effect of PDA on the hysteresis width. Higher PDA temperatures and longer times led to the smaller hysteresis widths for the HfO_xN_y/Si gate stacks, whereas resulted in the larger hysteresis widths for HfO_xN_y/Ge gate stacks, especially for the case of 600°C. Besides, in order to correctly observe the PDA effect on the shift of flatband voltage (V_{FB}), the maximum/minimum biases in the two-way C-V sweep was carefully chosen for avoiding the significant charge trapping. The results are presented in Fig. 5. The V_{FB} of as-deposited HfO_xN_y on Ge was (0.72±0.3) V, which is close to the work-function difference between Pt gate of (5.4±0.3) eV [10] and p-Ge substrate of 4.55 eV. A noticeable feature is that independent of the PDA time, the negative V_{FB} shift was found with raising the PDA temperature, implying that more fixed positive charges were introduced in the gate dielectric/IL, especially for 600°C annealing. The lowered V_{FB} after the PDA may be involved with the concentration of nitrogen in the gate dielectric/IL. Similar V_{FB} shift due to nitrogen addition was reported in the HfO_xN_y [11], ZrO_xN_y [12], and SiO_xN_y [13] dielectrics, etc.

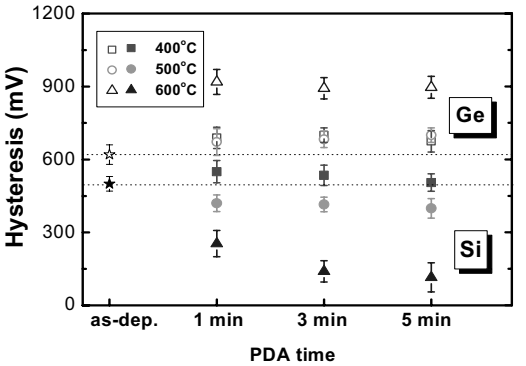

Fig. 4 The hysteresis dependence of the HfO_xN_y film on Si (solid symbols) and Ge (open symbols) substrates on the PDA temperature and time.

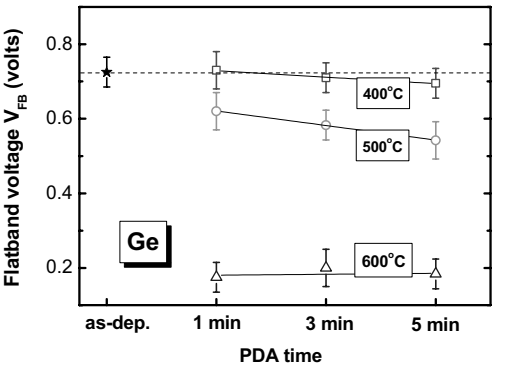

Fig. 5 The flatband voltage V_{FB} of the HfO_xN_y/Ge before (solid symbol) and after the PDA (open symbols).

We speculate that the differences of electrical characteristics between two capacitor systems after annealing may be closely related to the different

compositions and thicknesses of the resultant interfacial layers. For HfO_xN_y/Si, the IL is likely to grow during annealing and hence result in the increase in the EOT, as seen in Fig. 3. However, the situation seems different for HfO_xN_y/Ge. The IL of HfO_xN_y/Ge was confirmed to be hafnium-germanium mixed oxynitride from the FTIR and electron dispersive spectrometer (EDX) spectra (data not shown). The further examinations are in analysis for clarifying the detailed mechanism.

Fig. 6 depicts the room-temperature leakage current characteristics of Pt/HfO_xN_y/p-Ge measured at both bias polarities. Remarkably, the HfO_xN_y/p-Ge revealed extremely low gate leakage current with near 4 orders of magnitude reduction as compared to the standard SiO_2/Si with the similar EOT. From the Fig. 7, these Ge MOS capacitors also showed superior insulating properties with respect to other Hf-based gate dielectrics on n-Ge. Noted that the surface passivation of Ge substrate is needed before HfO_2 deposition to obtain the lower gate leakage.

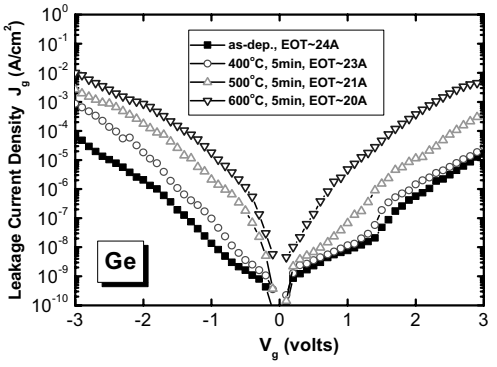

Fig. 6 The gate leakage current-voltage (J-V) characteristics of Pt/HfO_xN_y/Ge MOS capacitors before (solid symbols) and after PDA (open symbols).

4. Conclusions

The effect of post-deposition-annealing on the electrical characteristics of Ge MOS capacitors with HfO_xN_y gate dielectric has been studied. A lower EOT of 19.5 Å with a low leakage current of 1.8 x 10^{-5} A/cm^2 at V_G = -1V was achieved after dielectric annealing at 600°C for 5min, even though a larger hysteresis was observed. The continuous optimization of the interface structure through process modification is expected to further improve the electrical performance of the HfO_xN_y/Ge gate stack, which thus be considered as a promising gate dielectric of Ge device.

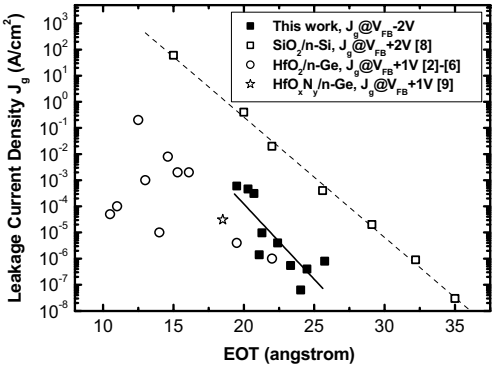

Fig. 7 Gate leakage currents versus the EOT of Pt/HfO_xN_y/p-Ge MOS capacitors (solid symbols) were plotted together with other's published data (open symbols).

Acknowledgements

The authors were grateful to the financial support from Taiwan Semiconductor Manufacturing Company, Ltd.

References

[1] H. Kim et al., Appl. Phys. Lett. 83, (2003) 2647-2649.
[2] E. P. Gusev et al., Appl. Phys. Lett. 85, (2004) 2334-2336.
[3] N. Wu et al., Appl. Phys. Lett. 84, (2004) 3741-3743.
[4] J. J.-H. Chen et al., IEEE Trans. Electron Dev. ED-51, (2004) 1441-1447.
[5] H. Kim et al., Appl. Phys. Lett. 85, (2004) 2902-2904.
[6] N. Wu et al., IEEE Electron Dev. Lett. 25, (2004) 631-633.
[7] T. Hori et al., J. Appl. Phys. 65, (1989) 629-635.
[8] S. H. Lo et al., IEEE Electron Dev. Lett. 18, (1997) 209-211.
[9] Q.-C. Zhang et al., Jpn. J. Appl. Phys. 43, (2004) L1208-L1210.
[10] R. C. Weast ed., CRC Handbook of Chemistry and Physics, (CRC, Boca Raton, FL, 1985)12-124.
[11] C. S. Kang et al., IEEE Trans. Electron Dev. ED-51, (2004) 220-227.
[12] R. E. Nieh et al., IEEE Trans. Electron Dev. ED-50, (2003) 333-340.
[13] P. Pan, and C. Paquette, Appl. Phys. Lett. 47, (1985) 473-475.